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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90352espmc1-gs-163e1



# 1. Product Lineup1 (Without Clock supervisor function)

■ Flash memory products

Part Number	MB90F351E	MB90F351TE	MB90F351ES	MB90F351TES					
	MB90F352E	MB90F352TE	MB90F352ES	MB90F351TES					
Parameter									
Туре		Flash memo							
CPU		F <sup>2</sup> MC-16	SLX CPU						
System clock	Minimum instruction execut	PLL clock multiplication circuit ( $\times$ 1, $\times$ 2, $\times$ 3, $\times$ 4, $\times$ 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL $\times$ 6)							
ROM		MB90F351E(S), MB90F352 Flash memory (Erase/write a 2TE(S)		at the same time):					
RAM		4 Kb	ytes						
Emulator-specific power supply*		-	-						
Sub clock pin (X0A, X1A) (Max 100 kHz)	Ye	es	ı	No					
Clock supervisor		N	0						
Low voltage/CPU operation detection reset	No	Yes	No Yes						
Operating voltage		perating (not using A/D conv converter/Flash programmi ernal bus							
Operating temperature		–40°C to	+125°C						
Package		LQFI	P-64						
		2 cha	nnels						
LIN-UART	Special synchronous option	ttings using a dedicated bau is for adapting to different sy ther as master or slave LIN o	nchronous serial protocols	ner)					
I <sup>2</sup> C (400 kbps)		1 cha	annel						
		15 cha	annels						
A/D converter	10-bit or 8-bit resolution Conversion time : Min 3 μs	includes sample time (per c	one channel)						
16-bit reload timer (2 channels)	Operation clock frequency : Supports External Event Co	fsys/ $2^1$ , fsys/ $2^3$ , fsys/ $2^5$ (fsyout function.	ys = Machine clock frequen	icy)					
40 hit Farance "	Free-run Timer 0 (clock inputere-run Timer 1 (clock inputere-run Timer 1)	ut FRCK0) corresponds to I0 ut FRCK1) corresponds to I0	CU0/1. CU4/5/6/7, OCU4/5/6/7.						
(2 channels)	6-bit Free-run timer 2 channels)  Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4). Operation clock frequency: fsys, fsys/2 <sup>1</sup> , fsys/2 <sup>2</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>4</sup> , fsys/2 <sup>5</sup> , fsys/2 <sup>6</sup> , fsys/2 <sup>7</sup> (fsys = Machine clock frequency)								
16 hit output		4 cha	nnels						
16-bit output compare		6-bit free-run Timer matches can be used to generate an		ters.					



■ MASK ROM products/Evaluation products

Part Number Parameter	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-1 01	MB90V340E-1		
Туре		MASK RO	M products		Evaluation products			
CPU			F <sup>2</sup> MC-1	6LX CPU				
System clock	·	•	2, ×3, ×4, ×6, 1/2 v 42 ns (oscillation of	when PLL stops) clock 4 MHz, PLL ×	6)			
ROM	,	B90351E(S), MB90 B90352E(S), MB90	` '		Exte	ernal		
RAM		4 Kt	oytes		30 K	bytes		
Emulator-specific power supply*		-	_		Y	es		
Sub clock pin (X0A, X1A) (Max 100 kHz)	Ye	es	N	No	No	Yes		
Clock supervisor			N	lo	•	1		
Low voltage/CPU operation detection reset	No	Yes	No	Yes	N	lo		
Operating voltage range	4.0 V to 5.5 V : at	normal operating ( using A/D converte using external bus	5 V ± 10%					
Operating temperature range		−40°C to	+125°C		_			
Package		LQF	P-64		PGA-299			
		2 cha	innels		5 channels			
LIN-UART	Special synchrono	ous options for ada		d rate generator (re nchronous serial p device				
I <sup>2</sup> C (400 kbps)		1 cha	annel		2 cha	nnels		
		15 ch	annels		24 ch	annels		
A/D converter		10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)						
		2 cha	innels		4 cha	nnels		
16-bit reload timer	Operation clock frequency: fsys/2 <sup>1</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>5</sup> (fsys = Machine clock frequency) Supports External Event Count function.							
16-bit free-run timer (2 channels)	Free-run Timer 0 ( Free-run Timer 1 (	Free-run Timer 0 corresponds to ICU0/1/2/3, OCU0/1/2/3. Free-run Timer 1 corresponds to ICU4/5/6/7, OCU4/5/6/7.						
•	Supports Timer Ci Operation clock from	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4). Operation clock frequency: fsys, fsys/2 <sup>1</sup> , fsys/2 <sup>2</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>4</sup> , fsys/2 <sup>5</sup> , fsys/2 <sup>6</sup> , fsys/2 <sup>7</sup> (fsys = Machine clock frequency)						



Part Number Parameter	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-1 01	MB90V340E-1 02				
		4 cha	ınnels		8 channels					
16-bit output compare		Signals an interrupt when 16-bit free-run Timer matches output compare registers.  A pair of compare registers can be used to generate an output signal.								
40 hit is not a set of		6 cha	innels		8 cha	annels				
16-bit input capture	Retains 16-bit free	e-run timer value by	/ (rising edge, fallin	ig edge, or the both	n edges), signals ar	n interrupt.				
8/16-bit programmable pulse gen- erator	8-	6 channels (16-bit) 8-bit reload o bit reload registers bit reload registers	8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16							
cidio	Supports 8-bit and 16-bit operation modes.  A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter.  Operation clock frequency: fsys, fsys/2 <sup>1</sup> , fsys/2 <sup>2</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>4</sup> or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)									
		1 ch	3 channels							
CAN interface	Compliant with CAN standard Version 2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering: Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.									
		8 cha	innels		16 ch	annels				
External interrupt	Can be used rising edge, falling edge, starting up by "H"/"L" level input, external interrupt, extended intelligent I/O services (El <sup>2</sup> OS) and DMA.									
D/A converter	- 2 channels									
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)									
Flash memory			-							
Corresponding evaluation name	MB90V3	40E-102	MB90V3	340E-101	-					

<sup>\*:</sup> It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used. Please refer to the Emulator hardware manual about details.



## 3. Packages and Product Correspondence

Package	MB90V340E-101 MB90V340E-102 MB90V340E-103 MB90V340E-104	MB90351E (S), MB90351TE (S) MB90F351E (S), MB90F351TE (S) MB90352E (S), MB90352TE (S) MB90F352E (S), MB90F352TE (S) MB90F356E (S), MB90356TE (S) MB90F356E (S), MB90F356TE (S) MB90F357E (S), MB90F357TE (S)
PGA-299C-A01	$\circ$	×
FPT-64P-M23 (12.0 mm, 0.65 mm pitch)	×	0
FPT-64P-M24 (10.0 mm, 0.50 mm pitch)	×	0

 $\bigcirc$ : Yes,  $\times$ : No

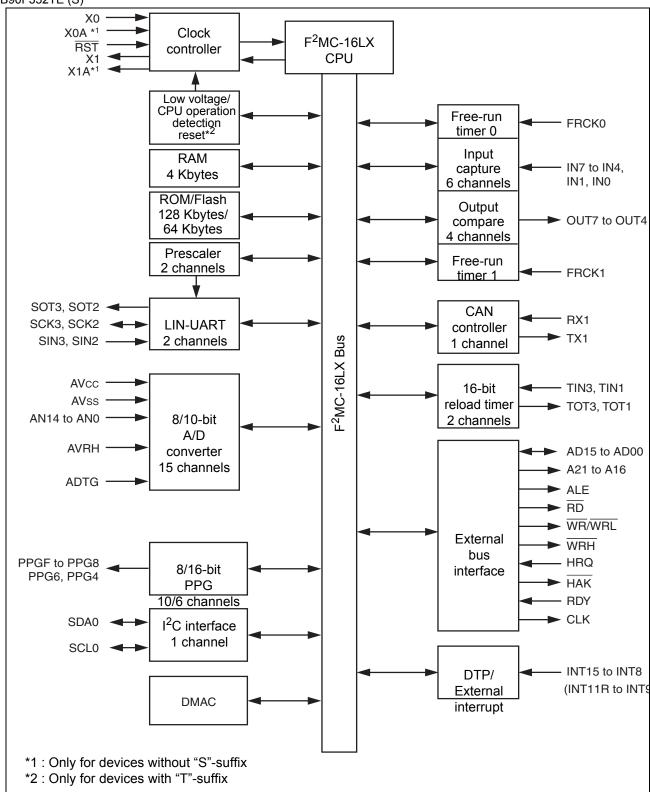
Note: Refer to "Package Dimensions" for detail of each package.



Pin No.	Pin name	I/O Circuit type*	Function
	P30	_	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
54	ALE	G	Address latch enable output pin. This function is enabled when external bus is enabled.
	IN4	1	Data sample input pin for input capture ICU4
	P31		General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
55	RD	G	Read strobe output pin for data bus. This function is enabled when external bus is enabled.
	IN5	1	Data sample input pin for input capture ICU5
	P32		General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the WR/WRL pin output disabled.
56	WR/WRL	G	Write strobe output pin for the data bus. This function is enabled when both the external bus and the WR/WRL pin output are enabled. WRL is used to write-strobe 8 lower bits of the data bus in 16-bit access. WR is used to write-strobe 8 bits of the data bus in 8-bit access.
	INT10R	1	External interrupt request input pin for INT10
57	P33	- G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode, in external bus 8-bit mode or with the WRH pin output disabled.
37	WRH		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.
	P34		General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
58	HRQ	G	Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT4	1	Wave form output pin for output compare OCU4
	P35		General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
59	HAK	G	Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT5	1	Wave form output pin for output compare OCU5
	P36		General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled.
60	RDY	G	Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
	OUT6		Wave form output pin for output compare OCU6



■ MB90351E (S), MB90351TE (S), MB90F351E (S), MB90F351TE (S), MB90352E (S), MB90352TE (S), MB90F352E (S)





Address	Register	Abbreviation	Access	Resource name	Initial value					
000058 <sub>H</sub>		1								
to 00005B <sub>H</sub>	Reserved									
00005C <sub>H</sub>	Output Compare Control Status Register 4	OCS4	R/W		0000XX00 <sub>B</sub>					
00005D <sub>H</sub>	Output Compare Control Status Register 5	OCS5	R/W	Output Compare 4/5	0XX00000 <sub>B</sub>					
00005E <sub>H</sub>	Output Compare Control Status Register 6	OCS6	R/W	Output Compare 6/7	0000XX00 <sub>B</sub>					
00005F <sub>H</sub>	Output Compare Control Status Register 7	OCS7	R/W	Output Compare 6/7	0XX00000 <sub>B</sub>					
000060 <sub>H</sub>	Timer Control Status Register 0	TMCSR0	R/W	40 hit Daland Times 0	00000000 <sub>B</sub>					
000061 <sub>H</sub>	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	XXXX0000 <sub>B</sub>					
000062 <sub>H</sub>	Timer Control Status Register 1	TMCSR1	R/W	4C hit Daland Timen 4	00000000 <sub>B</sub>					
000063 <sub>H</sub>	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	XXXX0000 <sub>B</sub>					
000064 <sub>H</sub>	Timer Control Status Register 2	TMCSR2	R/W	40 hit Daland Times 0	00000000 <sub>B</sub>					
000065 <sub>H</sub>	Timer Control Status Register 2	TMCSR2	R/W	16-bit Reload Timer 2	XXXX0000 <sub>B</sub>					
000066 <sub>H</sub>	Timer Control Status Register 3	TMCSR3	R/W	40.1 " D 1 1 1 1 1 2	00000000 <sub>B</sub>					
000067 <sub>H</sub>	Timer Control Status Register 3	TMCSR3	R/W	16-bit Reload Timer 3	XXXX0000 <sub>B</sub>					
000068 <sub>H</sub>	A/D Control Status Register 0	ADCS0	R/W		000XXXX0 <sub>B</sub>					
000069 <sub>H</sub>	A/D Control Status Register 1	ADCS1	R/W		0000000X <sub>B</sub>					
00006A <sub>H</sub>	A/D Data Register 0	ADCR0	R	A /D O	00000000 <sub>B</sub>					
00006B <sub>H</sub>	A/D Data Register 1	ADCR1	R	A/D Converter	XXXXXX00 <sub>B</sub>					
00006C <sub>H</sub>	ADC Setting Register 0	ADSR0	R/W		00000000 <sub>B</sub>					
00006D <sub>H</sub>	ADC Setting Register 1	ADSR1	R/W		00000000 <sub>B</sub>					
00006E <sub>H</sub>	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low Voltage/CPU Operation Detection Reset	00111000 <sub>B</sub>					
00006F <sub>H</sub>	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	XXXXXXX1 <sub>B</sub>					
000070 <sub>H</sub> to 00007F <sub>H</sub>	Reserved									
000080 <sub>H</sub> to 00008F <sub>H</sub>	Reserved for CAN controller 1. Refer to "CAN Controllers"									
000090 <sub>H</sub> to 00009A <sub>H</sub>	Reserved									



Address	Posistor	Abbreviation	A00000	Initial Value	
CAN1	Register	Appreviation	Access		
007D00 <sub>H</sub>	Control status register	CSR	R/W, W	0XXXX0X1 <sub>B</sub>	
007D01 <sub>H</sub>	Control status register	CSK	R/W, R	00XXX000 <sub>B</sub>	
007D02 <sub>H</sub>	Last event indicator register	LEIR	R/W	000X0000 <sub>B</sub>	
007D03 <sub>H</sub>	Last event indicator register	LLIIV	1000	XXXXXXXX <sub>B</sub>	
007D04 <sub>H</sub>	Receive/transmit error counter	RTEC	R	00000000 <sub>B</sub>	
007D05 <sub>H</sub>	Neceive/transmit error counter	KILO	IX.	00000000 <sub>B</sub>	
007D06 <sub>H</sub>	Bit timing register	BTR	R/W	11111111 <sub>B</sub>	
007D07 <sub>H</sub>	Dit tilling register	BIK	1000	X1111111 <sub>B</sub>	
007D08 <sub>H</sub>	IDE register	IDER	R/W	$XXXXXXXX_B$	
007D09 <sub>H</sub>	IDE register	IDEN	1000	XXXXXXXX <sub>B</sub>	
007D0A <sub>H</sub>	Transmit RTR register	TRTRR	R/W	00000000 <sub>B</sub>	
007D0B <sub>H</sub>	Transmit ivity register	IIVIIII	1000	00000000 <sub>B</sub>	
007D0C <sub>H</sub>	Remote frame receive waiting	RFWTR	R/W	XXXXXXXX <sub>B</sub>	
007D0D <sub>H</sub>	register	IXI VVIIX	1000	XXXXXXXX <sub>B</sub>	
007D0E <sub>H</sub>	Transmit interrupt	TIER	R/W	00000000 <sub>B</sub>	
007D0F <sub>H</sub>	enable register	TILIX	1000	00000000 <sub>B</sub>	
007D10 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007D11 <sub>H</sub>	Acceptance mask	AMSR	R/W	XXXXXXXX <sub>B</sub>	
007D12 <sub>H</sub>	select register		1000	XXXXXXXX <sub>B</sub>	
007D13 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007D14 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007D15 <sub>H</sub>	Acceptance mask register 0	AMR0	R/W	XXXXXXXX <sub>B</sub>	
007D16 <sub>H</sub>	Acceptance mask register o	Alviito	1000	XXXXXXXX <sub>B</sub>	
007D17 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007D18 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007D19 <sub>H</sub>	Acceptance mask register 1	AMR1	R/W	XXXXXXXX <sub>B</sub>	
007D1A <sub>H</sub>	Acceptance mask register i	AIVIRI	F/VV	XXXXXXXX <sub>B</sub>	
007D1B <sub>H</sub>				$XXXXXXXX_B$	



## **List of Message Buffers (ID Registers)**

Address	Register	Abbreviation	Access	Initial Value	
CAN1	Register	Abbreviation	Access	miliai vaido	
007C00 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
to 007C1F <sub>H</sub>	General-purpose RAM	_	R/W	to XXXXXXX <sub>B</sub>	
007C20 <sub>H</sub>			+	XXXXXXXX	
007C21 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C22 <sub>H</sub>	ID register 0	IDR0	R/W	XXXXXXXX	
007C23 <sub>H</sub>				XXXXXXXXB	
007C24 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C25 <sub>H</sub>				XXXXXXXXB	
007C26 <sub>H</sub>	ID register 1	IDR1	R/W	XXXXXXXX <sub>B</sub>	
007C27 <sub>H</sub>				XXXXXXXXB	
007C28 <sub>H</sub>			1	XXXXXXXX <sub>B</sub>	
007C29 <sub>H</sub>				XXXXXXXXB	
007C2A <sub>H</sub>	ID register 2	IDR2	R/W	XXXXXXXX <sub>B</sub>	
007C2B <sub>H</sub>				XXXXXXXXB	
007C2C <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C2D <sub>H</sub>	ID as vistos 0	IDR3	DAM	XXXXXXXXB	
007C2E <sub>H</sub>	ID register 3		R/W	XXXXXXXX <sub>B</sub>	
007C2F <sub>H</sub>				$XXXXXXXX_B$	
007C30 <sub>H</sub>				XXXXXXXX	
007C31 <sub>H</sub>	ID variatas 4	IDR4	R/W	XXXXXXXXB	
007C32 <sub>H</sub>	ID register 4		R/W	XXXXXXXX <sub>B</sub>	
007C33 <sub>H</sub>			XXXXXXXXB		
007C34 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C35 <sub>H</sub>	ID register 5	IDR5	R/W	XXXXXXXXB	
007C36 <sub>H</sub>	ID register 5	פאטו	K/VV	XXXXXXXX <sub>B</sub>	
007C37 <sub>H</sub>				XXXXXXXXB	
007C38 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C39 <sub>H</sub>	ID register 6	IDR6	R/W	XXXXXXXXB	
007C3A <sub>H</sub>	up register o	סאטו	[N/VV	XXXXXXXX <sub>B</sub>	
007C3B <sub>H</sub>				XXXXXXXXB	
007C3C <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C3D <sub>H</sub>	ID register 7	IDD7	D/M	XXXXXXXXB	
007C3E <sub>H</sub>	ID register 7	IDR7	R/W	XXXXXXXX <sub>B</sub>	
007C3F <sub>H</sub>				XXXXXXXXB	



Address	Register	Abbreviation	Access	Initial Value	
CAN1	Negistei	Abbieviation	Access	illitiai value	
007C40 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C41 <sub>H</sub>	ID register 8	IDR8	R/W	XXXXXXXX <sub>B</sub>	
007C42 <sub>H</sub>	ib register o	IDRO	INVV	XXXXXXXX <sub>B</sub>	
007C43 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C44 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C45 <sub>H</sub>	ID register 9	IDR9	R/W	XXXXXXXX <sub>B</sub>	
007C46 <sub>H</sub>	ib register 9	IDIX9	1000	XXXXXXXX <sub>B</sub>	
007C47 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C48 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C49 <sub>H</sub>	ID register 10	IDR10	R/W	XXXXXXXX <sub>B</sub>	
007C4A <sub>H</sub>	ID register to	IDKIU	17/1/	XXXXXXXX <sub>B</sub>	
007C4B <sub>H</sub>				XXXXXXXXB	
007C4C <sub>H</sub>			R/W	XXXXXXXX <sub>B</sub>	
007C4D <sub>H</sub>	ID register 11	IDR11		$XXXXXXXX_B$	
007C4E <sub>H</sub>	ib register 11	IDICIT	F/VV	XXXXXXXX <sub>B</sub>	
007C4F <sub>H</sub>				$XXXXXXXX_B$	
007C50 <sub>H</sub>		IDR12	R/W	XXXXXXXX <sub>B</sub>	
007C51 <sub>H</sub>	ID register 12			$XXXXXXXX_B$	
007C52 <sub>H</sub>	ID register 12		F/VV	XXXXXXXX <sub>B</sub>	
007C53 <sub>H</sub>				$XXXXXXXX_B$	
007C54 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C55 <sub>H</sub>	ID register 13	IDR13	R/W	$XXXXXXXX_B$	
007C56 <sub>H</sub>	ib register 13	IDK13	F/VV	XXXXXXXX <sub>B</sub>	
007C57 <sub>H</sub>				XXXXXXXXB	
007C58 <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C59 <sub>H</sub>	ID register 14	IDR14	R/W	XXXXXXXX <sub>B</sub>	
007C5A <sub>H</sub>	ID register 14	IDK 14	17/1/	XXXXXXXX <sub>B</sub>	
007C5B <sub>H</sub>				XXXXXXXXB	
007C5C <sub>H</sub>				XXXXXXXX <sub>B</sub>	
007C5D <sub>H</sub>	ID register 15	IDR15	R/W	XXXXXXXXB	
007C5E <sub>H</sub>	ID register 15	פואטו	TV VV	XXXXXXXX <sub>B</sub>	
007C5F <sub>H</sub>				XXXXXXXXB	

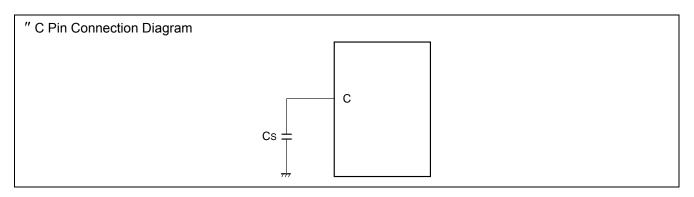


### 13.2 Recommended Operating Conditions

 $(V_{SS} = AV_{SS} = 0 V)$ 

Parameter	Symbol		Value		Unit	Remarks
raiailletei	Syllibol	Min	Тур	Max	Oilit	Remarks
		4.0	5.0	5.5	V	Under normal operation
Power supply voltage	V <sub>CC</sub> , AV <sub>CC</sub>	3.5	5.0	5.5	٧	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	_	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C <sub>S</sub>	0.1	_	1.0	μF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V <sub>CC</sub> pin should be greater than this capacitor.
Operating temperature	T <sub>A</sub>	-40	_	+125	°C	*

 $<sup>^*</sup>$ : If used exceeding  $T_A = +105^{\circ}C$ , be sure to contact Cypress for reliability limitations.



#### WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



## 13.4 AC Characteristics

### 13.4.1 Clock Timing

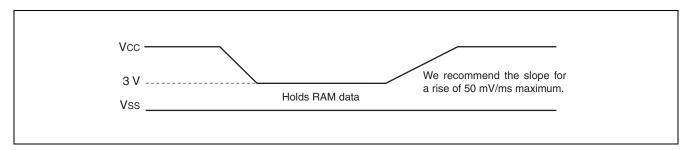
(T\_A = -40 °C to +125 °C, V\_{CC} = 5.0 V  $\pm$  10%,  $f_{CP} \leq$  24 MHz,  $V_{SS} = AV_{SS} = 0$  V)

Dovementor	Compleal	Di-	Value			I I mit	Domonico
Parameter	Symbol	Pin	Min	Тур	Max	Unit	Remarks
			3	_	16	MHz	1/2 (at PLL stop) When using an oscillation circuit
			4	_	16	MHz	1 multiplied PLL When using an oscillation circuit
		X0, X1	4	_	12	MHz	2 multiplied PLL When using an oscillation circuit
		λ0, λ1	4	_	8	MHz	3 multiplied PLL When using an oscillation circuit
			4	ı	6	MHz	4 multiplied PLL When using an oscillation circuit
	f <sub>C</sub>		-	_	4	MHz	6 multiplied PLL When using an oscillation circuit
Clock frequency	ic ic	X0	3	_	24	MHz	1/2 (at PLL stop), When using an external clock
			4	_	24	MHz	1 multiplied PLL When using an external clock
			4	_	12	MHz	2 multiplied PLL When using an external clock
			4	_	8	MHz	3 multiplied PLL When using an external clock
			4	_	6	MHz	4 multiplied PLL When using an external clock
			-	_	4	MHz	6 multiplied PLL When using an external clock
	fCL	X0A, X1A	_	32.768	100	kHz	When using sub clock
		X0, X1	62.5		333	ns	When using an oscillation circuit
Clock cycle time	t <sub>CYL</sub>	X0	41.67	_	333	ns	When using an external clock
	tCYLL	X0A, X1A	10	30.5	-	μS	
Input clock pulse width	P <sub>WH</sub> , P <sub>WL</sub>	X0	10	_	-	ns	Duty ratio should be about
Input clock pulse width	P <sub>WHL</sub> , P <sub>WLL</sub>	X0A	5	15.2	1	μS	30% to 70%.
Input clock rise and fall time	t <sub>CR</sub> , t <sub>CF</sub>	X0	_	_	5	ns	When using an external clock



Note: If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within

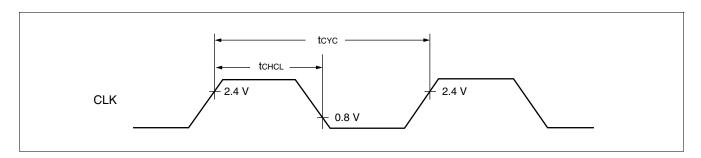
1 V/s, you can operate while using the PLL clock.



### 13.4.4 Clock Output Timing

(T\_A = 
$$-40^{\circ}C$$
 to  $+105^{\circ}C,~V_{CC}=5.0~V\pm10\%,~V_{SS}=0.0~V,~f_{CP}\leq24~MHz)$ 

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks	
				Min	Max	Uiiii	Nemarks	
Cycle time	t <sub>CYC</sub>	CLK	_	62.5	_	ns	f <sub>CP</sub> = 16 MHz	
				41.67	_	ns	f <sub>CP</sub> = 24 MHz	
CLK↑ →CLK ↓	tchcl	CLK	_	20	_	ns	f <sub>CP</sub> = 16 MHz	
				13	_	ns	f <sub>CP</sub> = 24 MHz	





## 13.4.5 Bus Timing (Read)

(T<sub>A</sub> = –40°C to +105°C, V<sub>CC</sub> = 5.0 V  $\pm$  10 %, V<sub>SS</sub> = 0.0 V, f<sub>CP</sub>  $\leq$  24 MHz)

Parameter	Sym-	Pin	Condition	Va	Unit	
Faranteter	bol	FIII	Condition	Min	Max	Ullit
ALE pulse width	t <sub>LHLL</sub>	ALE		t <sub>CP</sub> /2 - 10	_	ns
$Valid\;address\toALE\;\!\downarrowtime$	t <sub>AVLL</sub>	ALE, A21 to A16, AD15 to AD00		t <sub>CP</sub> /2 – 20	_	ns
$ALE \downarrow \to Address$ valid time	t <sub>LLAX</sub>	ALE, AD15 to AD00		t <sub>CP</sub> /2 - 15	_	ns
$Valid \; address \to \overline{RD} \; \downarrow \; time$	t <sub>AVRL</sub>	A21 to A16, AD15 to AD00, RD		t <sub>CP</sub> – 15	_	ns
Valid address → Valid data input	t <sub>AVDV</sub>	A21 to A16, AD15 to AD00		_	5 t <sub>CP</sub> /2 – 60	ns
RD pulse width	t <sub>RLRH</sub>	RD		(n*+3/2) t <sub>CP</sub> - 20	_	ns
$\overline{RD} \downarrow \to Valid$ data input	t <sub>RLDV</sub>	RD, AD15 to AD00	_	_	(n*+3/2) t <sub>CP</sub> - 50	ns
$\overline{RD} \uparrow \to Data \; hold \; time$	t <sub>RHDX</sub>	RD, AD15 to AD00		0	_	ns
$\overline{RD} \uparrow \to ALE \uparrow time$	t <sub>RHLH</sub>	RD, ALE		t <sub>CP</sub> /2 - 15	_	ns
$\overline{RD} \uparrow \to Address$ valid time	t <sub>RHAX</sub>	RD, A21 to A16		t <sub>CP</sub> /2 - 10	_	ns
Valid address → CLK ↑ time	t <sub>AVCH</sub>	A21 to A16, AD15 to AD00, CLK		t <sub>CP</sub> /2 – 16	_	ns
$\overline{RD} \downarrow \to CLK \uparrow time$	t <sub>RLCH</sub>	RD, CLK		t <sub>CP</sub> /2 – 15	_	ns
$ALE \downarrow \to \overline{RD} \downarrow time$	t <sub>LLRL</sub>	ALE, RD		t <sub>CP</sub> /2 – 15	_	ns

<sup>\*:</sup> Number of ready cycles

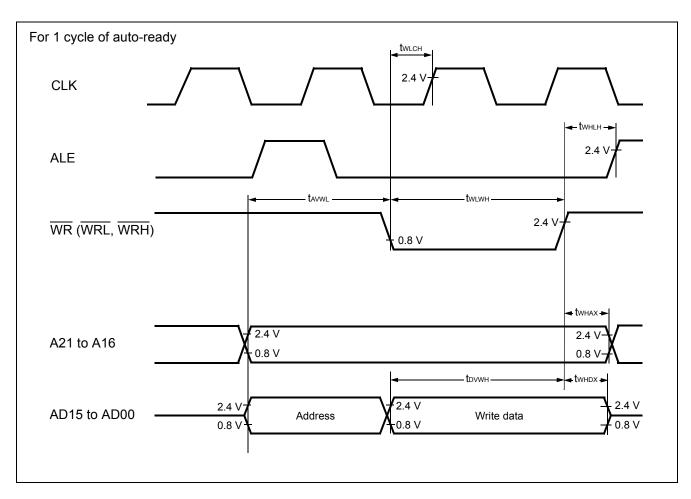


### 13.4.6 Bus Timing (Write)

(T<sub>A</sub> = -40°C to +105°C, V<sub>CC</sub> = 5.0 V  $\pm$  10 %, V<sub>SS</sub> = 0.0 V, f<sub>CP</sub>  $\leq$  24 MHz)

Parameter	Symbol	Pin	Condition	Value	Unit	
raidilletei	Symbol	FIII	Condition	Min	Min Max	
$Valid \; address \to \overline{WR} \; \downarrow time$	t <sub>AVWL</sub>	A21 to A16, AD15 to AD00, WR		t <sub>CP</sub> -15	_	ns
WR pulse width	t <sub>WLWH</sub>	WR		(n*+3/2)t <sub>CP</sub> - 20	_	ns
Valid data output $\rightarrow$ $\overline{\rm WR}$ $\uparrow$ time	t <sub>DVWH</sub>	AD15 to AD00, WR		(n*+3/2)t <sub>CP</sub> - 20	_	ns
$\overline{ m WR} \uparrow  ightarrow$ Data hold time	t <sub>WHDX</sub>	AD15 to AD00, WR	_	15	_	ns
$\overline{WR} \uparrow \to Address$ valid time	t <sub>WHAX</sub>	A21 to A16, WR		t <sub>CP</sub> /2 - 10	_	ns
$\overline{WR} \uparrow \to ALE \uparrow time$	t <sub>WHLH</sub>	WR, ALE		t <sub>CP</sub> /2 - 15	_	ns
$\overline{WR} \downarrow \to CLK \uparrow time$	t <sub>WLCH</sub>	WR, CLK		t <sub>CP</sub> /2 - 15	_	ns

<sup>\*:</sup> Number of ready cycles



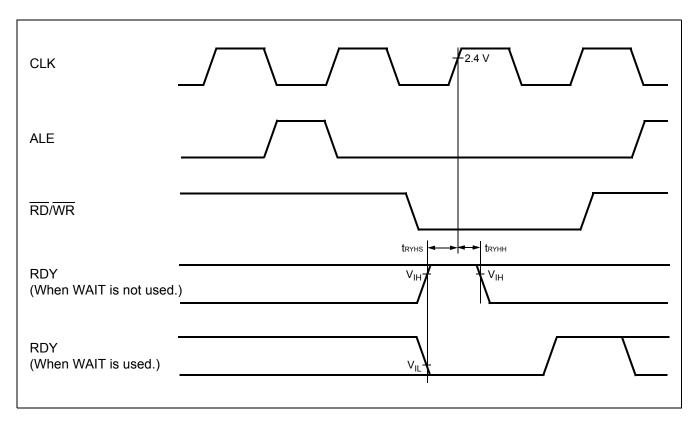


### 13.4.7 Ready Input Timing

(T<sub>A</sub> = -40°C to +105°C, V<sub>CC</sub> = 5.0 V  $\pm$  10 %, V<sub>SS</sub> = 0.0 V, f<sub>CP</sub>  $\leq$  24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks	
				Min	Max	Ullits	Remarks	
RDY set-up time	t <sub>RYHS</sub>	RDY		45	-	ns	f <sub>CP</sub> = 16 MHz	
		KDT	_	32	-	ns	f <sub>CP</sub> = 24 MHz	
RDY hold time	t <sub>RYHH</sub>	RDY		0	Ī	ns		

Note: If the RDY set-up time is insufficient, use the auto-ready function.





#### 13.4.9 LIN-UART2/3

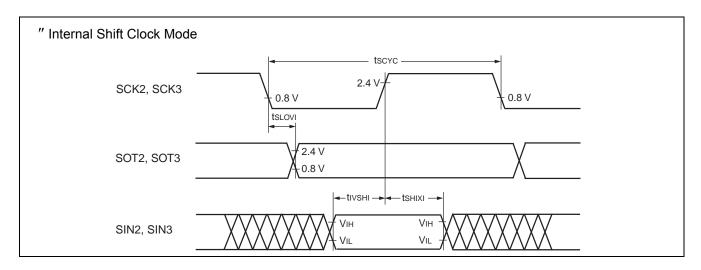
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

 $(T_A = -40^{\circ}C$  to +125°C,  $V_{CC} = 5.0~V \pm 10\%, f_{CP} \leq 24~MHz, \, V_{SS} = 0~V)$ 

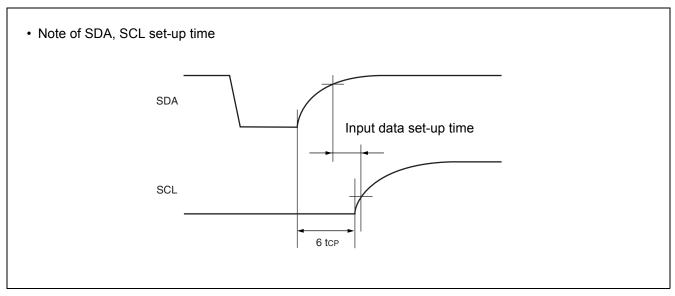
Parameter	Symbol	Pin	Condition	Value		Unit	
Parameter	Symbol	PIII	Condition	Min	Max	Offic	
Serial clock cycle time	t <sub>SCYC</sub>	SCK2, SCK3		5 t <sub>CP</sub>	_	ns	
$SCK \downarrow \to SOT$ delay time	t <sub>SLOVI</sub>	SCK2, SCK3 SOT2, SOT3	Internal shift clock	-50	+50	ns	
Valid SIN → SCK ↑	t <sub>IVSHI</sub>	SCK2, SCK3 SIN2, SIN3	mode output pins are CL = 80 pF + 1 TTL.	t <sub>CP</sub> + 80	_	ns	
SCK ↑ → Valid SIN hold time	t <sub>SHIXI</sub>	SCK2, SCK3 SIN2, SIN3		0	_	ns	
Serial clock "L" pulse width	t <sub>SHSL</sub>	SCK2, SCK3		3 t <sub>CP</sub> - t <sub>R</sub>	_	ns	
Serial clock "H" pulse width	t <sub>SLSH</sub>	SCK2, SCK3		t <sub>CP</sub> + 10	_	ns	
$SCK \downarrow \to SOT$ delay time	t <sub>SLOVE</sub>	SCK2, SCK3 SOT2, SOT3		_	2 t <sub>CP</sub> + 60	ns	
Valid SIN → SCK ↑	t <sub>IVSHE</sub>	SCK2, SCK3 SIN2, SIN3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	30	_	ns	
$SCK \uparrow \rightarrow Valid SIN hold time$	t <sub>SHIXE</sub>	SCK2, SCK3 SIN2, SIN3	35 <b>p</b> <u>2</u> .	t <sub>CP</sub> + 30	_	ns	
SCK fall time	t <sub>F</sub>	SCK2, SCK3		_	10	ns	
SCK rise time	t <sub>R</sub>	SCK2, SCK3		_	10	ns	

Notes: • AC characteristic in CLK synchronized mode.

- C<sub>L</sub> is load capacity value of pins when testing.
- t<sub>CP</sub> is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".

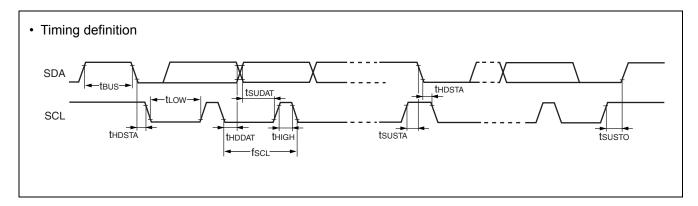






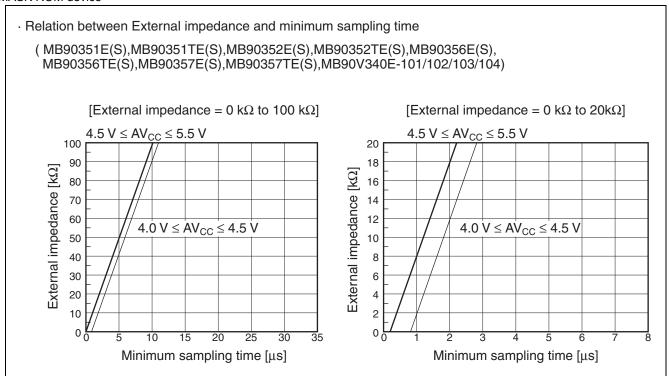
Note: The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.

Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.





### ■ MASK ROM device



### ■ About the error

Values of relative errors grow larger, as  $|AVRH - AV_{SS}|$  becomes smaller.



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