Infineon Technologies - MB90352ESPMC1-GS-163E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90352espmc1-gs-163e1

1. Product Lineup1 (Without Clock supervisor function)

■ Flash memory products

Parameter \ Part Number	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
Type	Flash memory products			
CPU	F^2MC-16LX CPU			
System clock	PLL clock multiplication circuit (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	64 Kbytes Flash memory : MB90F351E(S), MB90F351TE(S) 128 Kbytes Dual operation Flash memory (Erase/write and read can be operated at the same time) : MB90F352E(S), MB90F352TE(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No	
Clock supervisor	No			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus			
Operating temperature	−40°C to +125°C			
Package	LQFP-64			
LIN-UART	2 channels			
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	1 channel			
A/D converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit reload timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit Free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit output compare	4 channels			
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

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■ MASK ROM products/Evaluation products

Parameter \ Part Number	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-101	MB90V340E-102
Type	MASK ROM products				Evaluation products	
CPU	F^2MC-16LX CPU					
System clock	PLL clock multiplication circuit (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64 Kbytes : MB90351E(S), MB90351TE(S) 128 Kbytes : MB90352E(S), MB90352TE(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No		No	Yes
Clock supervisor	No					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40°C to +125°C				—	
Package	LQFP-64				PGA-299	
LIN-UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 kbps)	1 channel				2 channels	
A/D converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit reload timer	2 channels				4 channels	
	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU4/5/6/7.				Free-run Timer 0 corresponds to ICU0/1/2/3, OCU0/1/2/3. Free-run Timer 1 corresponds to ICU4/5/6/7, OCU4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

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Part Number / Parameter	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-101	MB90V340E-102
16-bit output compare	4 channels				8 channels	
	Signals an interrupt when 16-bit free-run Timer matches output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit input capture	6 channels				8 channels	
	Retains 16-bit free-run timer value by (rising edge, falling edge, or the both edges), signals an interrupt.					
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width×12 8-bit reload registers for H pulse width×12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN interface	1 channel				3 channels	
	Compliant with CAN standard Version 2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by “H”/“L” level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash memory	—					
Corresponding evaluation name	MB90V340E-102		MB90V340E-101		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

3. Packages and Product Correspondence

Package	MB90V340E-101 MB90V340E-102 MB90V340E-103 MB90V340E-104	MB90351E (S) , MB90351TE (S) MB90F351E (S) , MB90F351TE (S) MB90352E (S) , MB90352TE (S) MB90F352E (S) , MB90F352TE (S) MB90356E (S) , MB90356TE (S) MB90F356E (S) , MB90F356TE (S) MB90357E (S) , MB90357TE (S) MB90F357E (S) , MB90F357TE (S)
PGA-299C-A01	◯	×
FPT-64P-M23 (12.0 mm □, 0.65 mm pitch)	×	◯
FPT-64P-M24 (10.0 mm □, 0.50 mm pitch)	×	◯

◯ : Yes, × : No

Note : Refer to “Package Dimensions” for detail of each package.

Pin No.	Pin name	I/O Circuit type*	Function
54	P30	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when external bus is enabled.
	IN4		Data sample input pin for input capture ICU4
55	P31	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	$\overline{RD}$		Read strobe output pin for data bus. This function is enabled when external bus is enabled.
	IN5		Data sample input pin for input capture ICU5
56	P32	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the $\overline{WR}$/$\overline{WRL}$ pin output disabled.
	$\overline{WR}$/$\overline{WRL}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access. $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
	INT10R		External interrupt request input pin for INT10
57	P33	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode, in external bus 8-bit mode or with the $\overline{WRH}$ pin output disabled.
	$\overline{WRH}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.
58	P34	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT4		Wave form output pin for output compare OCU4
59	P35	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	$\overline{HAK}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT5		Wave form output pin for output compare OCU5
60	P36	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled.
	RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
	OUT6		Wave form output pin for output compare OCU6

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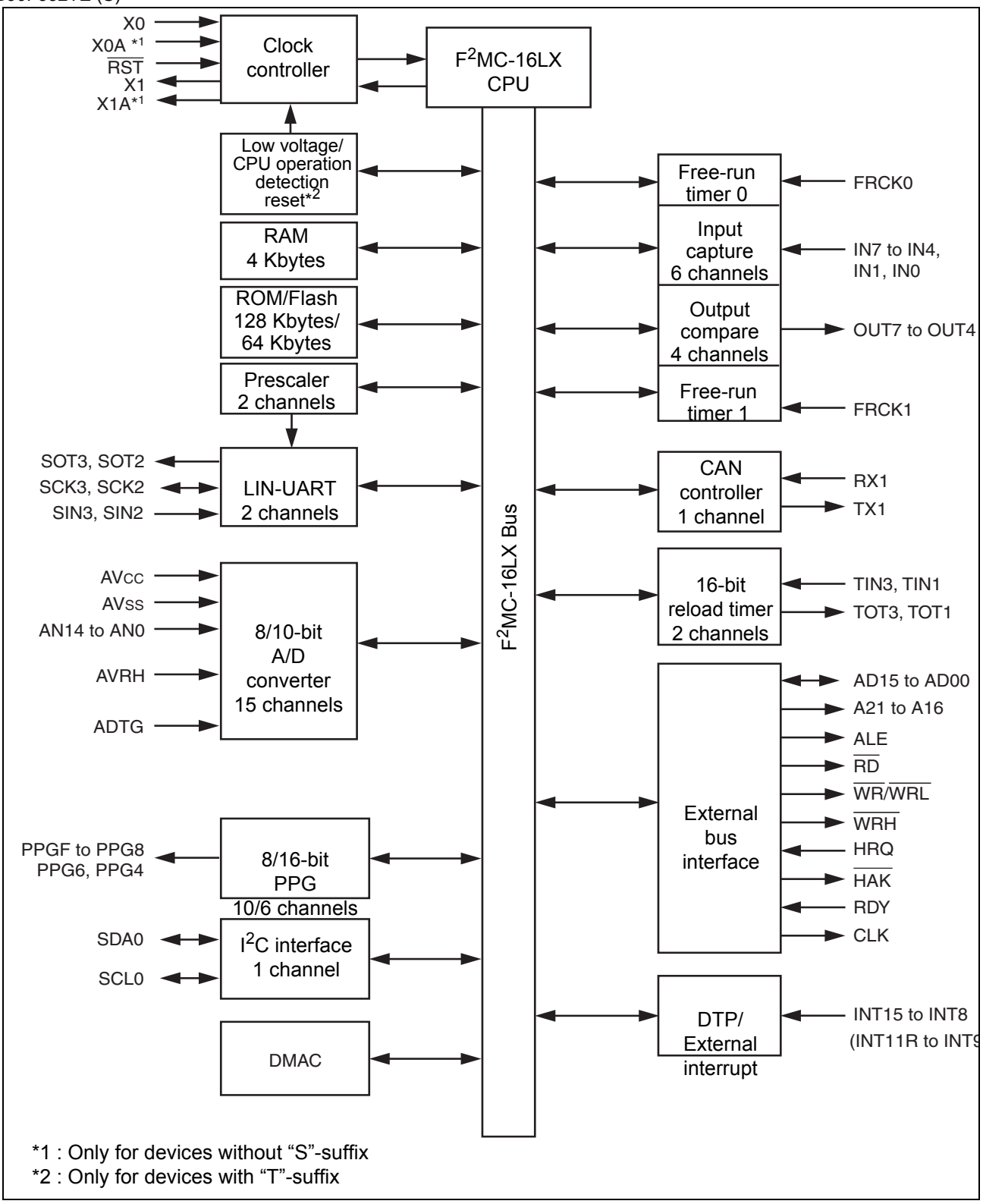
■ MB90351E (S) , MB90351TE (S) , MB90F351E (S) , MB90F351TE (S) , MB90352E (S) , MB90352TE (S) , MB90F352E (S) MB90F352TE (S)



Address	Register	Abbreviation	Access	Resource name	Initial value
000058_H to $00005B_H$	Reserved				
$00005C_H$	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	$0000XX00_B$
$00005D_H$	Output Compare Control Status Register 5	OCS5	R/W		$0XX00000_B$
$00005E_H$	Output Compare Control Status Register 6	OCS6	R/W	Output Compare 6/7	$0000XX00_B$
$00005F_H$	Output Compare Control Status Register 7	OCS7	R/W		$0XX00000_B$
000060_H	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000_B
000061_H	Timer Control Status Register 0	TMCSR0	R/W		$XXXX0000_B$
000062_H	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000_B
000063_H	Timer Control Status Register 1	TMCSR1	R/W		$XXXX0000_B$
000064_H	Timer Control Status Register 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000_B
000065_H	Timer Control Status Register 2	TMCSR2	R/W		$XXXX0000_B$
000066_H	Timer Control Status Register 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000_B
000067_H	Timer Control Status Register 3	TMCSR3	R/W		$XXXX0000_B$
000068_H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	$000XXXX0_B$
000069_H	A/D Control Status Register 1	ADCS1	R/W		$0000000X_B$
$00006A_H$	A/D Data Register 0	ADCR0	R		00000000_B
$00006B_H$	A/D Data Register 1	ADCR1	R		$XXXXXX00_B$
$00006C_H$	ADC Setting Register 0	ADSR0	R/W		00000000_B
$00006D_H$	ADC Setting Register 1	ADSR1	R/W		00000000_B
$00006E_H$	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low Voltage/CPU Operation Detection Reset	00111000_B
$00006F_H$	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	$XXXXXXX1_B$
000070_H to $00007F_H$	Reserved				
000080_H to $00008F_H$	Reserved for CAN controller 1. Refer to “CAN Controllers”				
000090_H to $00009A_H$	Reserved				

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Address CAN1	Register	Abbreviation	Access	Initial Value
$007D00_H$	Control status register	CSR	R/W, W R/W, R	$0XXXX0X1_B$ $00XXX000_B$
$007D01_H$				
$007D02_H$	Last event indicator register	LEIR	R/W	$000X0000_B$ $XXXXXXXX_B$
$007D03_H$				
$007D04_H$	Receive/transmit error counter	RTEC	R	00000000_B 00000000_B
$007D05_H$				
$007D06_H$	Bit timing register	BTR	R/W	11111111_B $X1111111_B$
$007D07_H$				
$007D08_H$	IDE register	IDER	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D09_H$				
$007D0A_H$	Transmit RTR register	TRTRR	R/W	00000000_B 00000000_B
$007D0B_H$				
$007D0C_H$	Remote frame receive waiting register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D0D_H$				
$007D0E_H$	Transmit interrupt enable register	TIER	R/W	00000000_B 00000000_B
$007D0F_H$				
$007D10_H$	Acceptance mask select register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D11_H$				
$007D12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D13_H$				
$007D14_H$	Acceptance mask register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D15_H$				
$007D16_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D17_H$				
$007D18_H$	Acceptance mask register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D19_H$				
$007D1A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D1B_H$				

List of Message Buffers (ID Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C00_H$ to $007C1F_H$	General-purpose RAM	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C20_H$	ID register 0	IDR0	R/W	$XXXXXXXX_B$
$007C21_H$				$XXXXXXXX_B$
$007C22_H$				$XXXXXXXX_B$
$007C23_H$				$XXXXXXXX_B$
$007C24_H$	ID register 1	IDR1	R/W	$XXXXXXXX_B$
$007C25_H$				$XXXXXXXX_B$
$007C26_H$				$XXXXXXXX_B$
$007C27_H$				$XXXXXXXX_B$
$007C28_H$	ID register 2	IDR2	R/W	$XXXXXXXX_B$
$007C29_H$				$XXXXXXXX_B$
$007C2A_H$				$XXXXXXXX_B$
$007C2B_H$				$XXXXXXXX_B$
$007C2C_H$	ID register 3	IDR3	R/W	$XXXXXXXX_B$
$007C2D_H$				$XXXXXXXX_B$
$007C2E_H$				$XXXXXXXX_B$
$007C2F_H$				$XXXXXXXX_B$
$007C30_H$	ID register 4	IDR4	R/W	$XXXXXXXX_B$
$007C31_H$				$XXXXXXXX_B$
$007C32_H$				$XXXXXXXX_B$
$007C33_H$				$XXXXXXXX_B$
$007C34_H$	ID register 5	IDR5	R/W	$XXXXXXXX_B$
$007C35_H$				$XXXXXXXX_B$
$007C36_H$				$XXXXXXXX_B$
$007C37_H$				$XXXXXXXX_B$
$007C38_H$	ID register 6	IDR6	R/W	$XXXXXXXX_B$
$007C39_H$				$XXXXXXXX_B$
$007C3A_H$				$XXXXXXXX_B$
$007C3B_H$				$XXXXXXXX_B$
$007C3C_H$	ID register 7	IDR7	R/W	$XXXXXXXX_B$
$007C3D_H$				$XXXXXXXX_B$
$007C3E_H$				$XXXXXXXX_B$
$007C3F_H$				$XXXXXXXX_B$

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Address CAN1	Register	Abbreviation	Access	Initial Value
$007C40_H$	ID register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C41_H$				
$007C42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C43_H$				
$007C44_H$	ID register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C45_H$				
$007C46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C47_H$				
$007C48_H$	ID register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C49_H$				
$007C4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C4B_H$				
$007C4C_H$	ID register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C4D_H$				
$007C4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C4F_H$				
$007C50_H$	ID register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C51_H$				
$007C52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C53_H$				
$007C54_H$	ID register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C55_H$				
$007C56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C57_H$				
$007C58_H$	ID register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C59_H$				
$007C5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C5B_H$				
$007C5C_H$	ID register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C5D_H$				
$007C5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C5F_H$				

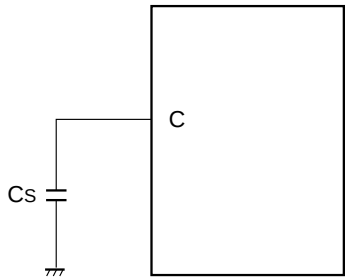
13.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	−40	—	+125	°C	*

* : If used exceeding T_A = +105°C, be sure to contact Cypress for reliability limitations.

″ C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

13.4 AC Characteristics

13.4.1 Clock Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	1/2 (at PLL stop) When using an oscillation circuit
			4	—	16	MHz	1 multiplied PLL When using an oscillation circuit
			4	—	12	MHz	2 multiplied PLL When using an oscillation circuit
			4	—	8	MHz	3 multiplied PLL When using an oscillation circuit
			4	—	6	MHz	4 multiplied PLL When using an oscillation circuit
			—	—	4	MHz	6 multiplied PLL When using an oscillation circuit
		X0	3	—	24	MHz	1/2 (at PLL stop), When using an external clock
			4	—	24	MHz	1 multiplied PLL When using an external clock
			4	—	12	MHz	2 multiplied PLL When using an external clock
			4	—	8	MHz	3 multiplied PLL When using an external clock
			4	—	6	MHz	4 multiplied PLL When using an external clock
			—	—	4	MHz	6 multiplied PLL When using an external clock
	fCL	X0A, X1A	—	32.768	100	kHz	When using sub clock
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0	41.67	—	333	ns	When using an external clock
	tCYLL	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio should be about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock

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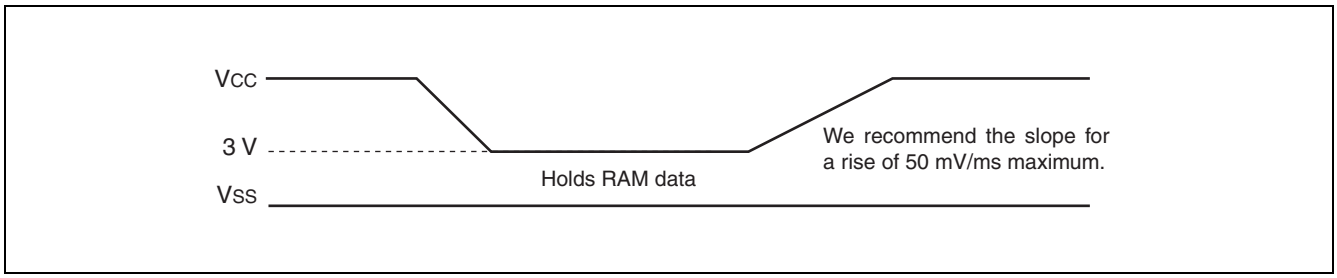
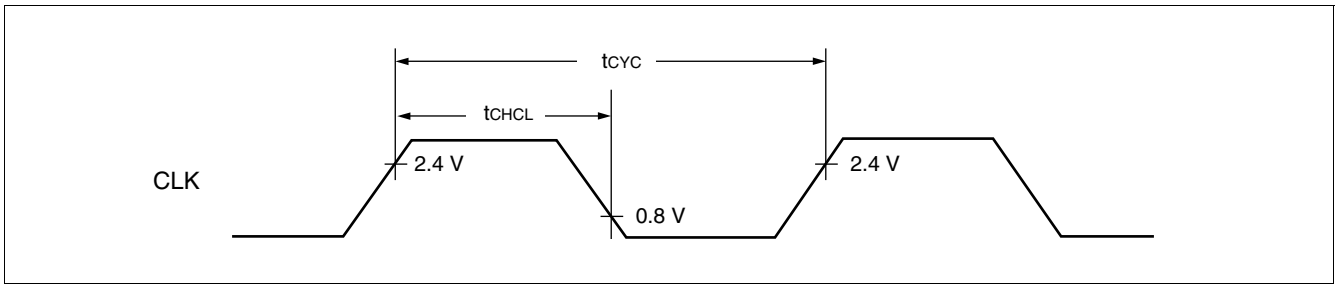
Note : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within
1 V/s, you can operate while using the PLL clock.



13.4.4 Clock Output Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	f_{CP} = 16 MHz
				41.67	—	ns	f_{CP} = 24 MHz
CLK↑ →CLK ↓	t_{CHCL}	CLK	—	20	—	ns	f_{CP} = 16 MHz
				13	—	ns	f_{CP} = 24 MHz



13.4.5 Bus Timing (Read)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, $f_{CP} \leq$ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE	–	$t_{CP}/2 - 10$	–	ns
Valid address → ALE ↓ time	t_{AVLL}	ALE, A21 to A16, AD15 to AD00		$t_{CP}/2 - 20$	–	ns
ALE ↓ → Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	–	ns
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	A21 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	–	ns
Valid address → Valid data input	t_{AVDV}	A21 to A16, AD15 to AD00		–	$5\ t_{CP}/2 - 60$	ns
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$(n^*+3/2)\ t_{CP} - 20$	–	ns
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		–	$(n^*+3/2)\ t_{CP} - 50$	ns
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	–	ns
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	–	ns
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A21 to A16		$t_{CP}/2 - 10$	–	ns
Valid address → CLK ↑ time	t_{AVCH}	A21 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	–	ns
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	–	ns
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	–	ns

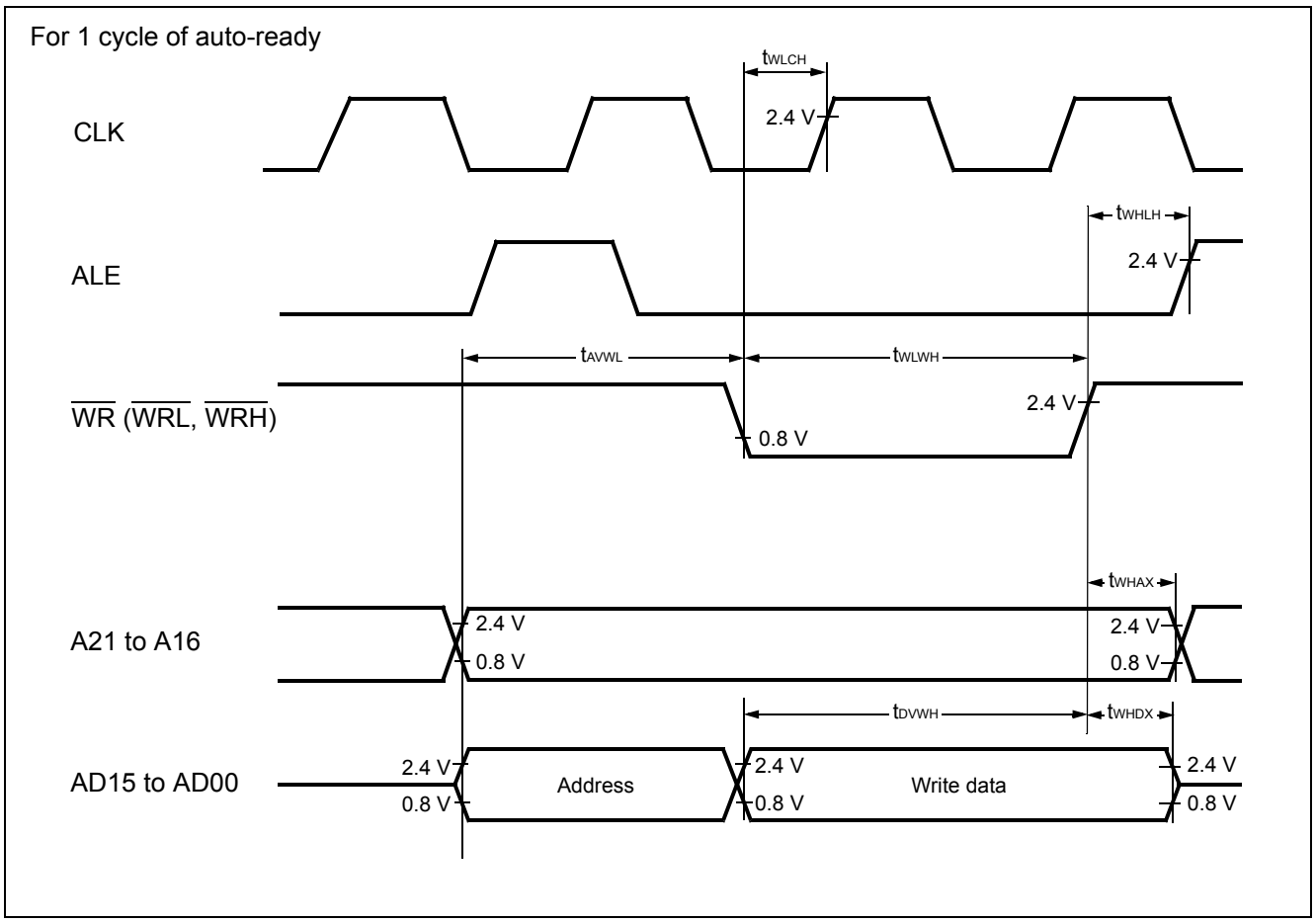
* : Number of ready cycles

13.4.6 Bus Timing (Write)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A21 to A16, AD15 to AD00, $\overline{WR}$	–	t_{CP}–15	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		(n*+3/2)t_{CP} – 20	–	ns
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		(n*+3/2)t_{CP} – 20	–	ns
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	–	ns
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A21 to A16, $\overline{WR}$		t_{CP}/2 – 10	–	ns
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	–	ns
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 15	–	ns

* : Number of ready cycles

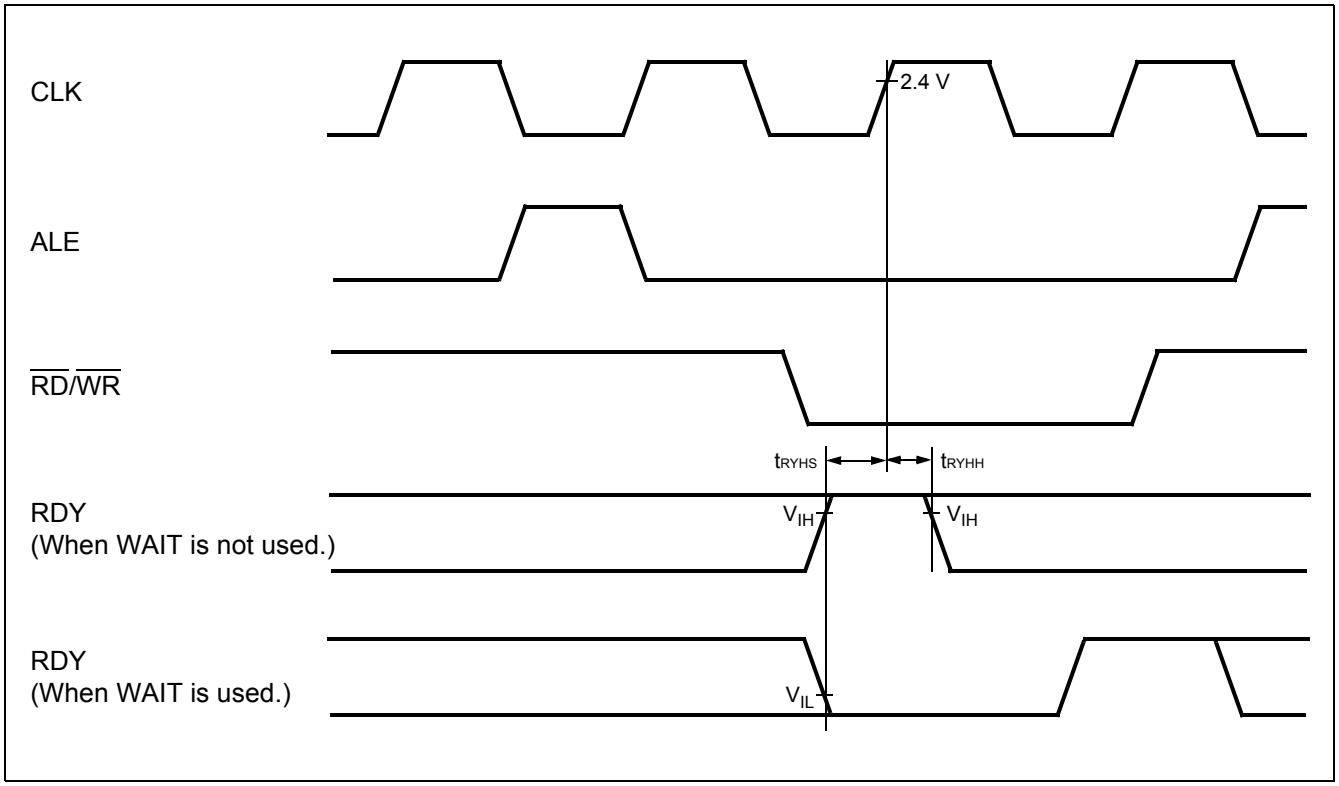


13.4.7 Ready Input Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
RDY set-up time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY set-up time is insufficient, use the auto-ready function.



13.4.9 LIN-UART2/3

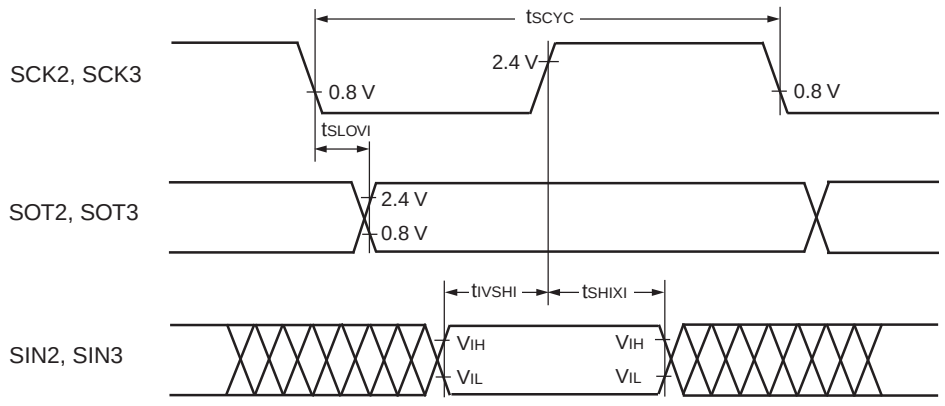
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

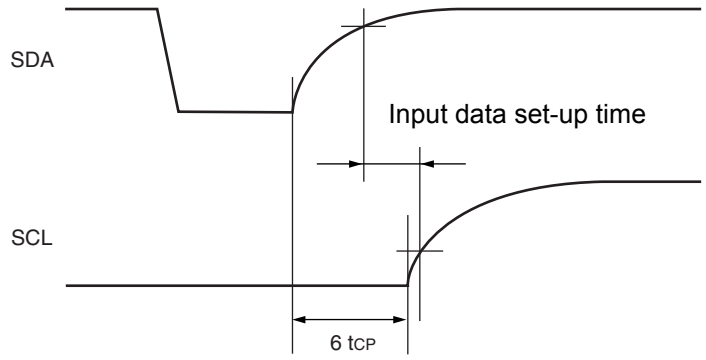
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal shift clock mode output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2, SCK3 SOT2, SOT3		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK2, SCK3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK2, SCK3		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK2, SCK3 SOT2, SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK2, SCK3 SIN2, SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK2, SCK3		—	10	ns
SCK rise time	t_R	SCK2, SCK3		—	10	ns

Notes :
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

″ Internal Shift Clock Mode

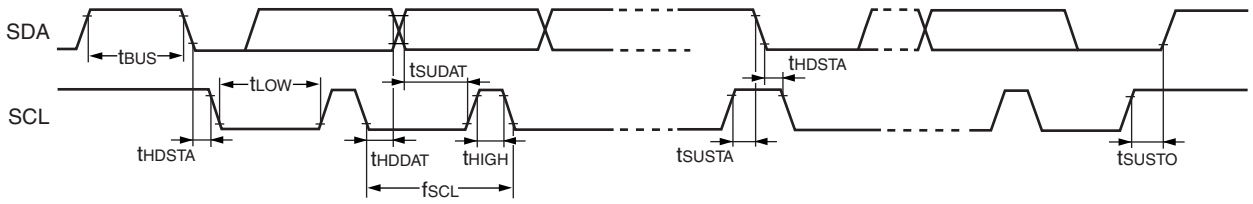


• Note of SDA, SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition

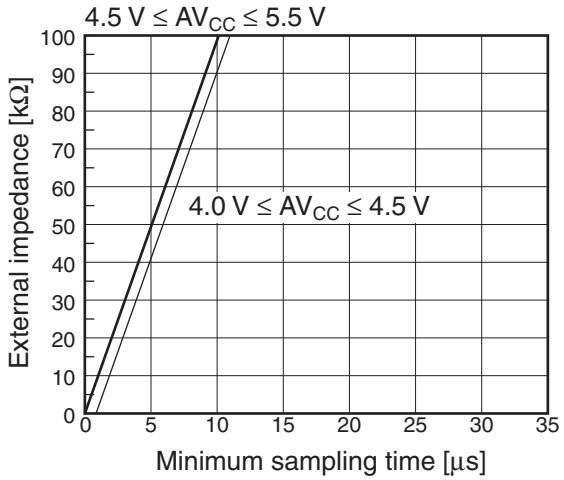


■ MASK ROM device

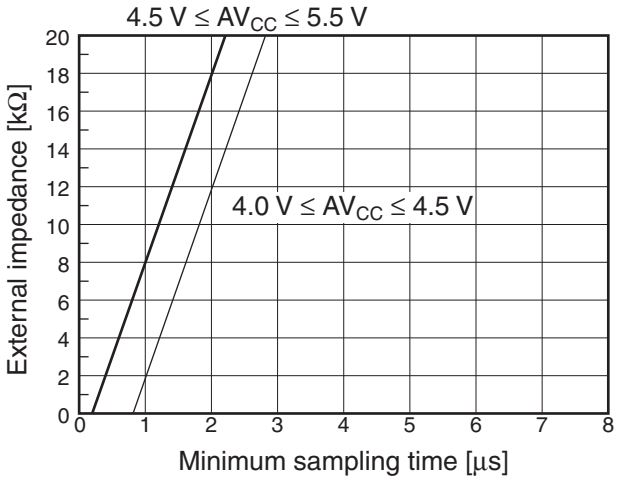
· Relation between External impedance and minimum sampling time

(MB90351E(S),MB90351TE(S),MB90352E(S),MB90352TE(S),MB90356E(S), MB90356TE(S),MB90357E(S),MB90357TE(S),MB90V340E-101/102/103/104)

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20kΩ]



■ About the error

Values of relative errors grow larger, as |AVRH − AV_{SS}| becomes smaller.

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