Infineon Technologies - MB90F351ESPMC1-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f351espmc1-gse1

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Parameter \ Part Number	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
16-bit Input capture	6 channels			
	Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge) , signals an interrupt.			
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width×12			
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN interface	1 channel			
	Compliant with CAN standard Version2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External interrupt	8 channels			
	Can be used rising edge, falling edge, starting up by “H”/“L” level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.			
D/A converter	—			
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F352E(S) and MB90F352TE(S) only)			
Corresponding evaluation name	MB90V340E-102		MB90V340E-101	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

Pin No.	Pin name	I/O Circuit type*	Function
24 to 31	P00 to P07	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD00 to AD07		Input/output pins of external address data bus lower 8 bits. This function is enabled when the external bus is enabled.
	INT8 to INT15		External interrupt request input pins for INT8 to INT15
32	P10	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD08		Input/output pin for external bus address data bus bit 8. This function is enabled when external bus is enabled.
	TIN1		Event input pin for reload timer1
33	P11	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD09		Input/output pin for external bus address data bus bit 9. This function is enabled when external bus is enabled.
	TOT1		Output pin for reload timer1
34	P12	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD10		Input/output pin for external bus address data bus bit 10. This function is enabled when external bus is enabled.
	SIN3		Serial data input pin for UART3
	INT11R		External interrupt request input pin for INT11
35	P13	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD11		Input/output pin for external bus address data bus bit 11. This function is enabled when external bus is enabled.
	SOT3		Serial data output pin for UART3
36	P14	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD12		Input/output pin for external bus address data bus bit 12. This function is enabled when external bus is enabled.
	SCK3		Clock input/output pin for UART3
37	P15	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD13		Input/output pin for external bus address data bus bit 13. This function is enabled when external bus is enabled.
38	P16	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD14		Input/output pin for external bus address data bus bit 14. This function is enabled when external bus is enabled.

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Pin No.	Pin name	I/O Circuit type*	Function
54	P30	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when external bus is enabled.
	IN4		Data sample input pin for input capture ICU4
55	P31	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	$\overline{RD}$		Read strobe output pin for data bus. This function is enabled when external bus is enabled.
	IN5		Data sample input pin for input capture ICU5
56	P32	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the $\overline{WR}$/$\overline{WRL}$ pin output disabled.
	$\overline{WR}$/$\overline{WRL}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access. $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
	INT10R		External interrupt request input pin for INT10
57	P33	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode, in external bus 8-bit mode or with the $\overline{WRH}$ pin output disabled.
	$\overline{WRH}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.
58	P34	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT4		Wave form output pin for output compare OCU4
59	P35	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	$\overline{HAK}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT5		Wave form output pin for output compare OCU5
60	P36	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled.
	RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
	OUT6		Wave form output pin for output compare OCU6

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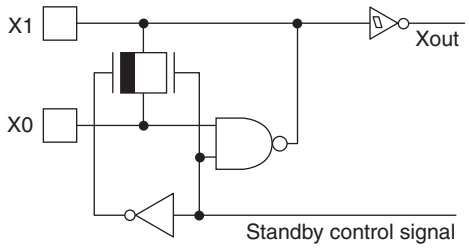
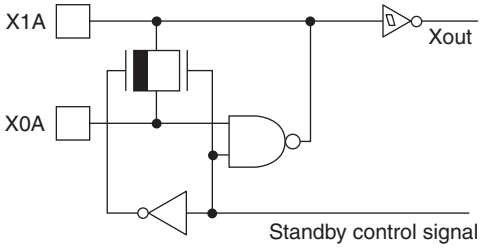
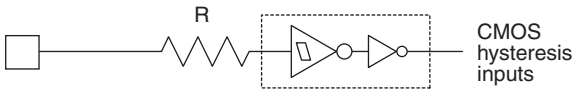
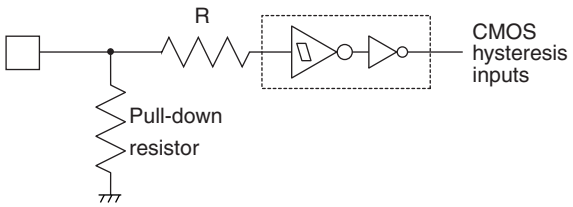
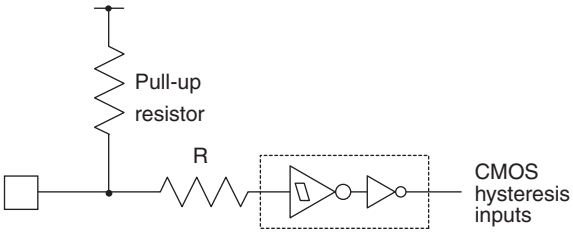
6. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM device CMOS hysteresis input pin ■ Flash memory device CMOS input pin
D		■ MASK ROM device CMOS hysteresis input pin Pull-down resistor value: approx. 50 kΩ ■ Flash memory device CMOS input pin No Pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

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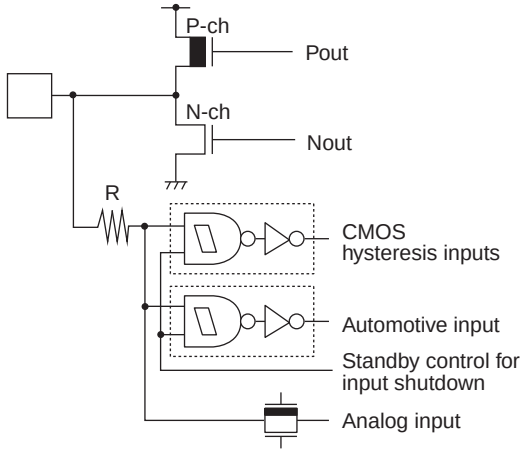
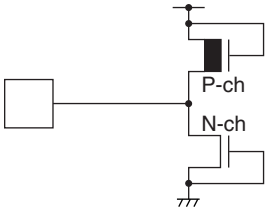
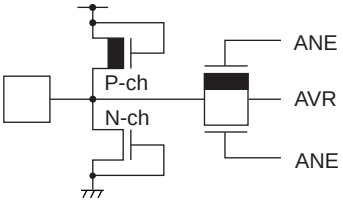
Type	Circuit	Remarks
I		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ Analog input for A/D converter
K		Protection circuit for power supply input
L		■ With the protection circuit of A/D converter reference voltage power input pin ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH.

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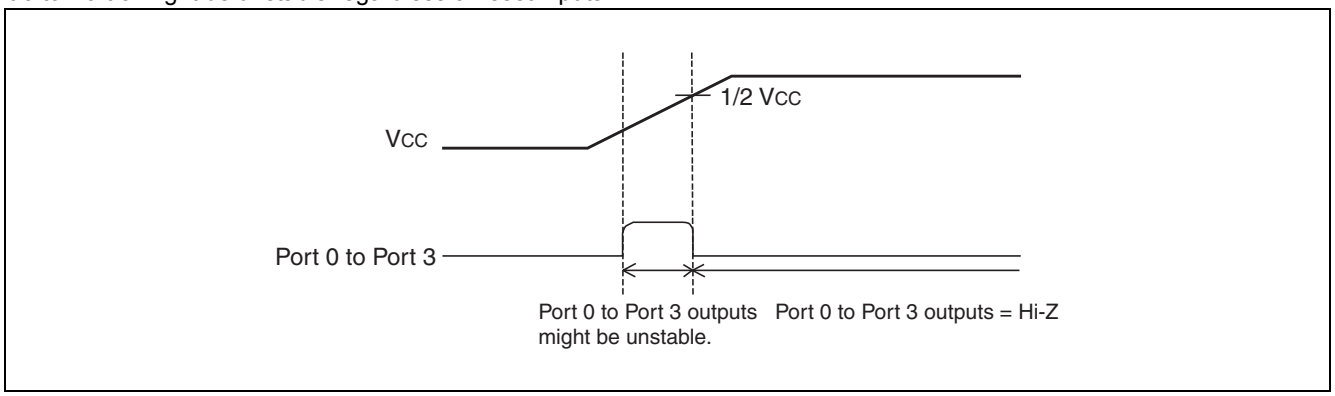
13. Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

14. Port 0 to port 3 output during power-on (External-bus mode)

As shown below, when power is turned on in external-bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable regardless of reset inputs.



15. Setting using CAN function

To use CAN function, please set “1” to DIRECT bit of CAN direct mode register (CDMR).

16. Flash security function

The security byte is located in the area of the Flash memory. If protection code 01_H is written in the security byte, the Flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Please refer to following table for the address of the security byte.

Product name	Flash memory size	Address for security bit
MB90F352E(S) MB90F352TE(S) MB90F357E(S) MB90F357TE(S)	Embedded 1 Mbit Flash memory	$FE0001_H$

17. Operation with T_A = +105°C or more

If used exceeding $T_A = +105°C$, please contact Cypress sales representatives for reliability limitations.

18. Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.
The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

(1) Low voltage detection reset circuit

Detection voltage
4.0 V ± 0.3 V

When a low voltage condition is detected, the low voltage detection flag (LVRC : LVRF) is set to “1” and an internal reset signal is output.
Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.

10. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
000000_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
000001_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
000002_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
000003_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
000004_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
000005_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
000006_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
000007_H to $00000A_H$	Reserved				
$00000B_H$	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111_B
$00000C_H$	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111_B
$00000D_H$	Reserved				
$00000E_H$	Input Level Select Register 0	ILSR0	R/W	Ports	00000000_B
$00000F_H$	Input Level Select Register 1	ILSR1	R/W	Ports	00000000_B
000010_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
000011_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
000012_H	Port 2 Direction Register	DDR2	R/W	Port 2	$XX000000_B$
000013_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
000014_H	Port 4 Direction Register	DDR4	R/W	Port 4	$XX000000_B$
000015_H	Port 5 Direction Register	DDR5	R/W	Port 5	$X0000000_B$
000016_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
000017_H to 000019_H	Reserved				
$00001A_H$	SIN input Level Setting Register	DDRA	W	UART2, UART3	$X00XXXXX_B$
$00001B_H$	Reserved				
$00001C_H$	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000_B
$00001D_H$	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000_B
$00001E_H$	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000_B
$00001F_H$	Port 3 Pull-up Control Register	PUCR3	R/W	Port 3	00000000_B
000020_H to 000037_H	Reserved				

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Address	Register	Abbreviation	Access	Resource name	Initial value
000058_H to $00005B_H$	Reserved				
$00005C_H$	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	$0000XX00_B$
$00005D_H$	Output Compare Control Status Register 5	OCS5	R/W		$0XX00000_B$
$00005E_H$	Output Compare Control Status Register 6	OCS6	R/W	Output Compare 6/7	$0000XX00_B$
$00005F_H$	Output Compare Control Status Register 7	OCS7	R/W		$0XX00000_B$
000060_H	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000_B
000061_H	Timer Control Status Register 0	TMCSR0	R/W		$XXXX0000_B$
000062_H	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000_B
000063_H	Timer Control Status Register 1	TMCSR1	R/W		$XXXX0000_B$
000064_H	Timer Control Status Register 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000_B
000065_H	Timer Control Status Register 2	TMCSR2	R/W		$XXXX0000_B$
000066_H	Timer Control Status Register 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000_B
000067_H	Timer Control Status Register 3	TMCSR3	R/W		$XXXX0000_B$
000068_H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	$000XXXX0_B$
000069_H	A/D Control Status Register 1	ADCS1	R/W		$0000000X_B$
$00006A_H$	A/D Data Register 0	ADCR0	R		00000000_B
$00006B_H$	A/D Data Register 1	ADCR1	R		$XXXXXX00_B$
$00006C_H$	ADC Setting Register 0	ADSR0	R/W		00000000_B
$00006D_H$	ADC Setting Register 1	ADSR1	R/W		00000000_B
$00006E_H$	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low Voltage/CPU Operation Detection Reset	00111000_B
$00006F_H$	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	$XXXXXXX1_B$
000070_H to $00007F_H$	Reserved				
000080_H to $00008F_H$	Reserved for CAN controller 1. Refer to “CAN Controllers”				
000090_H to $00009A_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$0000B9_H$	Interrupt Control Register 09	ICR09	W,R/W	Interrupt Control	00000111_B
$0000BA_H$	Interrupt Control Register 10	ICR10	W,R/W		00000111_B
$0000BB_H$	Interrupt Control Register 11	ICR11	W,R/W		00000111_B
$0000BC_H$	Interrupt Control Register 12	ICR12	W,R/W		00000111_B
$0000BD_H$	Interrupt Control Register 13	ICR13	W,R/W		00000111_B
$0000BE_H$	Interrupt Control Register 14	ICR14	W,R/W		00000111_B
$0000BF_H$	Interrupt Control Register 15	ICR15	W,R/W		00000111_B
$0000C0_H$ to $0000C9_H$	Reserved				
$0000CA_H$	External Interrupt Enable Register 1	ENIR1	R/W	External Interrupt 1	00000000_B
$0000CB_H$	External Interrupt Source Register 1	EIRR1	R/W		$XXXXXXXX_B$
$0000CC_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000_B
$0000CD_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000_B
$0000CE_H$	External Interrupt Source Select Register	EISSR	R/W		00000000_B
$0000CF_H$	PLL/Sub clock Control register	PSCCR	W	PLL	$XXXX0000_B$
$0000D0_H$	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	$XXXXXXXX_B$
$0000D1_H$	DMA Buffer Address Pointer M Register	BAPM	R/W		$XXXXXXXX_B$
$0000D2_H$	DMA Buffer Address Pointer H Register	BAPH	R/W		$XXXXXXXX_B$
$0000D3_H$	DMA Control Register	DMACS	R/W		$XXXXXXXX_B$
$0000D4_H$	I/O Register Address Pointer L Register	IOAL	R/W		$XXXXXXXX_B$
$0000D5_H$	I/O Register Address Pointer H Register	IOAH	R/W		$XXXXXXXX_B$
$0000D6_H$	Data Counter L Register	DCTL	R/W		$XXXXXXXX_B$
$0000D7_H$	Data Counter H Register	DCTH	R/W		$XXXXXXXX_B$
$0000D8_H$	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000_B
$0000D9_H$	Serial Control Register 2	SCR2	W,R/W		00000000_B
$0000DA_H$	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000_B
$0000DB_H$	Serial Status Register 2	SSR2	R,R/W		00001000_B
$0000DC_H$	Extended Communication Control Register 2	ECCR2	R,W, R/W		$000000XX_B$
$0000DD_H$	Extended Status/Control Register 2	ESCR2	R/W		00000100_B
$0000DE_H$	Baud Rate Generator Register 20	BGR20	R/W		00000000_B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$0000DF_H$	Baud Rate Generator Register 21	BGR21	R/W	UART2	00000000_B
$0000E0_H$ to $0000EF_H$	Reserved				
$0000F0_H$ to $0000FF_H$	External area				
007900_H to 007907_H	Reserved				
007908_H	Reload Register L4	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	$XXXXXXXX_B$
007909_H	Reload Register H4	PRLH4	R/W		$XXXXXXXX_B$
$00790A_H$	Reload Register L5	PRLL5	R/W		$XXXXXXXX_B$
$00790B_H$	Reload Register H5	PRLH5	R/W		$XXXXXXXX_B$
$00790C_H$	Reload Register L6	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	$XXXXXXXX_B$
$00790D_H$	Reload Register H6	PRLH6	R/W		$XXXXXXXX_B$
$00790E_H$	Reload Register L7	PRLL7	R/W		$XXXXXXXX_B$
$00790F_H$	Reload Register H7	PRLH7	R/W		$XXXXXXXX_B$
007910_H	Reload Register L8	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	$XXXXXXXX_B$
007911_H	Reload Register H8	PRLH8	R/W		$XXXXXXXX_B$
007912_H	Reload Register L9	PRLL9	R/W		$XXXXXXXX_B$
007913_H	Reload Register H9	PRLH9	R/W		$XXXXXXXX_B$
007914_H	Reload Register LA	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	$XXXXXXXX_B$
007915_H	Reload Register HA	PRLHA	R/W		$XXXXXXXX_B$
007916_H	Reload Register LB	PRLLB	R/W		$XXXXXXXX_B$
007917_H	Reload Register HB	PRLHB	R/W		$XXXXXXXX_B$
007918_H	Reload Register LC	PRLLC	R/W	16-bit Programmable Pulse Generator C/D	$XXXXXXXX_B$
007919_H	Reload Register HC	PRLHC	R/W		$XXXXXXXX_B$
$00791A_H$	Reload Register LD	PRLLD	R/W		$XXXXXXXX_B$
$00791B_H$	Reload Register HD	PRLHD	R/W		$XXXXXXXX_B$
$00791C_H$	Reload Register LE	PRLLE	R/W	16-bit Programmable Pulse Generator E/F	$XXXXXXXX_B$
$00791D_H$	Reload Register HE	PRLHE	R/W		$XXXXXXXX_B$
$00791E_H$	Reload Register LF	PRLLF	R/W		$XXXXXXXX_B$
$00791F_H$	Reload Register HF	PRLHF	R/W		$XXXXXXXX_B$
007920_H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	$XXXXXXXX_B$
007921_H	Input Capture Register 0	IPCP0	R		$XXXXXXXX_B$
007922_H	Input Capture Register 1	IPCP1	R		$XXXXXXXX_B$
007923_H	Input Capture Register 1	IPCP1	R		$XXXXXXXX_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007950_H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000_B
007951_H	Serial Control Register 3	SCR3	W, R/W		00000000_B
007952_H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000_B
007953_H	Serial Status Register 3	SSR3	R,R/W		00001000_B
007954_H	Extended Communication Control Register 3	ECCR3	R,W, R/W		$000000XX_B$
007955_H	Extended Status Control Register 3	ESCR3	R/W		00000100_B
007956_H	Baud Rate Generator Register 30	BGR30	R/W		00000000_B
007957_H	Baud Rate Generator Register 31	BGR31	R/W		00000000_B
007958_H, 007959_H	Reserved				
007960_H	Clock supervisor Control Register	CSVCR	R, R/W	Clock Supervisor	00011100_B
007961_H to $00796D_H$	Reserved				
$00796E_H$	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	$XXXXXXX0_B$
$00796F_H$	Reserved				
007970_H	I^2C Bus Status Register 0	IBSR0	R	I^2C Interface 0	00000000_B
007971_H	I^2C Bus Control Register 0	IBCR0	W,R/W		00000000_B
007972_H	I^2C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000_B
007973_H		ITBAH0	R/W		00000000_B
007974_H	I^2C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111_B
007975_H		ITMKH0	R/W		00111111_B
007976_H	I^2C 7-bit Slave Address Register 0	ISBA0	R/W		00000000_B
007977_H	I^2C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111_B
007978_H	I^2C data register 0	IDAR0	R/W		00000000_B
007979_H, $00797A_H$	Reserved				
$00797B_H$	I^2C Clock Control Register 0	ICCR0	R/W	I^2C Interface 0	00011111_B
$00797C_H$ to $0079A1_H$	Reserved				
$0079A2_H$	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000_B
$0079A3_H$	Flash Write Control Register 1	FWR1	R/W		00000000_B
$0079A4_H$	Sector Change Setting Register 0	SSR0	R/W		$00XXXXX0_B$
$0079A5_H$ to $0079C1_H$	Reserved				
$0079C2_H$	Clock modulator Control Register	CMCR	R, R/W	Clock Modulator	$0001X000_B$

(Continued)

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Address CAN1	Register	Abbreviation	Access	Initial Value
$007D00_H$	Control status register	CSR	R/W, W R/W, R	$0XXXX0X1_B$ $00XXX000_B$
$007D01_H$				
$007D02_H$	Last event indicator register	LEIR	R/W	$000X0000_B$ $XXXXXXXX_B$
$007D03_H$				
$007D04_H$	Receive/transmit error counter	RTEC	R	00000000_B 00000000_B
$007D05_H$				
$007D06_H$	Bit timing register	BTR	R/W	11111111_B $X1111111_B$
$007D07_H$				
$007D08_H$	IDE register	IDER	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D09_H$				
$007D0A_H$	Transmit RTR register	TRTRR	R/W	00000000_B 00000000_B
$007D0B_H$				
$007D0C_H$	Remote frame receive waiting register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D0D_H$				
$007D0E_H$	Transmit interrupt enable register	TIER	R/W	00000000_B 00000000_B
$007D0F_H$				
$007D10_H$	Acceptance mask select register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D11_H$				
$007D12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D13_H$				
$007D14_H$	Acceptance mask register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D15_H$				
$007D16_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D17_H$				
$007D18_H$	Acceptance mask register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D19_H$				
$007D1A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D1B_H$				

List of Message Buffers (ID Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C00_H$ to $007C1F_H$	General-purpose RAM	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C20_H$	ID register 0	IDR0	R/W	$XXXXXXXX_B$
$007C21_H$				$XXXXXXXX_B$
$007C22_H$				$XXXXXXXX_B$
$007C23_H$				$XXXXXXXX_B$
$007C24_H$	ID register 1	IDR1	R/W	$XXXXXXXX_B$
$007C25_H$				$XXXXXXXX_B$
$007C26_H$				$XXXXXXXX_B$
$007C27_H$				$XXXXXXXX_B$
$007C28_H$	ID register 2	IDR2	R/W	$XXXXXXXX_B$
$007C29_H$				$XXXXXXXX_B$
$007C2A_H$				$XXXXXXXX_B$
$007C2B_H$				$XXXXXXXX_B$
$007C2C_H$	ID register 3	IDR3	R/W	$XXXXXXXX_B$
$007C2D_H$				$XXXXXXXX_B$
$007C2E_H$				$XXXXXXXX_B$
$007C2F_H$				$XXXXXXXX_B$
$007C30_H$	ID register 4	IDR4	R/W	$XXXXXXXX_B$
$007C31_H$				$XXXXXXXX_B$
$007C32_H$				$XXXXXXXX_B$
$007C33_H$				$XXXXXXXX_B$
$007C34_H$	ID register 5	IDR5	R/W	$XXXXXXXX_B$
$007C35_H$				$XXXXXXXX_B$
$007C36_H$				$XXXXXXXX_B$
$007C37_H$				$XXXXXXXX_B$
$007C38_H$	ID register 6	IDR6	R/W	$XXXXXXXX_B$
$007C39_H$				$XXXXXXXX_B$
$007C3A_H$				$XXXXXXXX_B$
$007C3B_H$				$XXXXXXXX_B$
$007C3C_H$	ID register 7	IDR7	R/W	$XXXXXXXX_B$
$007C3D_H$				$XXXXXXXX_B$
$007C3E_H$				$XXXXXXXX_B$
$007C3F_H$				$XXXXXXXX_B$

(Continued)

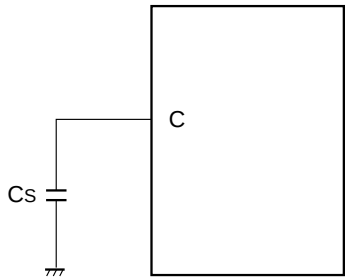
13.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	−40	—	+125	°C	*

* : If used exceeding T_A = +105°C, be sure to contact Cypress for reliability limitations.

″ C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCL}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub clock operation T_A = +25°C	—	70	140	µA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub clock operation T_A = +25°C	—	100	200	µA	MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T_A = +25°C	—	100	200	µA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub clock operation T_A = +25°C	—	120	240	µA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub clock operation T_A = +25°C	—	150	300	µA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T_A = +25°C	—	150	300	µA	MB90356TES MB90F356TES MB90357TES MB90F357TES

(Continued)

13.4 AC Characteristics

13.4.1 Clock Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	1/2 (at PLL stop) When using an oscillation circuit
			4	—	16	MHz	1 multiplied PLL When using an oscillation circuit
			4	—	12	MHz	2 multiplied PLL When using an oscillation circuit
			4	—	8	MHz	3 multiplied PLL When using an oscillation circuit
			4	—	6	MHz	4 multiplied PLL When using an oscillation circuit
			—	—	4	MHz	6 multiplied PLL When using an oscillation circuit
		X0	3	—	24	MHz	1/2 (at PLL stop), When using an external clock
			4	—	24	MHz	1 multiplied PLL When using an external clock
			4	—	12	MHz	2 multiplied PLL When using an external clock
			4	—	8	MHz	3 multiplied PLL When using an external clock
			4	—	6	MHz	4 multiplied PLL When using an external clock
			—	—	4	MHz	6 multiplied PLL When using an external clock
	fCL	X0A, X1A	—	32.768	100	kHz	When using sub clock
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0	41.67	—	333	ns	When using an external clock
	tCYLL	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio should be about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock

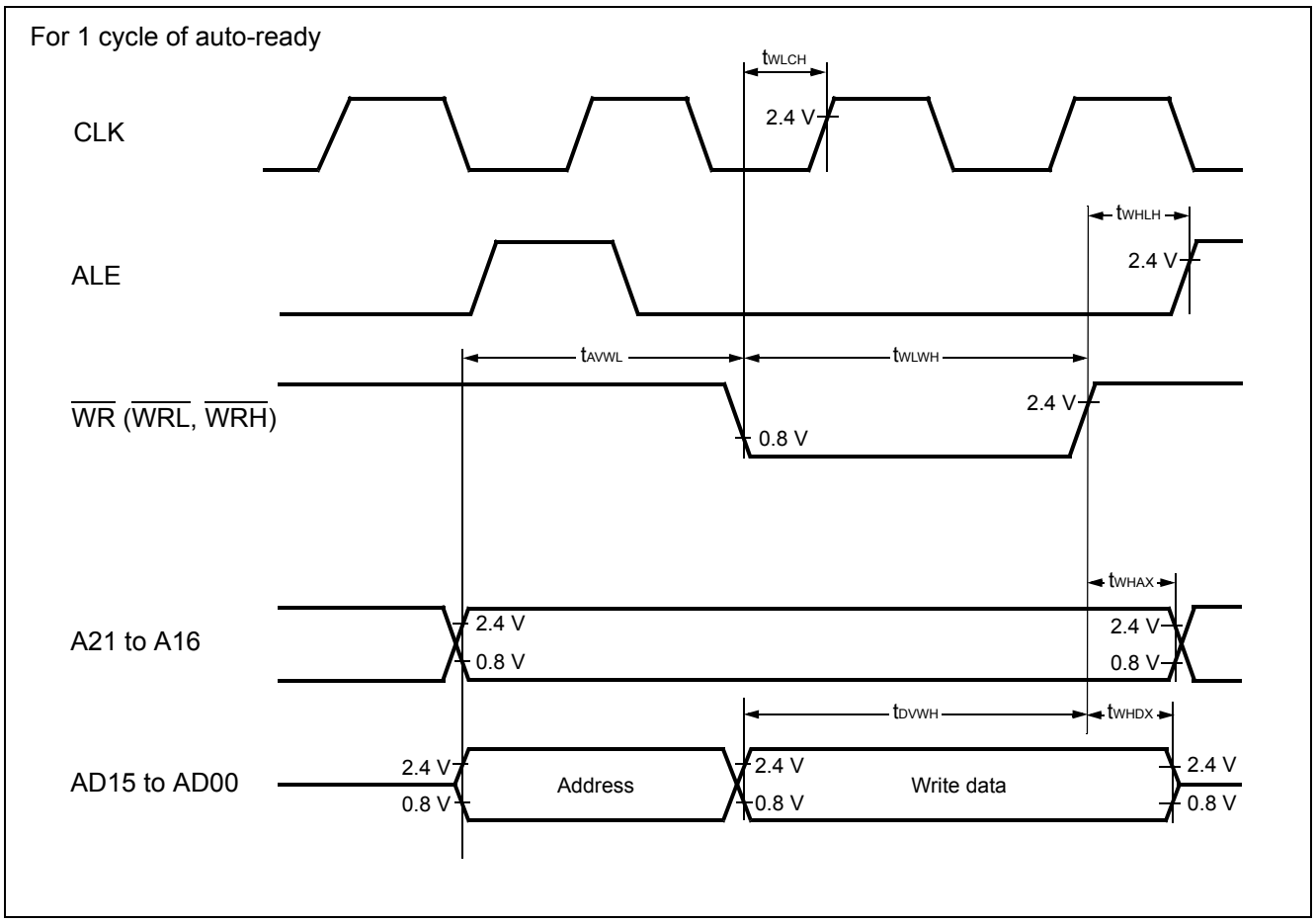
(Continued)

13.4.6 Bus Timing (Write)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A21 to A16, AD15 to AD00, $\overline{WR}$	–	t_{CP}–15	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		(n*+3/2)t_{CP} – 20	–	ns
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		(n*+3/2)t_{CP} – 20	–	ns
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	–	ns
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A21 to A16, $\overline{WR}$		t_{CP}/2 – 10	–	ns
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	–	ns
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 15	–	ns

* : Number of ready cycles



13.5 A/D Converter

(T_A = −40°C to +125°C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	AV_{SS} − 1.5×LSB	AV_{SS} + 0.5×LSB	AV_{SS} + 2.5×LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN14	AVRH − 3.5×LSB	AVRH − 1.5×LSB	AVRH + 0.5×LSB	V	
Compare time	—	—	1.0	—	16500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			2.0				4.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	×	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			1.2				4.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN14	− 0.3	—	+ 0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AV_{SS}	—	AVRH	V	
Reference voltage range	—	AVRH	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between channels	—	AN0 to AN14	—	—	4	LSB	

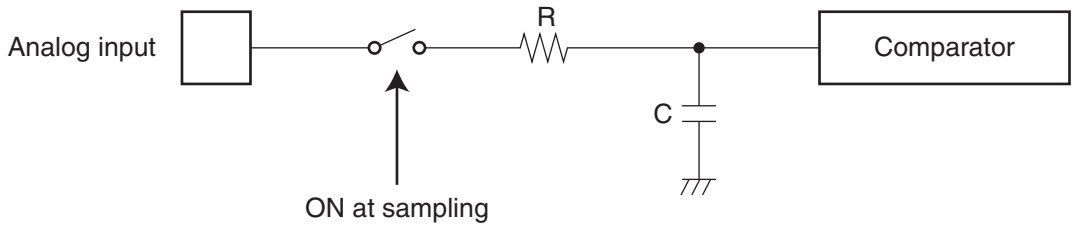
* : If A/D converter is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Notes on A/D Converter Section

■ About the external impedance of the analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting
A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

· Analog input equivalence circuit



MB90F351E(S),MB90F351TE(S),MB90F352E(S),MB90F352TE(S),
MB90F356E(S),MB90F356TE(S),MB90F357E(S),MB90F357TE(S)

	R	C
4.5 V ≤ AV_{CC} ≤ 5.5 V	2.0 kΩ (Max)	16.0 pF (Max)
4.0 V ≤ AV_{CC} ≤ 4.5 V	8.2 kΩ (Max)	16.0 pF (Max)

MB90351E(S),MB90351TE(S),MB90352E(S),MB90352TE(S),
MB90356E(S),MB90356TE(S),MB90357E(S),MB90357TE(S),
MB90V340E-101/102/103/104

	R	C
4.5 V ≤ AV_{CC} ≤ 5.5 V	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AV_{CC} ≤ 4.5 V	8.2 kΩ (Max)	14.4 pF (Max)

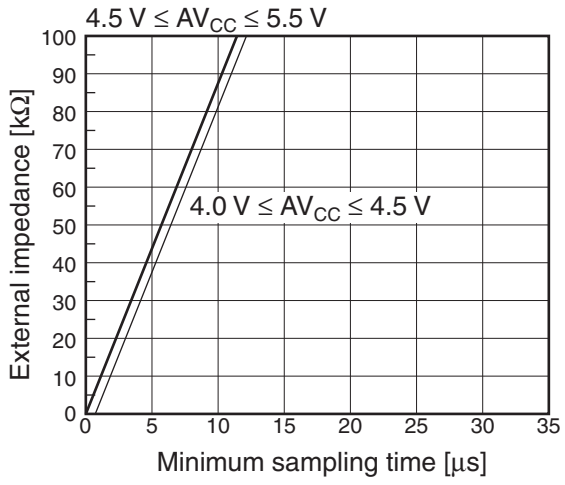
Note : The value is reference value.

■ Flash memory device

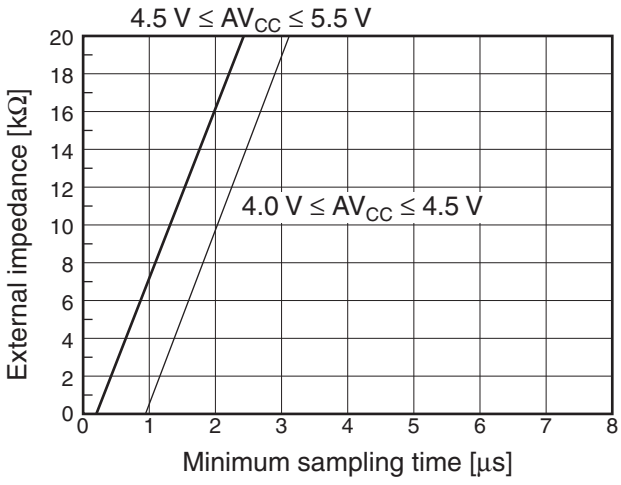
· Relation between External impedance and minimum sampling time

(MB90F351E(S),MB90F351TE(S),MB90F352E(S),MB90F352TE(S),
MB90F356E(S),MB90F356TE(S),MB90F357E(S),MB90F357TE(S))

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]

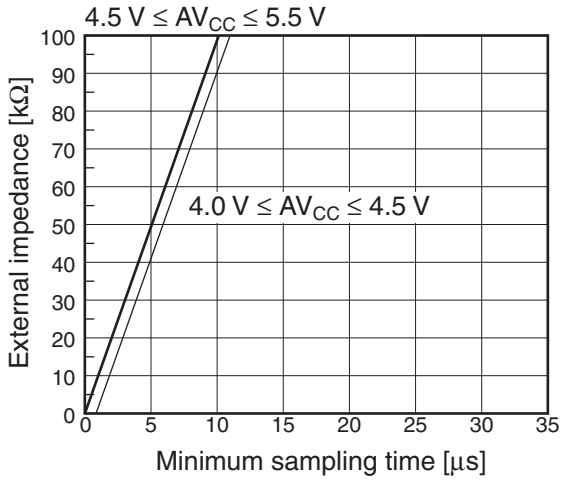


■ MASK ROM device

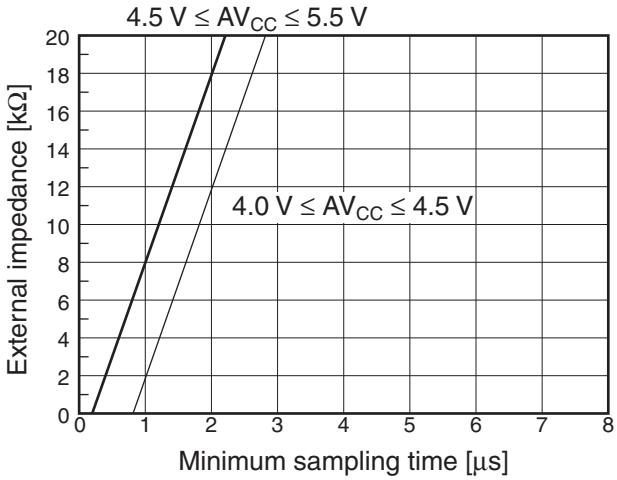
· Relation between External impedance and minimum sampling time

(MB90351E(S),MB90351TE(S),MB90352E(S),MB90352TE(S),MB90356E(S), MB90356TE(S),MB90357E(S),MB90357TE(S),MB90V340E-101/102/103/104)

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20kΩ]



■ About the error

Values of relative errors grow larger, as |AVRH − AV_{SS}| becomes smaller.