Infineon Technologies - MB90F351ESPMC1-GTE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f351espmc1-gte1

1. Product Lineup1 (Without Clock supervisor function)

■ Flash memory products

Parameter \ Part Number	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
Type	Flash memory products			
CPU	F^2MC-16LX CPU			
System clock	PLL clock multiplication circuit (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	64 Kbytes Flash memory : MB90F351E(S), MB90F351TE(S) 128 Kbytes Dual operation Flash memory (Erase/write and read can be operated at the same time) : MB90F352E(S), MB90F352TE(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No	
Clock supervisor	No			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus			
Operating temperature	−40°C to +125°C			
Package	LQFP-64			
LIN-UART	2 channels			
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	1 channel			
A/D converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit reload timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit Free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit output compare	4 channels			
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

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Part Number / Parameter	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-101	MB90V340E-102
16-bit output compare	4 channels				8 channels	
	Signals an interrupt when 16-bit free-run Timer matches output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit input capture	6 channels				8 channels	
	Retains 16-bit free-run timer value by (rising edge, falling edge, or the both edges), signals an interrupt.					
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width×12 8-bit reload registers for H pulse width×12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN interface	1 channel				3 channels	
	Compliant with CAN standard Version 2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by “H”/“L” level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash memory	—					
Corresponding evaluation name	MB90V340E-102		MB90V340E-101		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

2. Product Lineup 2 (With Clock supervisor function)

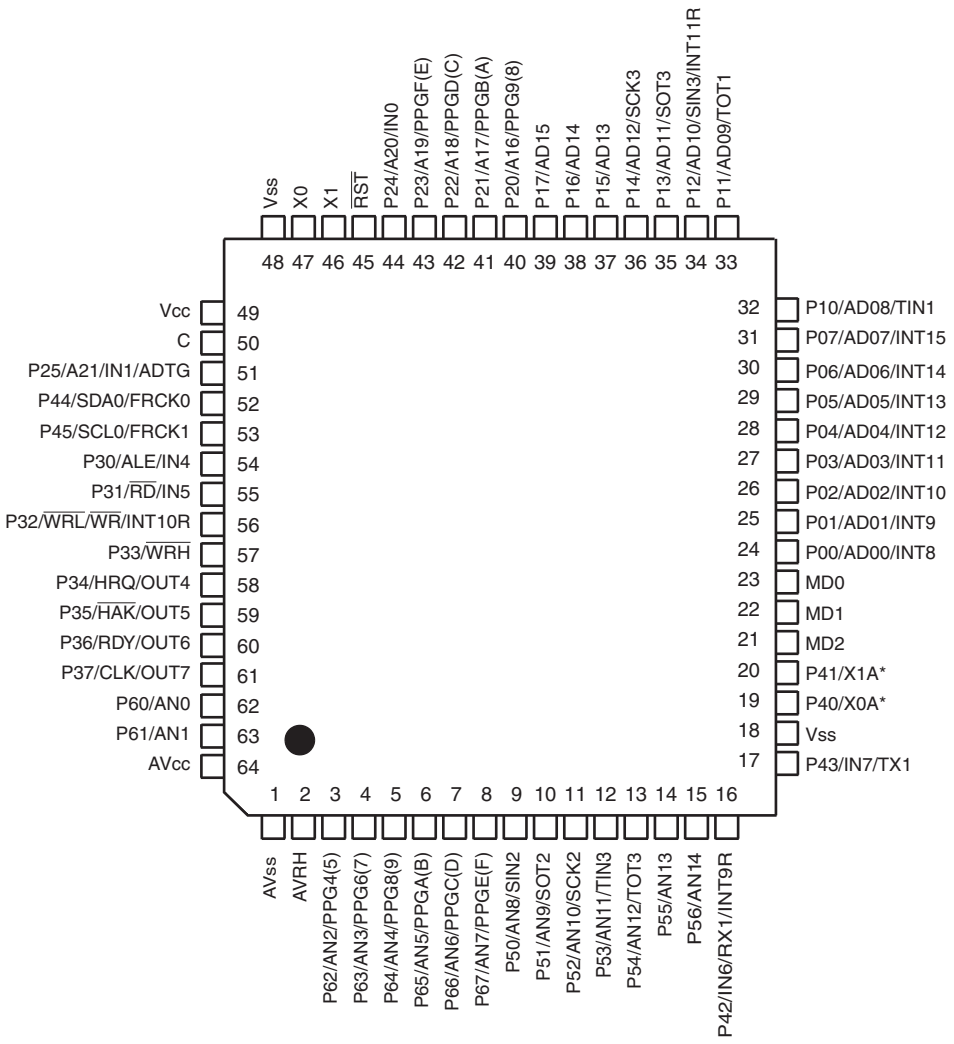
■ Flash memory products

Parameter \ Part Number	MB90F356E MB90F357E	MB90F356TE MB90F357TE	MB90F356ES MB90F357ES	MB90F356TES MB90F357TES
Type	Flash memory products			
CPU	F^2MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	64 Kbytes Flash memory : MB90F356E(S), MB90F356TE(S) 128 Kbytes Dual operation Flash memory (Erase/write and read can be operated at the same time) : MB90F357E(S), MB90F357TE(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A)	Yes		No	
Clock supervisor	Yes			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 3.5 V to 5.5 V : at using A/D converter/Flash programming 3.5 V to 5.5 V : at using external bus			
Operating temperature range	−40°C to +125°C			
Package	LQFP-64			
LIN-UART	2 channels			
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	1 channel			
A/D converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit reload timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit output compare	4 channels			
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

4. Pin Assignments

■ MB90351E (S) , MB90351TE (S) , MB90F351E (S) , MB90F351TE (S) , MB90352E (S) , MB90352TE (S) , MB90F352E (S) , MB90F352TE (S) , MB90356E (S) , MB90356TE (S) , MB90F356E (S) , MB90F356TE (S) , MB90357E (S) , MB90357TE (S) , MB90F357E (S) , MB90F357TE (S)

(TOP VIEW)



(FPT-64P-M23, FPT-64P-M24)

* : Devices without S-suffix : X0A, X1A
Devices with S-suffix : P40, P41

Pin No.	Pin name	I/O Circuit type*	Function
39	P17	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD15		Input/output pin for external bus address data bus bit 15. This function is enabled when external bus is enabled.
40 to 43	P20 to P23	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pins are enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A16 to A19		Output pins for A16 to A19 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins A16 to A19.
	PPG9 (8) PPGB (A) PPGD (C) PPGF (E)		Output pins for PPGs
44	P24	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A20		Output pin for A20 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A20.
	IN0		Data sample input pin for input capture ICU0
51	P25	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A21		Output pin for A21 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A21.
	IN1		Data sample input pin for input capture ICU1
	ADTG		Trigger input pin for A/D converter
52	P44	H	General purpose I/O port
	SDA0		Serial data I/O pin for I^2C 0
	FRCK0		Input pin for the 16-bit Free-run Timer 0
53	P45	H	General purpose I/O port
	SCL0		Serial clock I/O pin for I^2C 0
	FRCK1		Input pin for the 16-bit Free-run Timer 1

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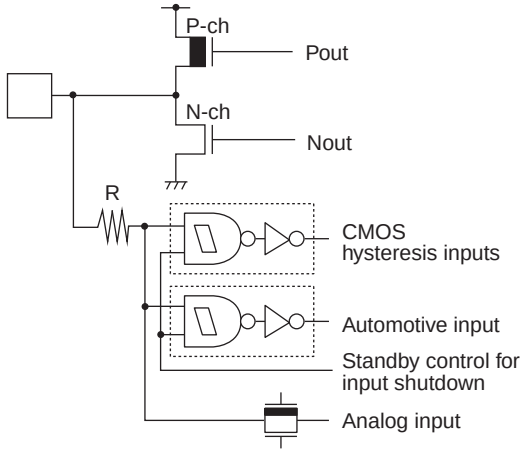
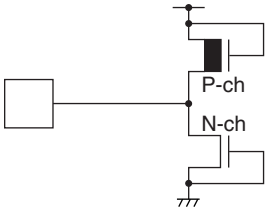
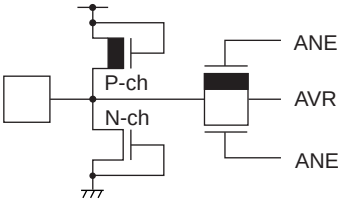
Pin No.	Pin name	I/O Circuit type*	Function
61	P37	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the CLK output disabled.
	CLK		CLK output pin. This function is enabled when both the external bus and CLK output are enabled.
	OUT7		Wave form output pin for output compare OCU7
62, 63	P60, P61	I	General purpose I/O ports
	AN0, AN1		Analog input pins for A/D converter
64	AV_{CC}	K	V_{CC} power input pin for analog circuits
2	AVRH	L	Reference voltage input for the A/D converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
1	AV_{SS}	K	V_{SS} power input pin for analog circuits
22, 23	MD1, MD0	C	Input pins for specifying the operating mode
21	MD2	D	Input pin for specifying the operating mode
49	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
18, 48	V_{SS}	—	Power (0 V) input pins
50	C	K	This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 μF ceramic capacitor.

* : For the I/O circuit type, refer to “I/O Circuit Type”.

Type	Circuit	Remarks
I		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ Analog input for A/D converter
K		Protection circuit for power supply input
L		■ With the protection circuit of A/D converter reference voltage power input pin ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH.

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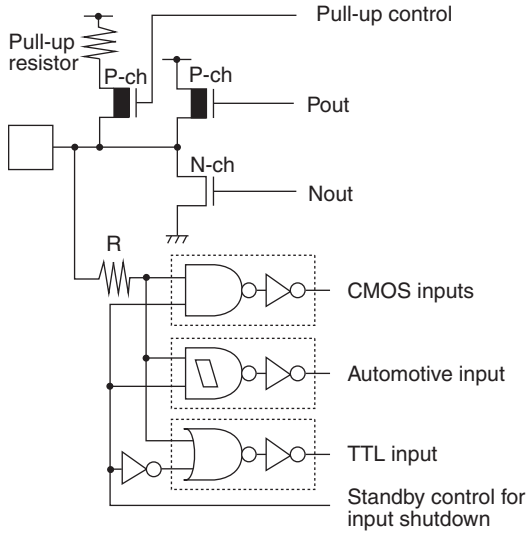
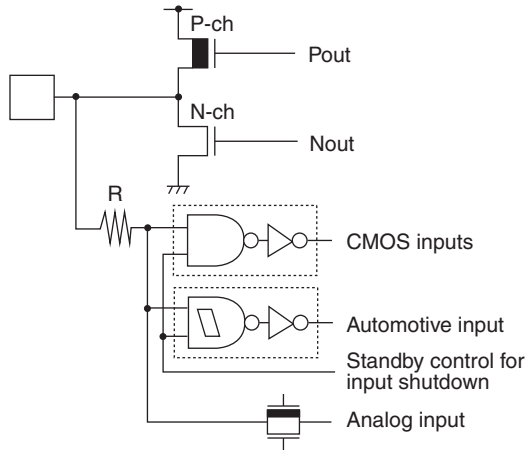
Type	Circuit	Remarks
N		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ TTL input (With the standby-time input shutdown function) ■ Programmable pull-up resistor: approx. 50 kΩ
O		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ Analog input for A/D converter

7. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions :

■A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.

■A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.

■The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage (V_{CC}) .

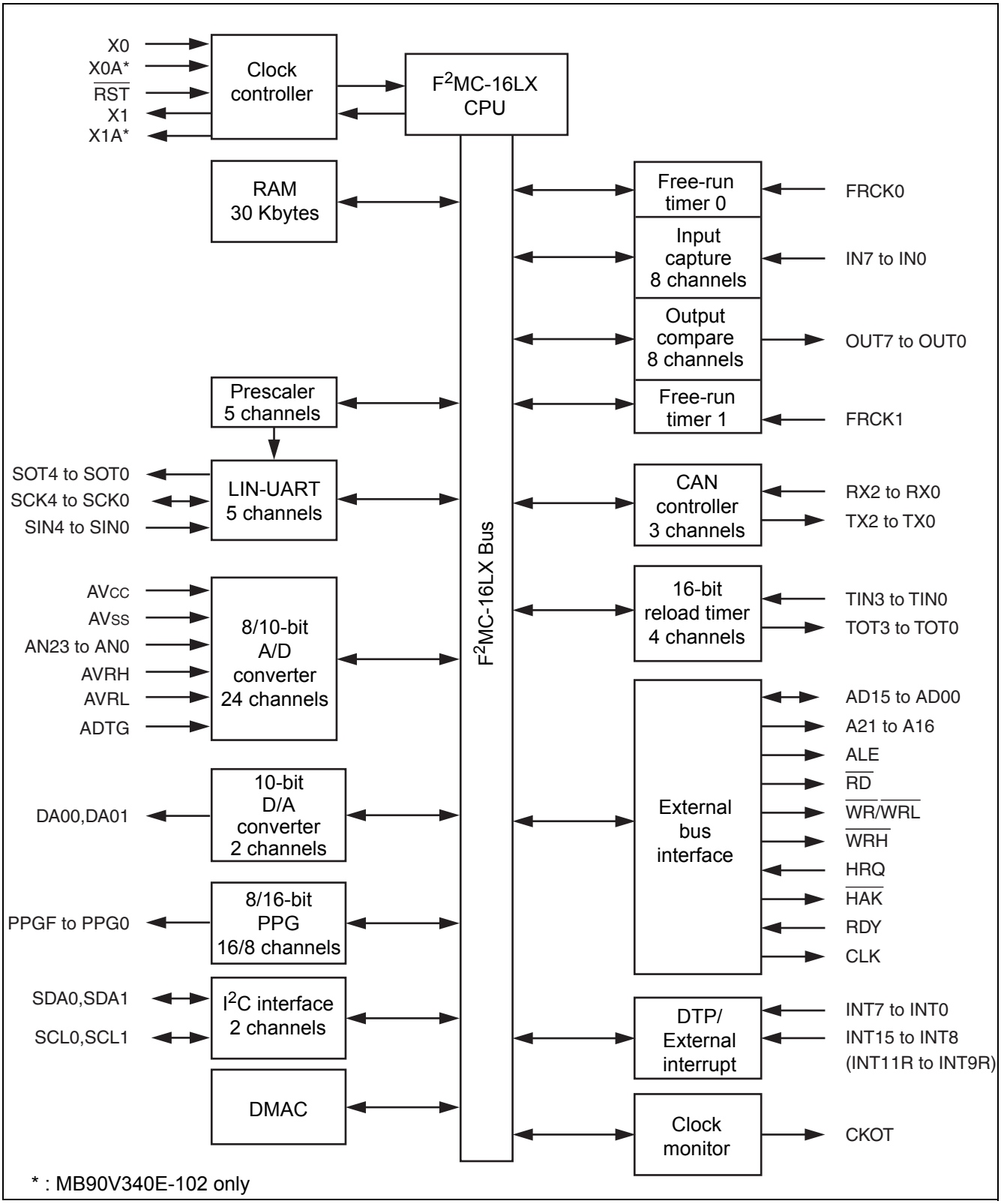
2. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

Unused I/O pins should be set to the output state and can be left open, or the input state with the above described connection.

8. Block Diagrams

■ MB90V340E-101/102



List of Message Buffers (ID Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C00_H$ to $007C1F_H$	General-purpose RAM	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C20_H$	ID register 0	IDR0	R/W	$XXXXXXXX_B$
$007C21_H$				$XXXXXXXX_B$
$007C22_H$				$XXXXXXXX_B$
$007C23_H$				$XXXXXXXX_B$
$007C24_H$	ID register 1	IDR1	R/W	$XXXXXXXX_B$
$007C25_H$				$XXXXXXXX_B$
$007C26_H$				$XXXXXXXX_B$
$007C27_H$				$XXXXXXXX_B$
$007C28_H$	ID register 2	IDR2	R/W	$XXXXXXXX_B$
$007C29_H$				$XXXXXXXX_B$
$007C2A_H$				$XXXXXXXX_B$
$007C2B_H$				$XXXXXXXX_B$
$007C2C_H$	ID register 3	IDR3	R/W	$XXXXXXXX_B$
$007C2D_H$				$XXXXXXXX_B$
$007C2E_H$				$XXXXXXXX_B$
$007C2F_H$				$XXXXXXXX_B$
$007C30_H$	ID register 4	IDR4	R/W	$XXXXXXXX_B$
$007C31_H$				$XXXXXXXX_B$
$007C32_H$				$XXXXXXXX_B$
$007C33_H$				$XXXXXXXX_B$
$007C34_H$	ID register 5	IDR5	R/W	$XXXXXXXX_B$
$007C35_H$				$XXXXXXXX_B$
$007C36_H$				$XXXXXXXX_B$
$007C37_H$				$XXXXXXXX_B$
$007C38_H$	ID register 6	IDR6	R/W	$XXXXXXXX_B$
$007C39_H$				$XXXXXXXX_B$
$007C3A_H$				$XXXXXXXX_B$
$007C3B_H$				$XXXXXXXX_B$
$007C3C_H$	ID register 7	IDR7	R/W	$XXXXXXXX_B$
$007C3D_H$				$XXXXXXXX_B$
$007C3E_H$				$XXXXXXXX_B$
$007C3F_H$				$XXXXXXXX_B$

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List of Message Buffers (DLC Registers and Data Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C60_H$	DLC register 0	DLCR0	R/W	$XXXXXXXX_B$
$007C61_H$				
$007C62_H$	DLC register 1	DLCR1	R/W	$XXXXXXXX_B$
$007C63_H$				
$007C64_H$	DLC register 2	DLCR2	R/W	$XXXXXXXX_B$
$007C65_H$				
$007C66_H$	DLC register 3	DLCR3	R/W	$XXXXXXXX_B$
$007C67_H$				
$007C68_H$	DLC register 4	DLCR4	R/W	$XXXXXXXX_B$
$007C69_H$				
$007C6A_H$	DLC register 5	DLCR5	R/W	$XXXXXXXX_B$
$007C6B_H$				
$007C6C_H$	DLC register 6	DLCR6	R/W	$XXXXXXXX_B$
$007C6D_H$				
$007C6E_H$	DLC register 7	DLCR7	R/W	$XXXXXXXX_B$
$007C6F_H$				
$007C70_H$	DLC register 8	DLCR8	R/W	$XXXXXXXX_B$
$007C71_H$				
$007C72_H$	DLC register 9	DLCR9	R/W	$XXXXXXXX_B$
$007C73_H$				
$007C74_H$	DLC register 10	DLCR10	R/W	$XXXXXXXX_B$
$007C75_H$				
$007C76_H$	DLC register 11	DLCR11	R/W	$XXXXXXXX_B$
$007C77_H$				
$007C78_H$	DLC register 12	DLCR12	R/W	$XXXXXXXX_B$
$007C79_H$				
$007C7A_H$	DLC register 13	DLCR13	R/W	$XXXXXXXX_B$
$007C7B_H$				
$007C7C_H$	DLC register 14	DLCR14	R/W	$XXXXXXXX_B$
$007C7D_H$				
$007C7E_H$	DLC register 15	DLCR15	R/W	$XXXXXXXX_B$
$007C7F_H$				

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Address	Register	Abbreviation	Access	Initial Value
CAN1				
$007CF0_H$ to $007CF7_H$	Data register 14 (8 bytes)	DTR14	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CF8_H$ to $007CFF_H$	Data register 15 (8 bytes)	DTR15	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

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*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

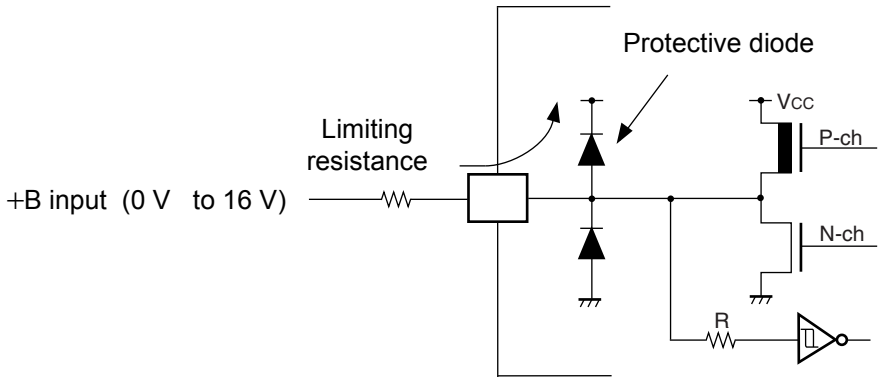
*3: V_I and V_O should not exceed $V_{CC} + 0.3$ V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56, P60 to P67

*5: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56 (for evaluation device : P50 to P55) , P60 to P67

- ″ Use within recommended operating conditions.
- ″ Use at DC voltage (current)
- ″ The +B signal should always be applied a connecting limit resistance between the +B signal and the microcontroller.
- ″ The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- ″ Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- ″ Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- ″ Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- ″ Care must be taken not to leave the +B input pin open.
- ″ Recommended circuit sample:

• Input/output equivalent circuits



*6 : If used exceeding $T_A = +105°C$, be sure to contact Cypress for reliability limitations.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

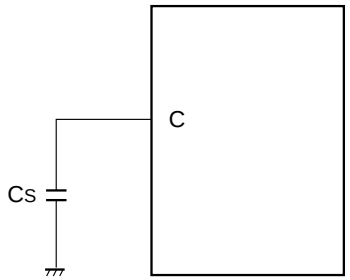
13.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	−40	—	+125	°C	*

* : If used exceeding T_A = +105°C, be sure to contact Cypress for reliability limitations.

″ C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

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(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

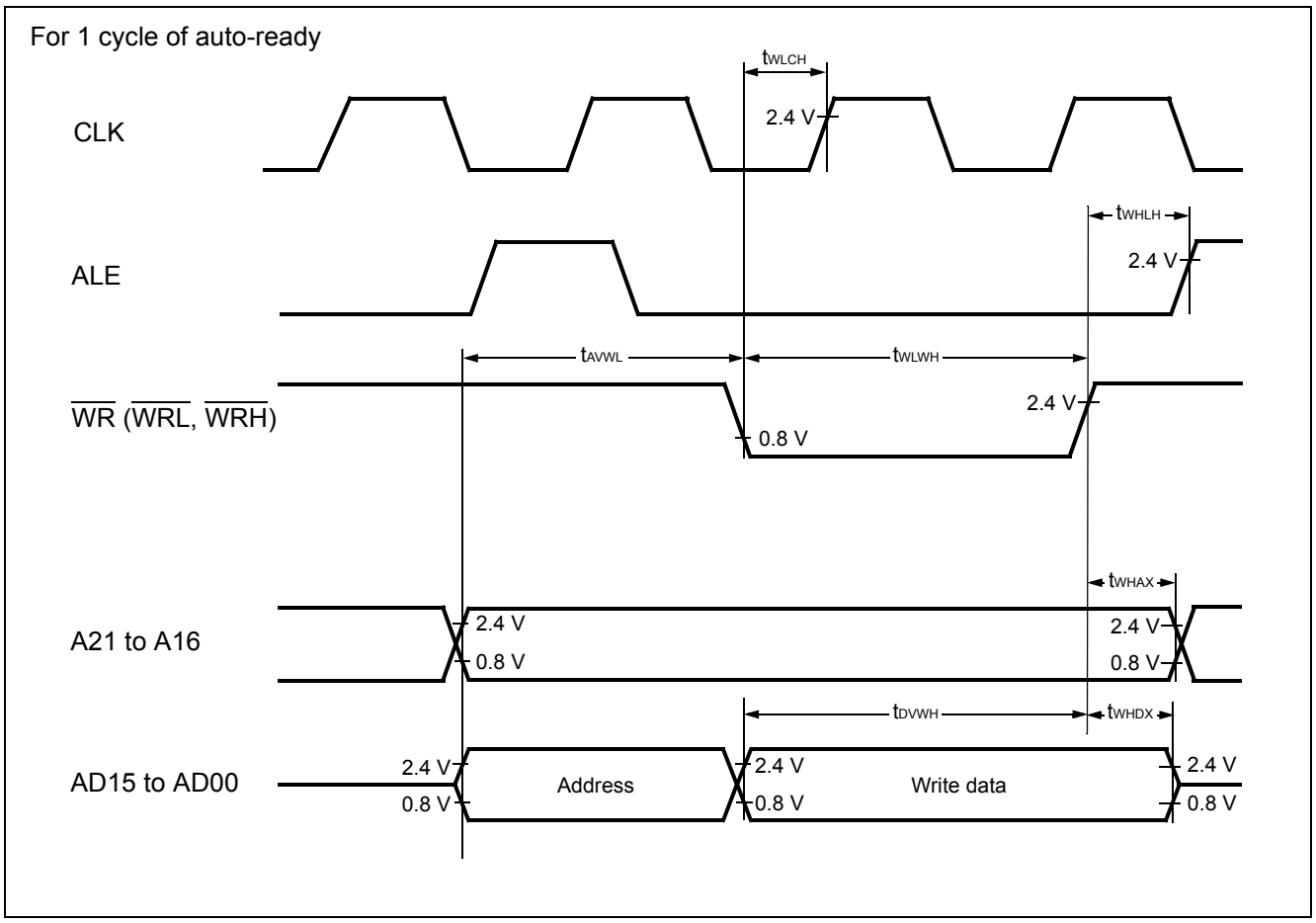
Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCT}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At watch mode T_A = +25°C	—	10	35	µA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At watch mode T_A = +25°C	—	25	150	µA	MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At watch mode T_A = +25°C	—	25	150	µA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At watch mode T_A = +25°C	—	60	140	µA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At watch mode T_A = +25°C	—	80	250	µA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At watch mode T_A = +25°C	—	80	250	µA	MB90356TES MB90F356TES MB90357TES MB90F357TES
	I_{CCH}		V_{CC} = 5.0 V, At stop mode, T_A = +25°C	—	7	25	µA	Devices without “T”-suffix
				—	60	130	µA	Devices with “T”-suffix
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, V_{CC}, V_{SS}	—	—	5	15	pF	

13.4.6 Bus Timing (Write)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A21 to A16, AD15 to AD00, $\overline{WR}$	–	t_{CP}–15	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		(n*+3/2)t_{CP} – 20	–	ns
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		(n*+3/2)t_{CP} – 20	–	ns
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	–	ns
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A21 to A16, $\overline{WR}$		t_{CP}/2 – 10	–	ns
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	–	ns
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 15	–	ns

* : Number of ready cycles

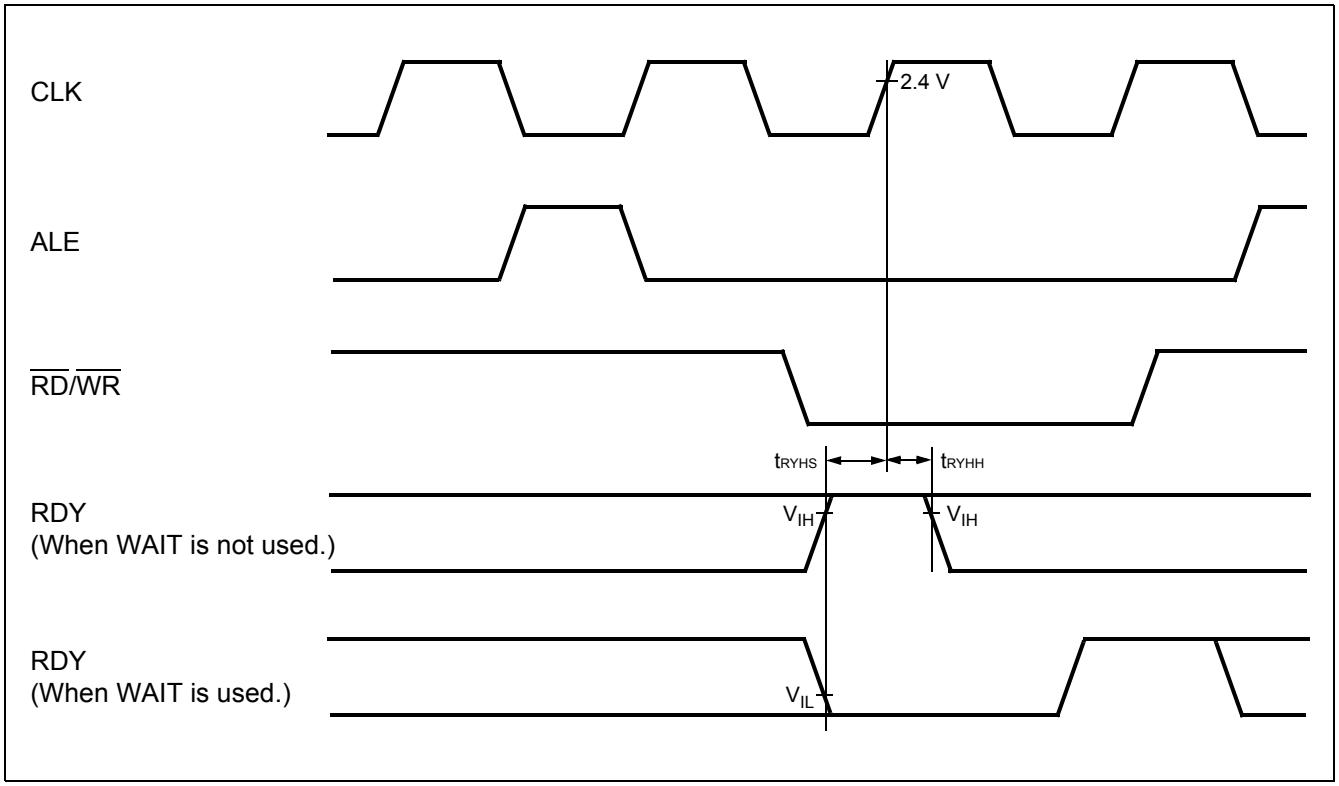


13.4.7 Ready Input Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
RDY set-up time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

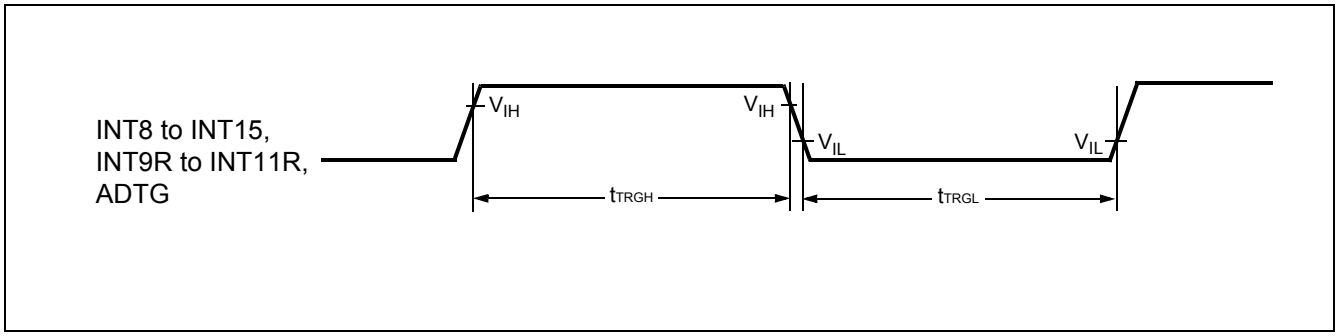
Note : If the RDY set-up time is insufficient, use the auto-ready function.



13.4.10 Trigger Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

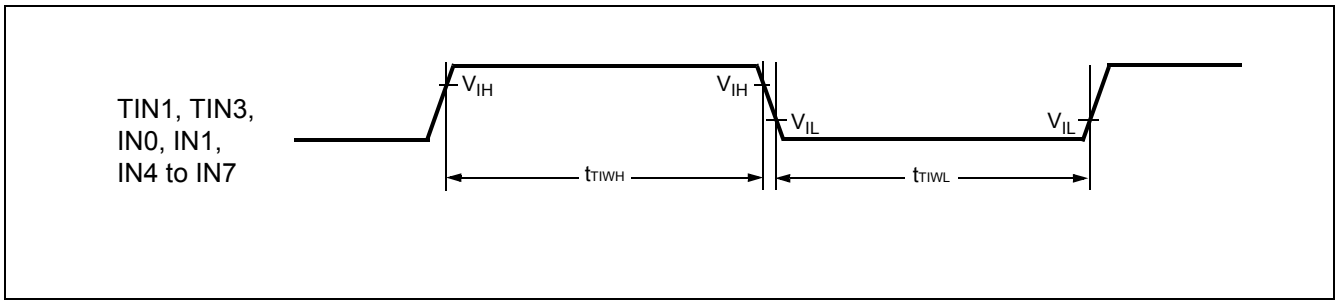
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	5 t_{CP}	—	ns



13.4.11 Timer Related Resource Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN1, TIN3,IN0, IN1, IN4 to IN7	—	4 t_{CP}	—	ns



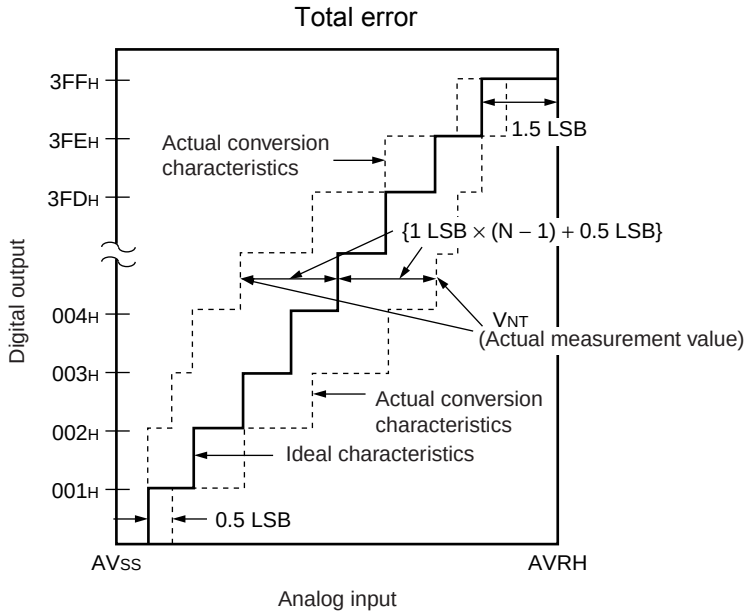
13.4.12 Timer Related Resource Output Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT1, TOT3, PPG4, PPG6, PPG8 to PPGF	—	30	—	ns

13.6 Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation between a line across zero-transition line (“00 0000 0000” ← → “00 0000 0001”) and full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) and actual conversion characteristics.
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between an actual value and a theoretical value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{AVRH - AV_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

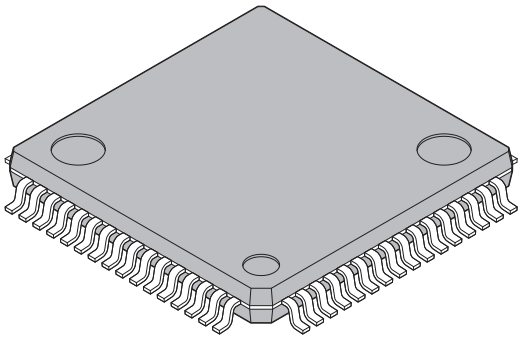
V_{OT} (Ideal value) $= AV_{SS} + 0.5$ LSB [V]

V_{FST} (Ideal value) $= AVRH - 1.5$ LSB [V]

V_{NT} : A voltage at which digital output transits from $(N - 1)_H$ to N_H.

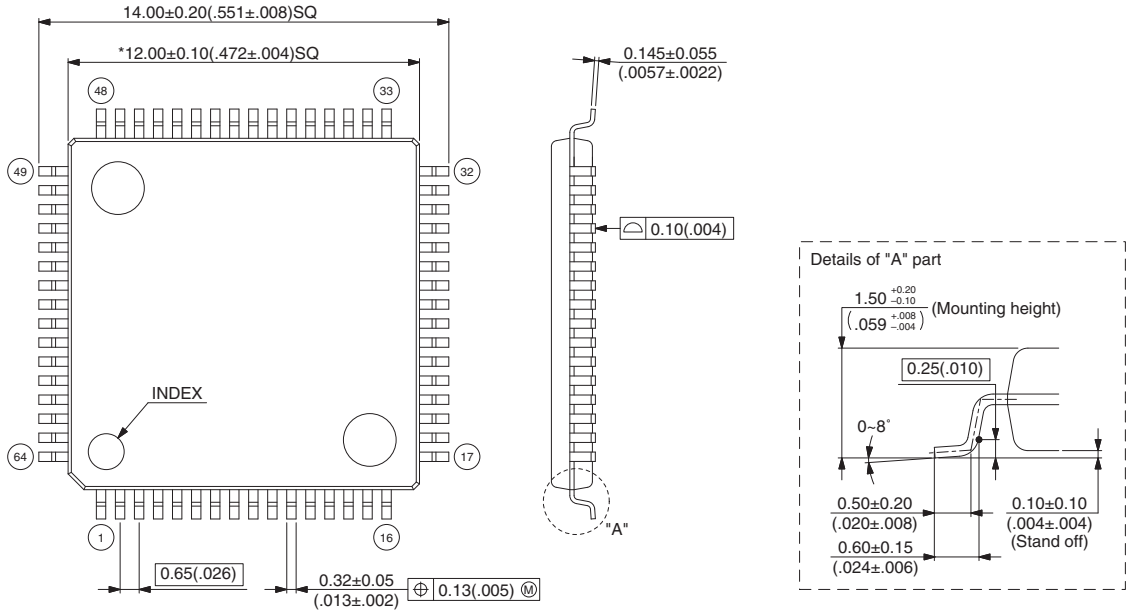
(Continued)

14.1 Package Dimensions

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65
(FPT-64P-M23)		

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)