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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352espmc1-gs-spe2

- 8/16-bit PPG timer : 8-bit ∞ 10 channels or 16-bit × 6 channels

- 16-bit reload timer : 2 channels (only Evaluation products has 4 channels)

- 16- bit input/output timer
  - 16-bit free-run timer : 2 channels (FRT0 : ICU0/1, FRT1 : ICU4/5/6/7, OCU4/5/6/7)
  - 16- bit input capture: (ICU) : 6 channels
  - 16-bit output compare : (OCU) : 4 channels

FULL-CAN interface: 1 channel

- Compliant with CAN standard Version2.0 Part A and Part B

- 16 message buffers are built-in

- CAN wake-up function

LIN-UART: 2 channels

- Equipped with full-duplex double buffer

- Clock-asynchronous or clock-synchronous serial transmission is available.

I^{2}C interface: 1 channel

Up to 400 kbps transfer rate

DTP/External interrupt: 8 channels, CAN wakeup: 1 channel

Module for activation of extended intelligent I/O service (EI^{2}OS), DMA, and generation of external interrupt by external input.

Delay interrupt generator module

Generates interrupt request for task switching.

8/10-bit A/D converter: 15 channels

- Resolution is selectable between 8-bit and 10-bit.

- Activation by external trigger input is allowed.

- Conversion time : 3 μs (at 24 MHz machine clock, including sampling time)

Address matching detection (Program patch) function

- Address matching detection for 6 address pointers.

Capable of changing input voltage level for port

- Automotive/CMOS-Schmitt (initial level is Automotive in single chip mode)

- TTL level (corresponds to external bus pins only, initial level of these pins is TTL in external bus mode)

Low voltage/CPU operation detection reset (devices with T-suffix)

- Detects low voltage (4.0 V $\pm$ 0.3 V) and resets automatically

- Resets automatically when program is runaway and counter is not cleared within interval time
  (approx. 262 ms : external 4 MHz)

Dual operation Flash memory (only devices 128 Kbytes Flash memory)

- Erase/write and read can be executed in the different bank (Upper Bank/Lower Bank) at the same time.

Supported T$_A$ = + 125°C

The maximum operating frequency is 24 MHz* : (at T$_A$ = +125°C) .

Flash security function

- Protects the content of Flash memory
  (MB90F352x, MB90F357x only)

External bus interface

- 4 Mbytes external memory space
  MB90F351E(S), MB90F351TE(S), MB90F352E(S), MB90F352TE(S) : External bus Interface can not be used in internal vector mode. It can be used only in external vector mode.

- * : If used exceeding T$_A$ = + 105 °C, be sure to contact Cypress for reliability limitations.

1. Product Lineup1 (Without Clock supervisor function)

■ Flash memory products

Part Number / Parameter	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
Type	Flash memory products			
CPU	F^2MC-16LX CPU			
System clock	PLL clock multiplication circuit ($\times$ 1, $\times$ 2, $\times$ 3, $\times$ 4, $\times$ 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL $\times$ 6)			
ROM	64 Kbytes Flash memory : MB90F351E(S), MB90F351TE(S) 128 Kbytes Dual operation Flash memory (Erase/write and read can be operated at the same time) : MB90F352E(S), MB90F352TE(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No	
Clock supervisor	No			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus			
Operating temperature	$-40°C$ to $+125°C$			
Package	LQFP-64			
LIN-UART	2 channels			
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	1 channel			
A/D converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit reload timer (2 channels)	Operation clock frequency : $fsys/2^1$, $fsys/2^3$, $fsys/2^5$ (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit Free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4) . Operation clock frequency : fsys, $fsys/2^1$, $fsys/2^2$, $fsys/2^3$, $fsys/2^4$, $fsys/2^5$, $fsys/2^6$, $fsys/2^7$ (fsys = Machine clock frequency)			
16-bit output compare	4 channels			
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

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Part Number / Parameter	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-101	MB90V340E-102
16-bit output compare	4 channels				8 channels	
	Signals an interrupt when 16-bit free-run Timer matches output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit input capture	6 channels				8 channels	
	Retains 16-bit free-run timer value by (rising edge, falling edge, or the both edges), signals an interrupt.					
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width×12 8-bit reload registers for H pulse width×12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN interface	1 channel				3 channels	
	Compliant with CAN standard Version 2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by "H"/"L" level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash memory	—					
Corresponding evaluation name	MB90V340E-102		MB90V340E-101		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

2. Product Lineup 2 (With Clock supervisor function)

■ Flash memory products

Part Number Parameter	MB90F356E MB90F357E	MB90F356TE MB90F357TE	MB90F356ES MB90F357ES	MB90F356TES MB90F357TES
Type	Flash memory products			
CPU	F^2MC-16LX CPU			
System clock	On-chip PLL clock multiplier ($\times1$, $\times2$, $\times3$, $\times4$, $\times6$, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL $\times$ 6)			
ROM	64 Kbytes Flash memory : MB90F356E(S), MB90F356TE(S) 128 Kbytes Dual operation Flash memory (Erase/write and read can be operated at the same time) : MB90F357E(S), MB90F357TE(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A)	Yes		No	
Clock supervisor	Yes			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 3.5 V to 5.5 V : at using A/D converter/Flash programming 3.5 V to 5.5 V : at using external bus			
Operating temperature range	$-40°C$ to $+125°C$			
Package	LQFP-64			
LIN-UART	2 channels			
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	1 channel			
A/D converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit reload timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit output compare	4 channels			
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

3. Packages and Product Correspondence

Package	MB90V340E-101 MB90V340E-102 MB90V340E-103 MB90V340E-104	MB90351E (S) , MB90351TE (S) MB90F351E (S) , MB90F351TE (S) MB90352E (S) , MB90352TE (S) MB90F352E (S) , MB90F352TE (S) MB90356E (S) , MB90356TE (S) MB90F356E (S) , MB90F356TE (S) MB90357E (S) , MB90357TE (S) MB90F357E (S) , MB90F357TE (S)
PGA-299C-A01	◯	×
FPT-64P-M23 (12.0 mm □ , 0.65 mm pitch)	×	◯
FPT-64P-M24 (10.0 mm □ , 0.50 mm pitch)	×	◯

◯ : Yes, × : No

Note : Refer to "Package Dimensions" for detail of each package.

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Pin No.	Pin name	I/O Circuit type*	Function
61	P37	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the CLK output disabled.
	CLK		CLK output pin. This function is enabled when both the external bus and CLK output are enabled.
	OUT7		Wave form output pin for output compare OCU7
62, 63	P60, P61	I	General purpose I/O ports
	AN0, AN1		Analog input pins for A/D converter
64	AV$_{CC}$	K	V$_{CC}$ power input pin for analog circuits
2	AVRH	L	Reference voltage input for the A/D converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV$_{CC}$.
1	AV$_{SS}$	K	V$_{SS}$ power input pin for analog circuits
22, 23	MD1, MD0	C	Input pins for specifying the operating mode
21	MD2	D	Input pin for specifying the operating mode
49	V$_{CC}$	—	Power (3.5 V to 5.5 V) input pin
18, 48	V$_{SS}$	—	Power (0 V) input pins
50	C	K	This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 μF ceramic capacitor.

* : For the I/O circuit type, refer to "I/O Circuit Type".

6. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM device CMOS hysteresis input pin ■ Flash memory device CMOS input pin
D		■ MASK ROM device CMOS hysteresis input pin Pull-down resistor value: approx. 50 kΩ ■ Flash memory device CMOS input pin No Pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

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Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

9. Turning-on sequence of power supply to A/D converter and analog inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN14) after turning-on the digital power supply (V_{CC}) .Turn-off the digital power after turning off the A/D converter power
supply and analog inputs. In this case, make sure that the power supply voltage does not exceed the rated voltage of the A/D converter (turning on/of the analog and digital power supplies simultaneously is acceptable).

10. Connection of unused pins of A/D converter if A/D converter is not used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

11. Notes on energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at
50 μs or more (0.2 V to 2.7 V) .

12. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/
60 MHz) fall below 10$\%$ of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.
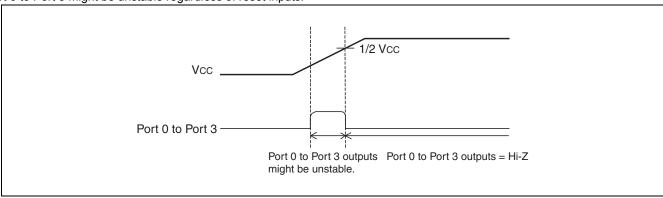
13. Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

14. Port 0 to port 3 output during power-on (External-bus mode)

As shown below, when power is turned on in external-bus mode, there is a possibility that output signal of
Port 0 to Port 3 might be unstable regardless of reset inputs.

15. Setting using CAN function

To use CAN function, please set "1" to DIRECT bit of CAN direct mode register (CDMR).

16. Flash security function

The security byte is located in the area of the Flash memory. If protection code 01_H is written in the security byte, the Flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Please refer to following table for the address of the security byte.

Product name	Flash memory size	Address for security bit
MB90F352E(S) MB90F352TE(S) MB90F357E(S) MB90F357TE(S)	Embedded 1 Mbit Flash memory	$FE0001_H$

17. Operation with $T_A = +105°C$ or more

If used exceeding $T_A = +105°C$, please contact Cypress sales representatives for reliability limitations.

18. Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.
The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

(1) Low voltage detection reset circuit

Detection voltage
4.0 V $\pm$ 0.3 V

When a low voltage condition is detected, the low voltage detection flag (LVRC : LVRF) is set to "1" and an internal reset signal is output.
Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.

During an internal RAM write cycle, low voltage reset is generated after the completion of writing. During the output of this internal reset, the reset output from the low voltage detection reset circuit is suppressed.

(2) CPU operation detection reset circuit

The CPU operation detection reset circuit is a counter that prevents program runaway. The counter starts automatically after a power-on reset, and must be continually and regularly cleared within a given time. If the given time interval elapses and the counter has not been cleared, a cause such as infinite program looping is assumed and an internal reset signal is generated. The internal reset generated from the CPU operation detection circuit has a width of 5 machine cycles.

Interval time
$2^{20}/F_C$ (approx. 262 ms*)

* : This value assumes the interval time at an oscillation clock frequency of 4 MHz.
   During recovery from standby mode, the detection period is the maximum interval plus 20 μs.

   This circuit does not operate in modes where CPU operation is stopped.
   The CPU operation detection reset circuit counter is cleared under any of the following conditions.

■ "0" writing to CL bit of LVRC register

■ Internal reset

■ Main oscillation clock stop

■ Transit to sleep mode
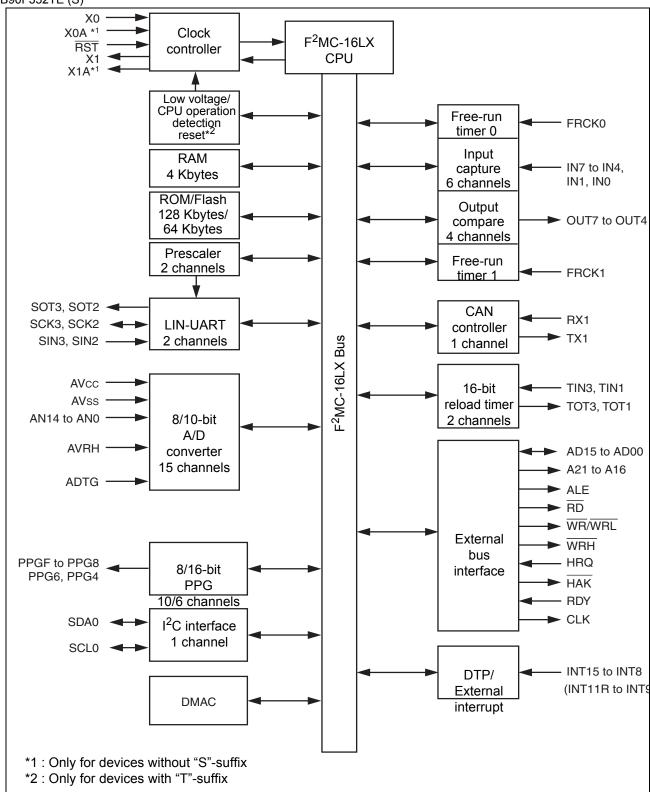
■ Transit to timebase timer mode and watch mode

19. Internal CR oscillation circuit

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Oscillation frequency	f_{RC}	50	100	200	kHz
Oscillation stabilization wait time	tstab	—	—	100	μs

■ MB90351E (S) , MB90351TE (S) , MB90F351E (S) , MB90F351TE (S) , MB90352E (S) , MB90352TE (S) , MB90F352E (S)
MB90F352TE (S)

X0 → Clock controller
X0A *1 →
$\overline{RST}$ →
X1 ←
X1A*1 ←

Clock controller → F^{2}MC-16LX CPU

Low voltage/ CPU operation detection reset*2

RAM 4 Kbytes

ROM/Flash 128 Kbytes/ 64 Kbytes

Prescaler 2 channels

SOT3, SOT2 ←
SCK3, SCK2 ↔ LIN-UART 2 channels
SIN3, SIN2 →

AV$_{CC}$ →
AV$_{SS}$ →
AN14 to AN0 → 8/10-bit A/D converter 15 channels
AVRH →
ADTG →

PPGF to PPG8 PPG6, PPG4 ← 8/16-bit PPG 10/6 channels

SDA0 ↔ I^{2}C interface 1 channel
SCL0 ↔

DMAC

F^{2}MC-16LX Bus

Free-run timer 0 ← FRCK0

Input capture 6 channels ← IN7 to IN4, IN1, IN0

Output compare 4 channels → OUT7 to OUT4

Free-run timer 1 ← FRCK1

CAN controller 1 channel ← RX1 → TX1

16-bit reload timer 2 channels ← TIN3, TIN1 → TOT3, TOT1

External bus interface
↔ AD15 to AD00
→ A21 to A16
→ ALE
→ $\overline{RD}$
→ $\overline{WR}/\overline{WRL}$
→ $\overline{WRH}$
← HRQ
→ $\overline{HAK}$
← RDY
→ CLK

DTP/ External interrupt ← INT15 to INT8 (INT11R to INT9

*1 : Only for devices without "S"-suffix
*2 : Only for devices with "T"-suffix

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
007924$_H$ to 007927$_H$	Reserved				
007928$_H$	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXX$_B$
007929$_H$	Input Capture Register 4	IPCP4	R		XXXXXXXX$_B$
00792A$_H$	Input Capture Register 5	IPCP5	R		XXXXXXXX$_B$
00792B$_H$	Input Capture Register 5	IPCP5	R		XXXXXXXX$_B$
00792C$_H$	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXX$_B$
00792D$_H$	Input Capture Register 6	IPCP6	R		XXXXXXXX$_B$
00792E$_H$	Input Capture Register 7	IPCP7	R		XXXXXXXX$_B$
00792F$_H$	Input Capture Register 7	IPCP7	R		XXXXXXXX$_B$
007930$_H$ to 007937$_H$	Reserved				
007938$_H$	Output Compare Register 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX$_B$
007939$_H$	Output Compare Register 4	OCCP4	R/W		XXXXXXXX$_B$
00793A$_H$	Output Compare Register 5	OCCP5	R/W		XXXXXXXX$_B$
00793B$_H$	Output Compare Register 5	OCCP5	R/W		XXXXXXXX$_B$
00793C$_H$	Output Compare Register 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX$_B$
00793D$_H$	Output Compare Register 6	OCCP6	R/W		XXXXXXXX$_B$
00793E$_H$	Output Compare Register 7	OCCP7	R/W		XXXXXXXX$_B$
00793F$_H$	Output Compare Register 7	OCCP7	R/W		XXXXXXXX$_B$
007940$_H$	Timer Data Register 0	TCDT0	R/W	Free-run Timer 0	00000000$_B$
007941$_H$	Timer Data Register 0	TCDT0	R/W		00000000$_B$
007942$_H$	Timer Control Status Register 0	TCCSL0	R/W		00000000$_B$
007943$_H$	Timer Control Status Register 0	TCCSH0	R/W		0XXXXXXX$_B$
007944$_H$	Timer Data Register 1	TCDT1	R/W	Free-run Timer 1	00000000$_B$
007945$_H$	Timer Data Register 1	TCDT1	R/W		00000000$_B$
007946$_H$	Timer Control Status Register 1	TCCSL1	R/W		00000000$_B$
007947$_H$	Timer Control Status Register 1	TCCSH1	R/W		0XXXXXXX$_B$
007948$_H$	Timer Register 0/Reload Register 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX$_B$
007949$_H$			R/W		XXXXXXXX$_B$
00794A$_H$	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX$_B$
00794B$_H$			R/W		XXXXXXXX$_B$
00794C$_H$	Timer Register 2/Reload Register 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX$_B$
00794D$_H$			R/W		XXXXXXXX$_B$
00794E$_H$	Timer Register 3/Reload Register 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX$_B$
00794F$_H$			R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007950$_H$	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000$_B$
007951$_H$	Serial Control Register 3	SCR3	W, R/W		00000000$_B$
007952$_H$	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000$_B$
007953$_H$	Serial Status Register 3	SSR3	R,R/W		00001000$_B$
007954$_H$	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX$_B$
007955$_H$	Extended Status Control Register 3	ESCR3	R/W		00000100$_B$
007956$_H$	Baud Rate Generator Register 30	BGR30	R/W		00000000$_B$
007957$_H$	Baud Rate Generator Register 31	BGR31	R/W		00000000$_B$
007958$_H$, 007959$_H$	Reserved				
007960$_H$	Clock supervisor Control Register	CSVCR	R, R/W	Clock Supervisor	00011100$_B$
007961$_H$ to 00796D$_H$	Reserved				
00796E$_H$	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	XXXXXXX0$_B$
00796F$_H$	Reserved				
007970$_H$	I^{2}C Bus Status Register 0	IBSR0	R	I^{2}C Interface 0	00000000$_B$
007971$_H$	I^{2}C Bus Control Register 0	IBCR0	W,R/W		00000000$_B$
007972$_H$	I^{2}C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000$_B$
007973$_H$		ITBAH0	R/W		00000000$_B$
007974$_H$	I^{2}C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111$_B$
007975$_H$		ITMKH0	R/W		00111111$_B$
007976$_H$	I^{2}C 7-bit Slave Address Register 0	ISBA0	R/W		00000000$_B$
007977$_H$	I^{2}C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111$_B$
007978$_H$	I^{2}C data register 0	IDAR0	R/W		00000000$_B$
007979$_H$, 00797A$_H$	Reserved				
00797B$_H$	I^{2}C Clock Control Register 0	ICCR0	R/W	I^{2}C Interface 0	00011111$_B$
00797C$_H$ to 0079A1$_H$	Reserved				
0079A2$_H$	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000$_B$
0079A3$_H$	Flash Write Control Register 1	FWR1	R/W		00000000$_B$
0079A4$_H$	Sector Change Setting Register 0	SSR0	R/W		00XXXXX0$_B$
0079A5$_H$ to 0079C1$_H$	Reserved				
0079C2$_H$	Clock modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000$_B$

(Continued)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C80$_H$ to 007C87$_H$	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007C88$_H$ to 007C8F$_H$	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007C90$_H$ to 007C97$_H$	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007C98$_H$ to 007C9F$_H$	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CA0$_H$ to 007CA7$_H$	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CA8$_H$ to 007CAF$_H$	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CB0$_H$ to 007CB7$_H$	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CB8$_H$ to 007CBF$_H$	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CC0$_H$ to 007CC7$_H$	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CC8$_H$ to 007CCF$_H$	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CD0$_H$ to 007CD7$_H$	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CD8$_H$ to 007CDF$_H$	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CE0$_H$ to 007CE7$_H$	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$
007CE8$_H$ to 007CEF$_H$	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX$_B$ to XXXXXXXX$_B$

(Continued)

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Interrupt cause	EI^{2}OS corresponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	**Address**	**Number**	**Address**
UART 2 RX	Y2	14	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART 2 TX	Y1	15	#40	FFFF5C$_H$		
Flash Memory	N	—	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed Interrupt	N	—	#42	FFFF54$_H$		

Y1 : Usable

Y2 : Usable, with EI^{2}OS stop function

N : Unusable

Notes : • The peripheral resources sharing the ICR register have the same interrupt level.
  • When the peripheral resources sharing the ICR register use extended intelligent I/O service, only one can use EI^{2}OS at a time.
  • When either of the two peripheral resources sharing the ICR register specifies EI^{2}OS, the other one cannot use interrupts.

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	**Max**		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$*2
	AVRH	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH$*2
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	I_{CLAMP}	−4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma|I_{CLAMP}|$	—	40	mA	*5
"L" level maximum output current	I_{OL}	—	15	mA	*4
"L" level average output current	I_{OLAV}	—	4	mA	*4
"L" level maximum overall output current	ΣI_{OL}	—	100	mA	*4
"L" level average overall output current	ΣI_{OLAV}	—	50	mA	*4
"H" level maximum output current	I_{OH}	—	−15	mA	*4
"H" level average output current	I_{OHAV}	—	−4	mA	*4
"H" level maximum overall output current	ΣI_{OH}	—	−100	mA	*4
"H" level average overall output current	ΣI_{OHAV}	—	−50	mA	*4
Power consumption	P_D	—	454	mW	
Operating temperature	T_A	−40	+105	°C	
		−40	+125	°C	*6
Storage temperature	T_{STG}	−55	+150	°C	

(Continued)
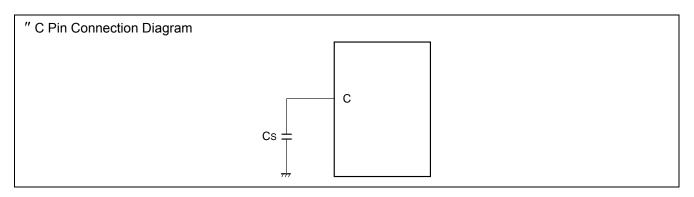
13.2 Recommended Operating Conditions

$(V_{SS} = AV_{SS} = 0\ V)$

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	μF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	−40	—	+125	°C	*

* : If used exceeding $T_A = +105°C$, be sure to contact Cypress for reliability limitations.

″ C Pin Connection Diagram

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.