Infineon Technologies - MB90F352ESPMC1-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352espmc1-gse2

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Parameter \ Part Number	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
16-bit Input capture	6 channels			
	Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge) , signals an interrupt.			
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width×12			
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN interface	1 channel			
	Compliant with CAN standard Version2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External interrupt	8 channels			
	Can be used rising edge, falling edge, starting up by “H”/“L” level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.			
D/A converter	—			
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F352E(S) and MB90F352TE(S) only)			
Corresponding evaluation name	MB90V340E-102		MB90V340E-101	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

■ MASK ROM products/Evaluation products

Parameter \ Part Number	MB90356E MB90357E	MB90356TE MB90357TE	MB90356ES MB90357ES	MB90356TES MB90357TES	MB90V340E-103	MB90V340E-104
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64 Kbytes :MB90356E(S), MB90356TE(S) 128 Kbytes :MB90357E(S), MB90357TE(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A)	Yes		No		No	Yes
Clock supervisor	Yes					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40°C to +125°C				—	
Package	LQFP-64				PGA-299	
LIN-UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 kbps)	1 channel				2 channels	
A/D converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit reload timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				Free-run Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. Free-run Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

(Continued)

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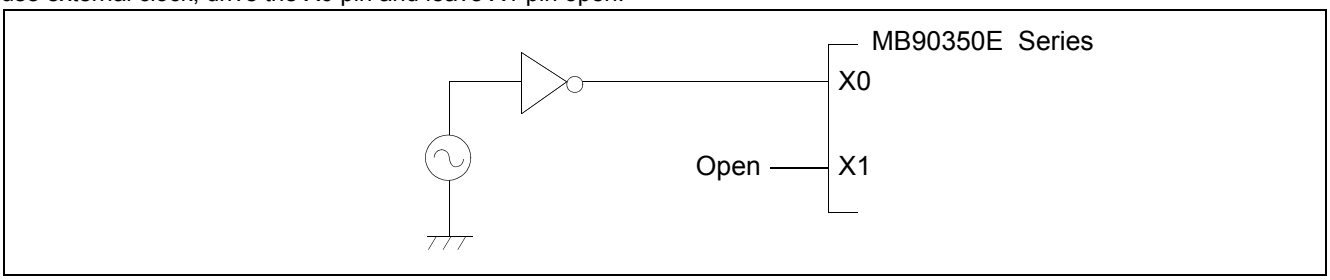
Parameter \ Part Number	MB90356E MB90357E	MB90356TE MB90357TE	MB90356ES MB90357ES	MB90356TES MB90357TES	MB90V340E-103	MB90V340E-104
16-bit output compare	4 channels				8 channels	
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit input capture	6 channels				8 channels	
	Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters×12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters×16 8-bit reload registers for L pulse width×16 8-bit reload registers for H pulse width×16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN interface	1 channel				3 channels	
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash memory	—					
Corresponding EVA name	MB90V340E-104		MB90V340E-103		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

3. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



4. Precautions for when not using a sub clock signal

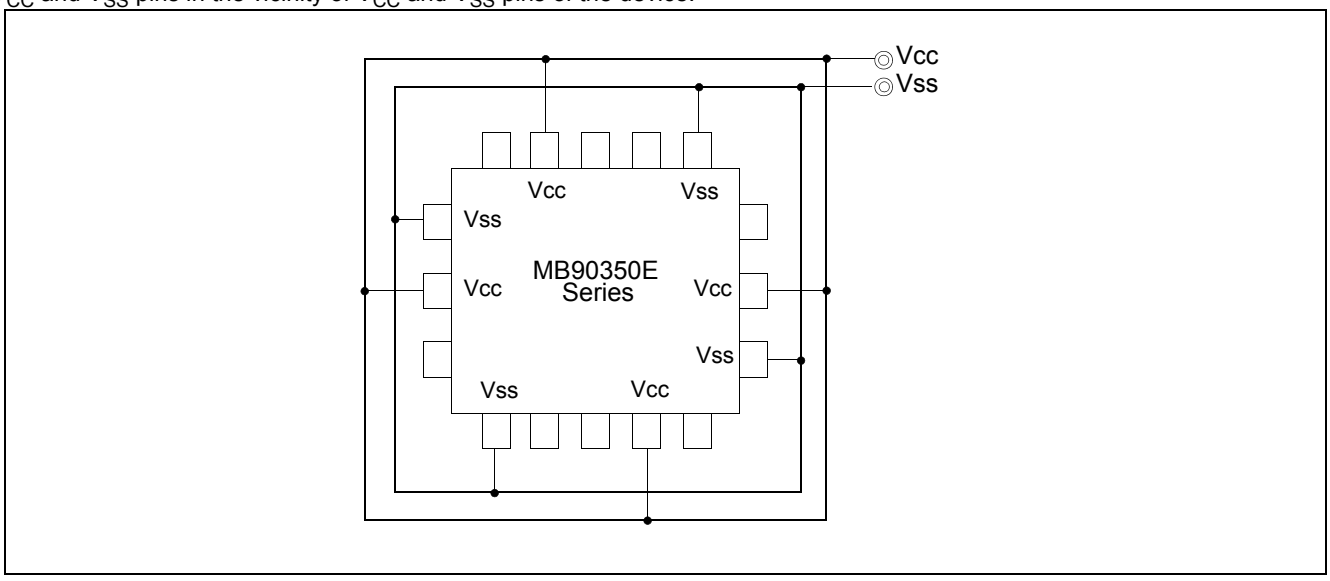
X0A and X1A are oscillation pins for sub clock. If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

5. Notes on during operation of PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Cypress will not guarantee results of operations if such failure occurs.

6. Treatment of Power Supply Pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
  Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.
- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



7. Pull-up/down resistors

The MB90350E series does not support internal pull-up/down resistors (Port 0 to Port 3: built-in pull-up resistors). Use external components where needed.

8. Crystal oscillator circuit

Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

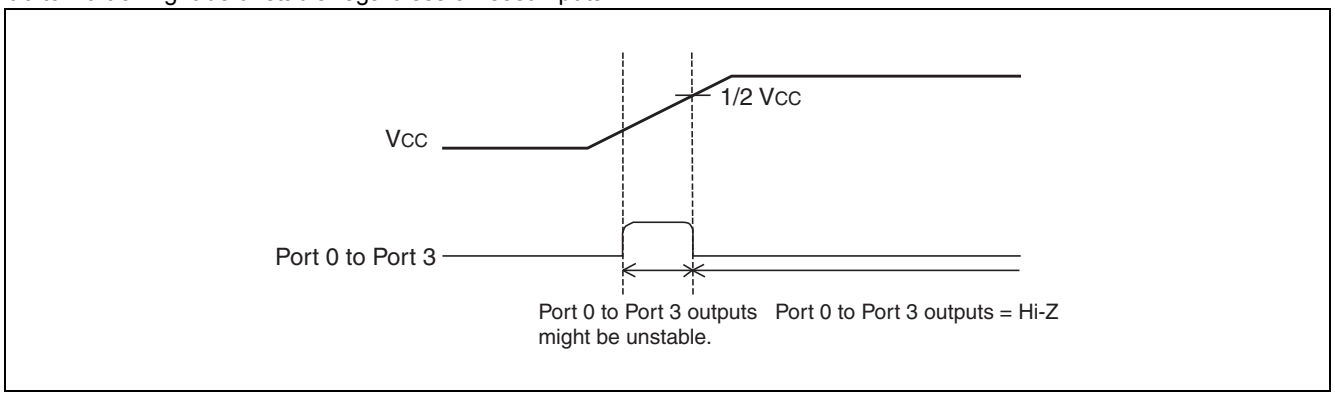
13. Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

14. Port 0 to port 3 output during power-on (External-bus mode)

As shown below, when power is turned on in external-bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable regardless of reset inputs.



15. Setting using CAN function

To use CAN function, please set “1” to DIRECT bit of CAN direct mode register (CDMR).

16. Flash security function

The security byte is located in the area of the Flash memory. If protection code 01_H is written in the security byte, the Flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Please refer to following table for the address of the security byte.

Product name	Flash memory size	Address for security bit
MB90F352E(S) MB90F352TE(S) MB90F357E(S) MB90F357TE(S)	Embedded 1 Mbit Flash memory	$FE0001_H$

17. Operation with T_A = +105°C or more

If used exceeding $T_A = +105°C$, please contact Cypress sales representatives for reliability limitations.

18. Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.
The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

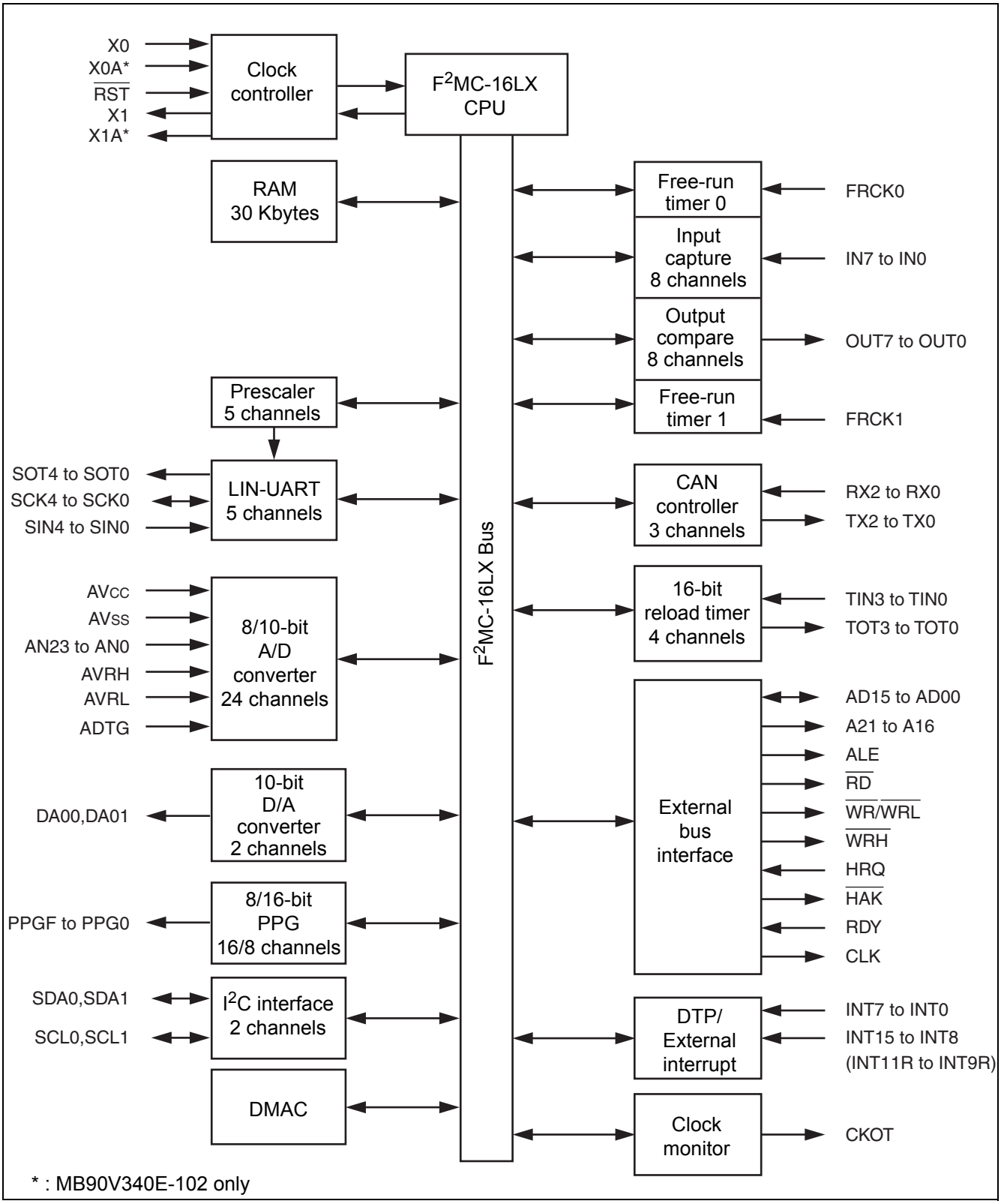
(1) Low voltage detection reset circuit

Detection voltage
4.0 V ± 0.3 V

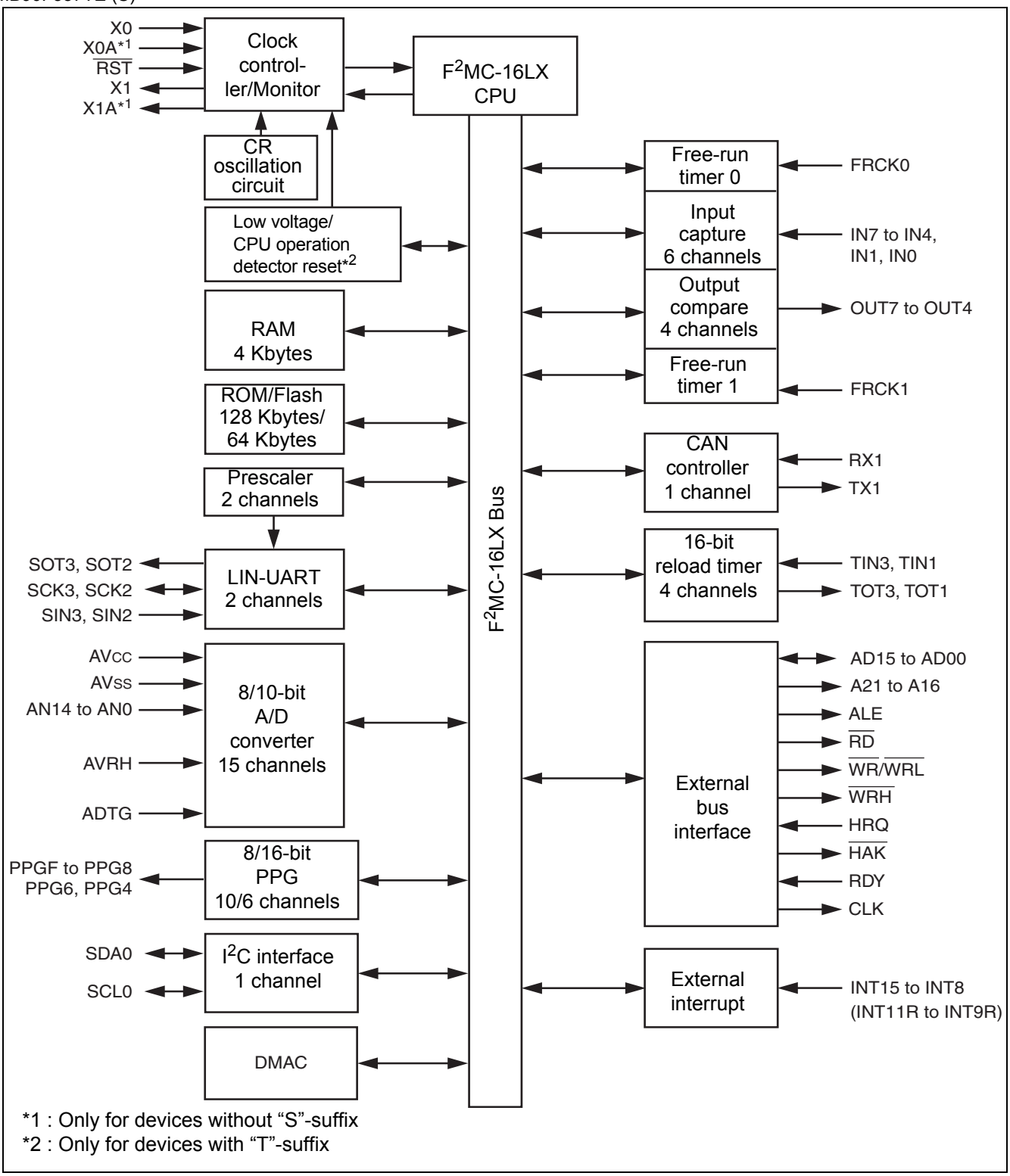
When a low voltage condition is detected, the low voltage detection flag (LVRC : LVRF) is set to “1” and an internal reset signal is output.
Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.

8. Block Diagrams

■ MB90V340E-101/102



■ MB90356E (S) , MB90356TE (S) , MB90F356E (S) , MB90F356TE (S) , MB90357E (S) , MB90357TE (S) , MB90F357E (S) , MB90F357TE (S)



Address	Register	Abbreviation	Access	Resource name	Initial value
$0000B9_H$	Interrupt Control Register 09	ICR09	W,R/W	Interrupt Control	00000111_B
$0000BA_H$	Interrupt Control Register 10	ICR10	W,R/W		00000111_B
$0000BB_H$	Interrupt Control Register 11	ICR11	W,R/W		00000111_B
$0000BC_H$	Interrupt Control Register 12	ICR12	W,R/W		00000111_B
$0000BD_H$	Interrupt Control Register 13	ICR13	W,R/W		00000111_B
$0000BE_H$	Interrupt Control Register 14	ICR14	W,R/W		00000111_B
$0000BF_H$	Interrupt Control Register 15	ICR15	W,R/W		00000111_B
$0000C0_H$ to $0000C9_H$	Reserved				
$0000CA_H$	External Interrupt Enable Register 1	ENIR1	R/W	External Interrupt 1	00000000_B
$0000CB_H$	External Interrupt Source Register 1	EIRR1	R/W		$XXXXXXXX_B$
$0000CC_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000_B
$0000CD_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000_B
$0000CE_H$	External Interrupt Source Select Register	EISSR	R/W		00000000_B
$0000CF_H$	PLL/Sub clock Control register	PSCCR	W	PLL	$XXXX0000_B$
$0000D0_H$	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	$XXXXXXXX_B$
$0000D1_H$	DMA Buffer Address Pointer M Register	BAPM	R/W		$XXXXXXXX_B$
$0000D2_H$	DMA Buffer Address Pointer H Register	BAPH	R/W		$XXXXXXXX_B$
$0000D3_H$	DMA Control Register	DMACS	R/W		$XXXXXXXX_B$
$0000D4_H$	I/O Register Address Pointer L Register	IOAL	R/W		$XXXXXXXX_B$
$0000D5_H$	I/O Register Address Pointer H Register	IOAH	R/W		$XXXXXXXX_B$
$0000D6_H$	Data Counter L Register	DCTL	R/W		$XXXXXXXX_B$
$0000D7_H$	Data Counter H Register	DCTH	R/W		$XXXXXXXX_B$
$0000D8_H$	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000_B
$0000D9_H$	Serial Control Register 2	SCR2	W,R/W		00000000_B
$0000DA_H$	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000_B
$0000DB_H$	Serial Status Register 2	SSR2	R,R/W		00001000_B
$0000DC_H$	Extended Communication Control Register 2	ECCR2	R,W, R/W		$000000XX_B$
$0000DD_H$	Extended Status/Control Register 2	ESCR2	R/W		00000100_B
$0000DE_H$	Baud Rate Generator Register 20	BGR20	R/W		00000000_B

(Continued)

(Continued)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007D00_H$	Control status register	CSR	R/W, W R/W, R	$0XXXX0X1_B$ $00XXX000_B$
$007D01_H$				
$007D02_H$	Last event indicator register	LEIR	R/W	$000X0000_B$ $XXXXXXXX_B$
$007D03_H$				
$007D04_H$	Receive/transmit error counter	RTEC	R	00000000_B 00000000_B
$007D05_H$				
$007D06_H$	Bit timing register	BTR	R/W	11111111_B $X1111111_B$
$007D07_H$				
$007D08_H$	IDE register	IDER	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D09_H$				
$007D0A_H$	Transmit RTR register	TRTRR	R/W	00000000_B 00000000_B
$007D0B_H$				
$007D0C_H$	Remote frame receive waiting register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D0D_H$				
$007D0E_H$	Transmit interrupt enable register	TIER	R/W	00000000_B 00000000_B
$007D0F_H$				
$007D10_H$	Acceptance mask select register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D11_H$				
$007D12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D13_H$				
$007D14_H$	Acceptance mask register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D15_H$				
$007D16_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D17_H$				
$007D18_H$	Acceptance mask register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D19_H$				
$007D1A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D1B_H$				

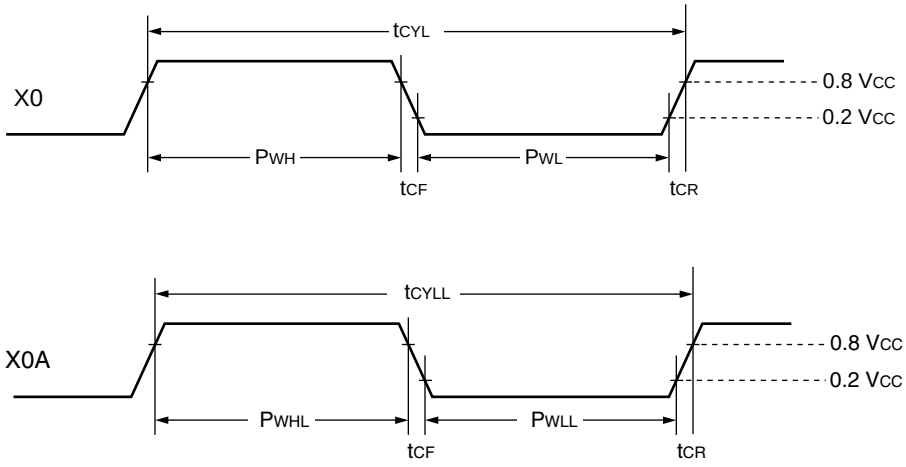
(Continued)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

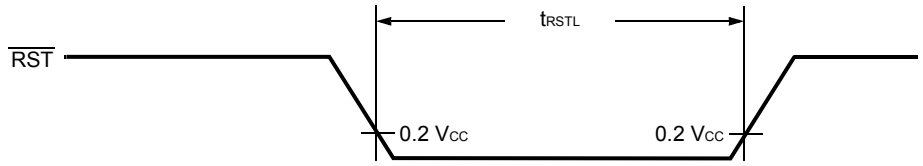
*: The limitation is in the range of the clock frequency when PLL is used. Use within the range in graph of "· PLL guaranteed operation range External clock frequency and internal operation clock frequency".

- Clock Timing

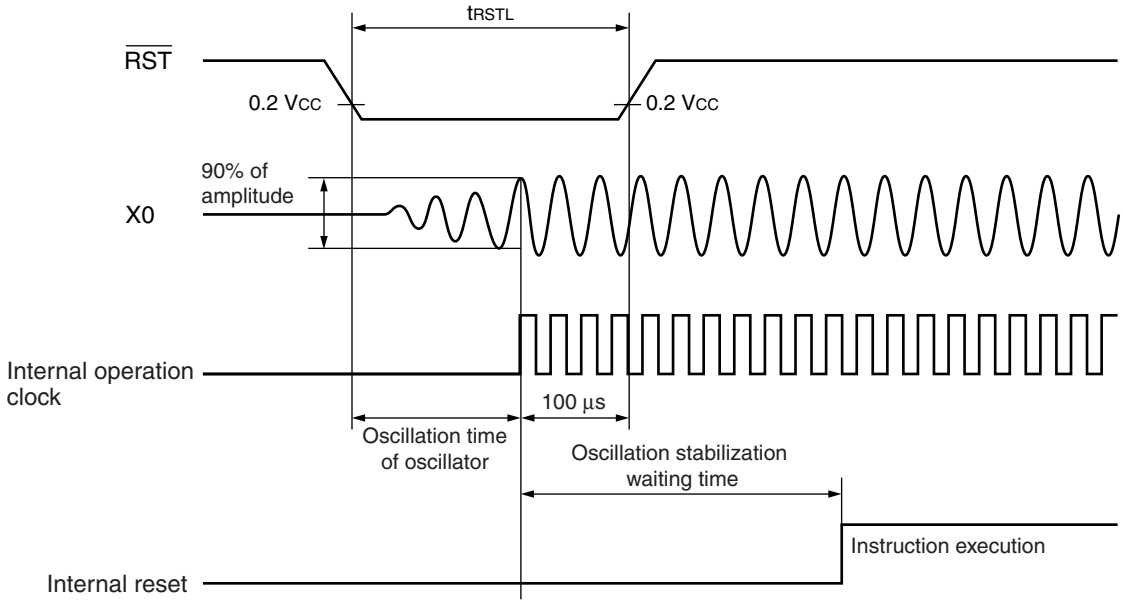


* : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillators, the oscillation time is between hundreds of μs to several ms. With an external clock, the oscillation time is 0 ms.

Under normal operation:



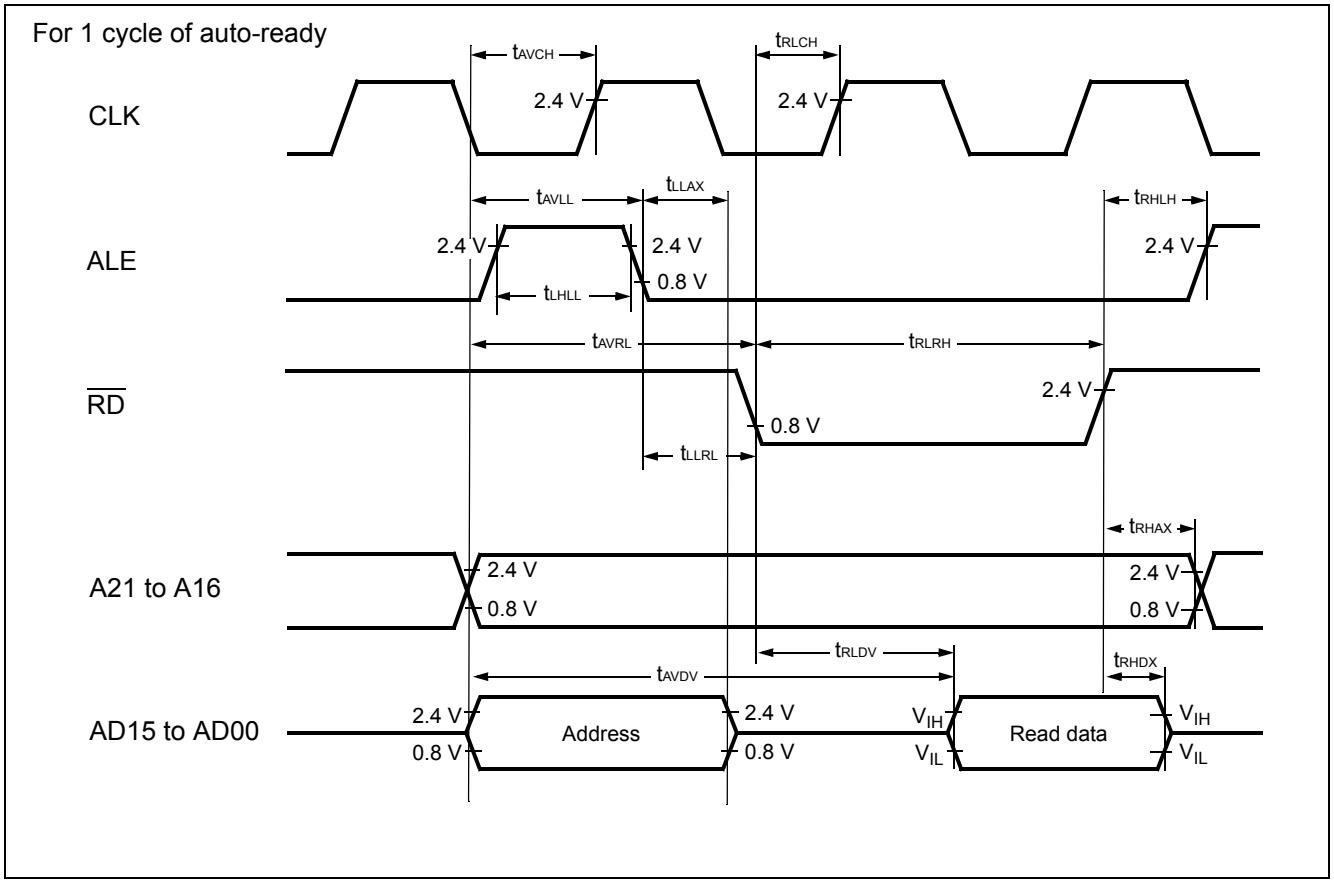
In Stop mode, Sub Clock mode, Sub Sleep mode and, Watch mode:



13.4.3 Power On Reset

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Waiting time until power-on

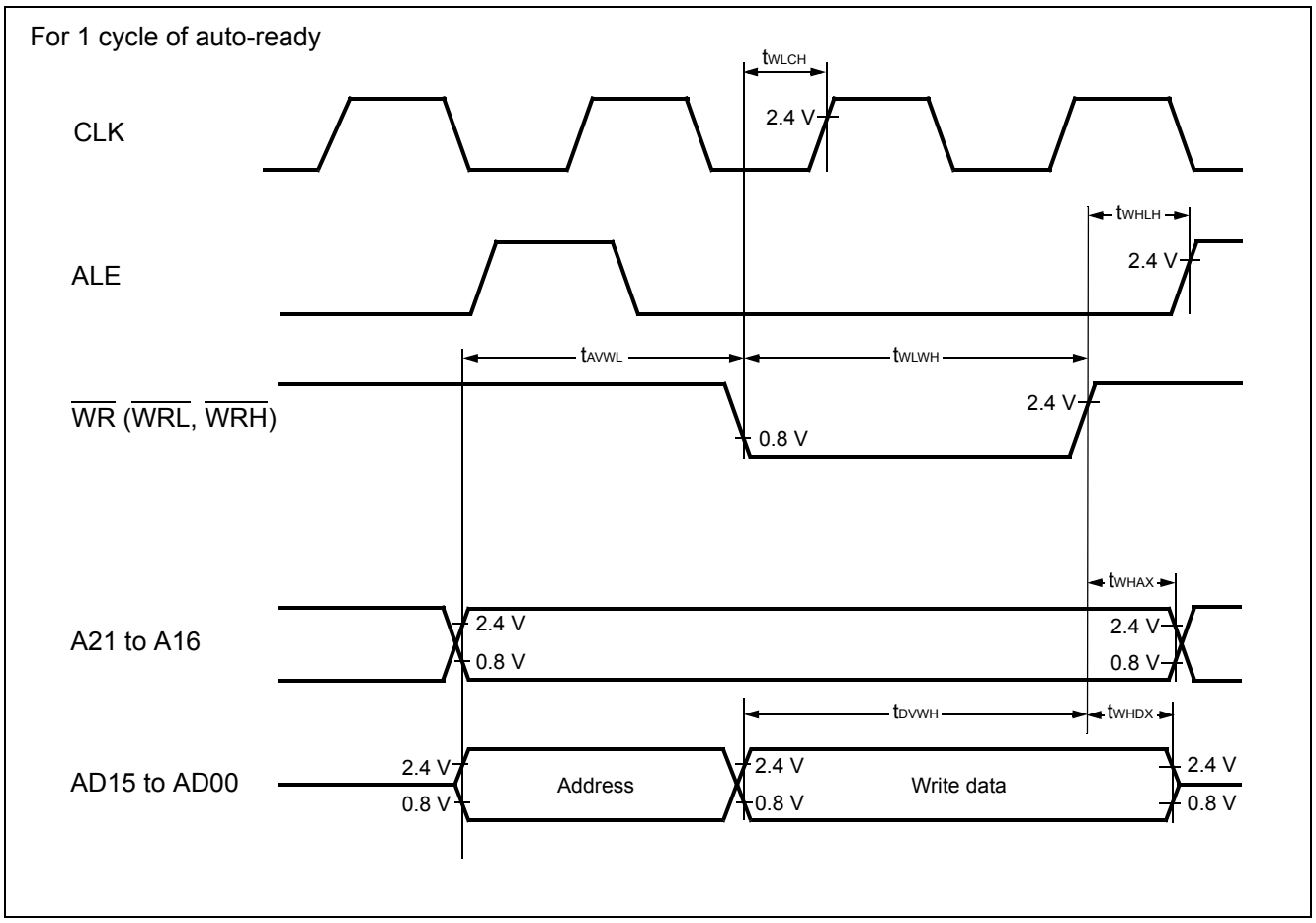

For 1 cycle of auto-ready
CLK
ALE
RD
A21 to A16
AD15 to AD00
tAVCH
tRLCH
2.4 V
tAVLL
tLLAX
tRHLH
0.8 V
tLHLL
tAVRL
tRLRH
tLLRL
tRHAX
tRLDV
tAVDV
tRHDX
Address
Read data
VIH
VIL

13.4.6 Bus Timing (Write)

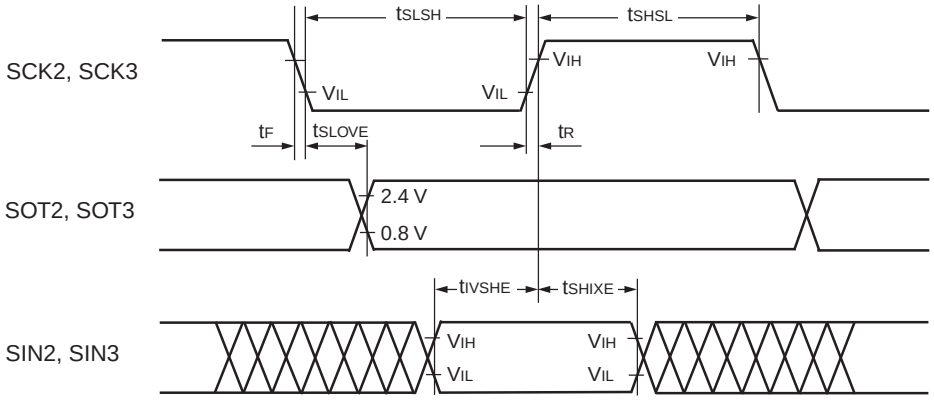
(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A21 to A16, AD15 to AD00, $\overline{WR}$	–	t_{CP}–15	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		(n*+3/2)t_{CP} – 20	–	ns
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		(n*+3/2)t_{CP} – 20	–	ns
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	–	ns
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A21 to A16, $\overline{WR}$		t_{CP}/2 – 10	–	ns
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	–	ns
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 15	–	ns

* : Number of ready cycles



●External Shift Clock Mode



■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

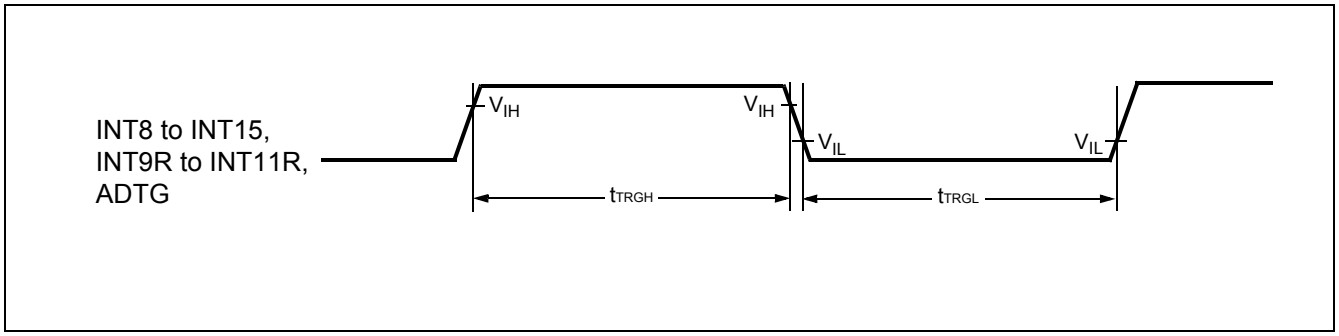
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal shift clock mode output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	–	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2, SCK3 SOT2, SOT3		−50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK2, SCK3 SIN2, SIN3		0	–	ns
Serial clock “H” pulse width	t_{SHSL}	SCK2, SCK3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	3 t_{CP} - t_R	–	ns
Serial clock “L” pulse width	t_{SLSH}	SCK2, SCK3		t_{CP} + 10	–	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK2, SCK3 SOT2, SOT3		–	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK2, SCK3 SIN2, SIN3		30	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 30	–	ns
SCK fall time	t_F	SCK2, SCK3		–	10	ns
SCK rise time	t_R	SCK2, SCK3		–	10	ns

Notes :
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

13.4.10 Trigger Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

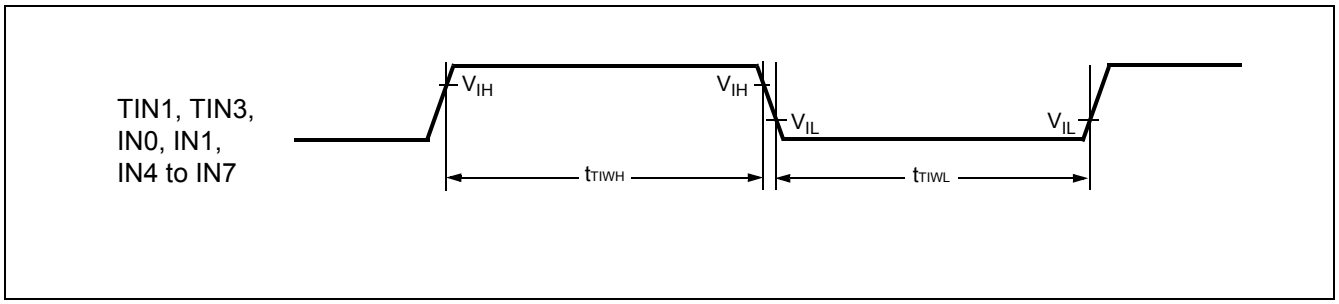
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	5 t_{CP}	—	ns



13.4.11 Timer Related Resource Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN1, TIN3,IN0, IN1, IN4 to IN7	—	4 t_{CP}	—	ns

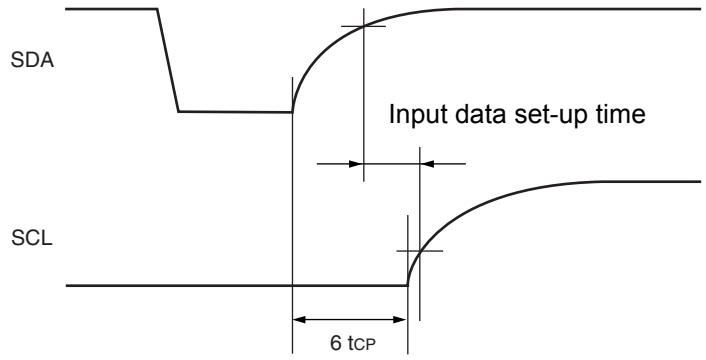


13.4.12 Timer Related Resource Output Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

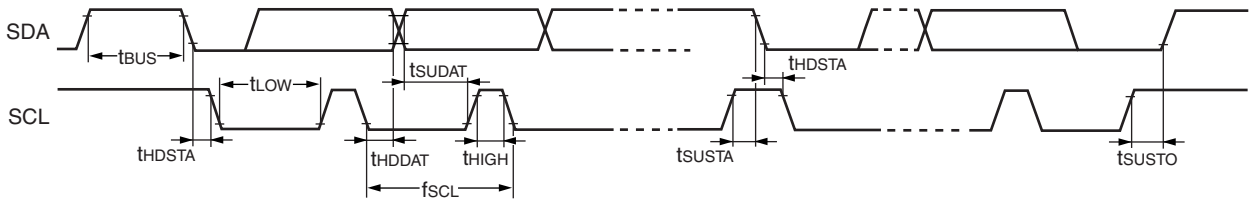
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT1, TOT3, PPG4, PPG6, PPG8 to PPGF	—	30	—	ns

• Note of SDA, SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition



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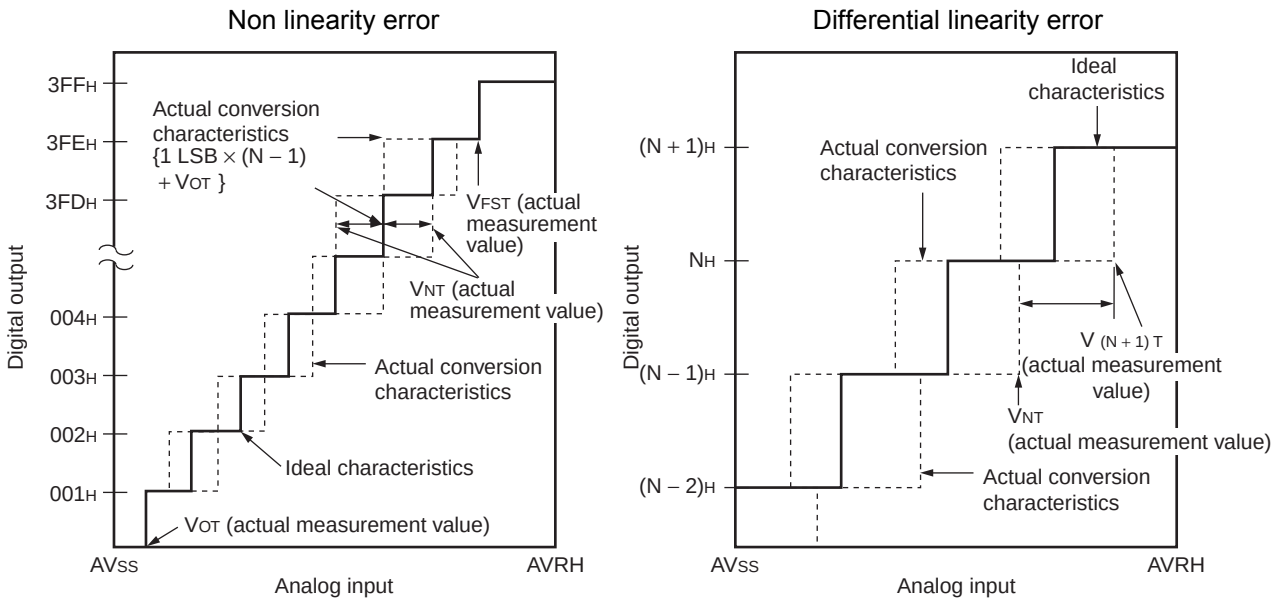


$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

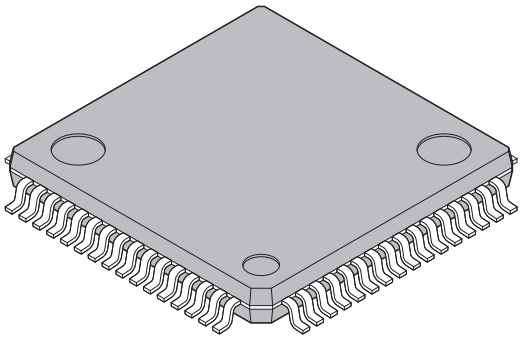
N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H".
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$".

13.7 Flash Memory Program/Erase Characteristics

■ Dual Operation Flash Memory

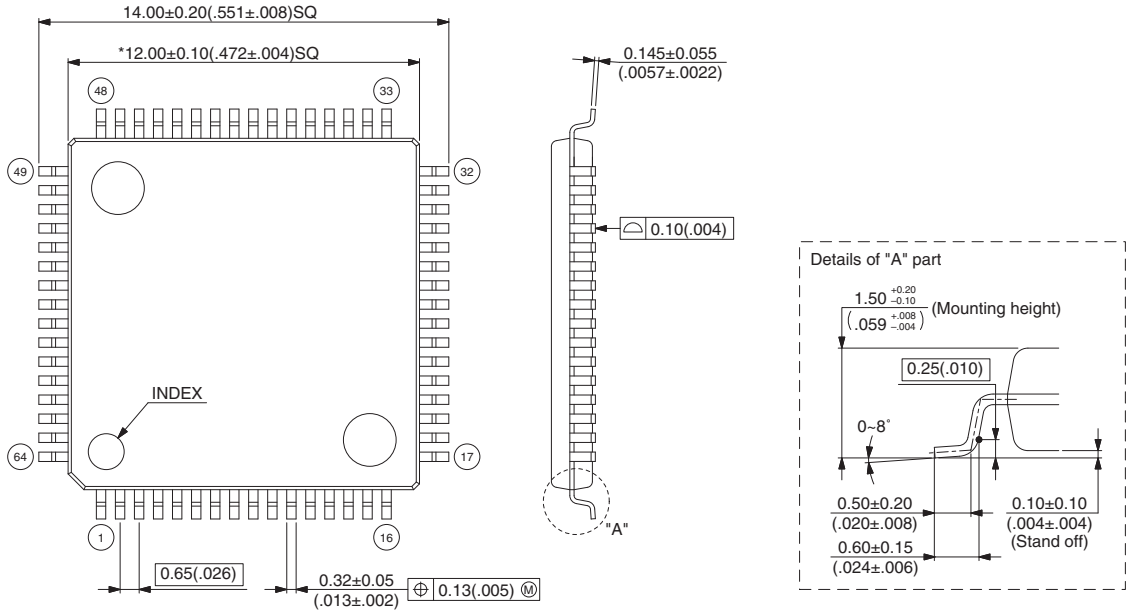
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T_A = +25°C V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10000	—	—	cycle	

14.1 Package Dimensions

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65
(FPT-64P-M23)		

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

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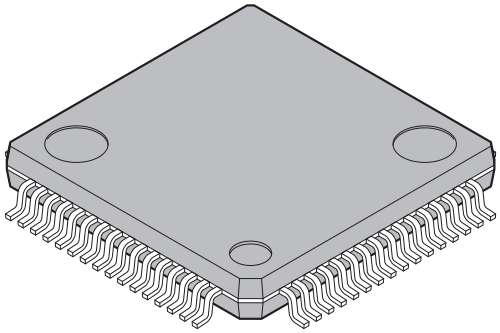
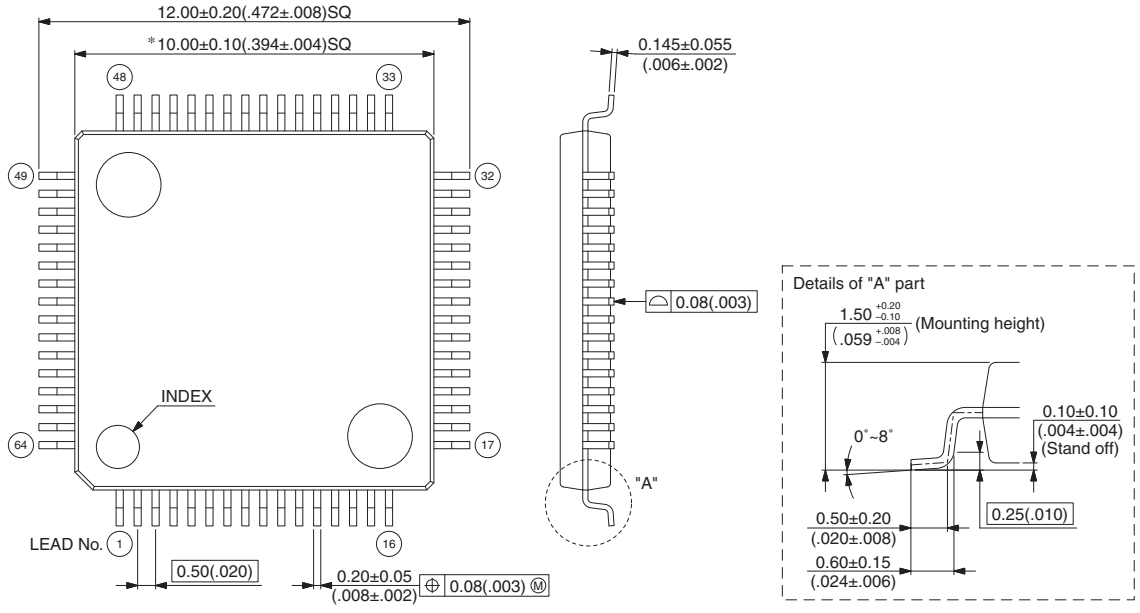
64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-64P-M24)	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values