Infineon Technologies - MB90F352TESPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352tespmc-gse1

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Parameter \ Part Number	MB90F356E MB90F357E	MB90F356TE MB90F357TE	MB90F356ES MB90F357ES	MB90F356TES MB90F357TES
16-bit input capture	6 channels			
	Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.			
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width×12 8-bit reload registers for H pulse width×12			
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN interface	1 channel			
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External interrupt	8 channels			
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.			
D/A converter	—			
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F357x only)			
Corresponding EVA name	MB90V340E-104		MB90V340E-103	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

■ MASK ROM products/Evaluation products

Parameter \ Part Number	MB90356E MB90357E	MB90356TE MB90357TE	MB90356ES MB90357ES	MB90356TES MB90357TES	MB90V340E-103	MB90V340E-104
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64 Kbytes :MB90356E(S), MB90356TE(S) 128 Kbytes :MB90357E(S), MB90357TE(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A)	Yes		No		No	Yes
Clock supervisor	Yes					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40°C to +125°C				—	
Package	LQFP-64				PGA-299	
LIN-UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 kbps)	1 channel				2 channels	
A/D converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit reload timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				Free-run Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. Free-run Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

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Parameter \ Part Number	MB90356E MB90357E	MB90356TE MB90357TE	MB90356ES MB90357ES	MB90356TES MB90357TES	MB90V340E-103	MB90V340E-104
16-bit output compare	4 channels				8 channels	
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit input capture	6 channels				8 channels	
	Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters×12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters×16 8-bit reload registers for L pulse width×16 8-bit reload registers for H pulse width×16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN interface	1 channel				3 channels	
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash memory	—					
Corresponding EVA name	MB90V340E-104		MB90V340E-103		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

Pin No.	Pin name	I/O Circuit type*	Function
39	P17	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD15		Input/output pin for external bus address data bus bit 15. This function is enabled when external bus is enabled.
40 to 43	P20 to P23	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pins are enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A16 to A19		Output pins for A16 to A19 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins A16 to A19.
	PPG9 (8) PPGB (A) PPGD (C) PPGF (E)		Output pins for PPGs
44	P24	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A20		Output pin for A20 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A20.
	IN0		Data sample input pin for input capture ICU0
51	P25	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A21		Output pin for A21 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A21.
	IN1		Data sample input pin for input capture ICU1
	ADTG		Trigger input pin for A/D converter
52	P44	H	General purpose I/O port
	SDA0		Serial data I/O pin for I^2C 0
	FRCK0		Input pin for the 16-bit Free-run Timer 0
53	P45	H	General purpose I/O port
	SCL0		Serial clock I/O pin for I^2C 0
	FRCK1		Input pin for the 16-bit Free-run Timer 1

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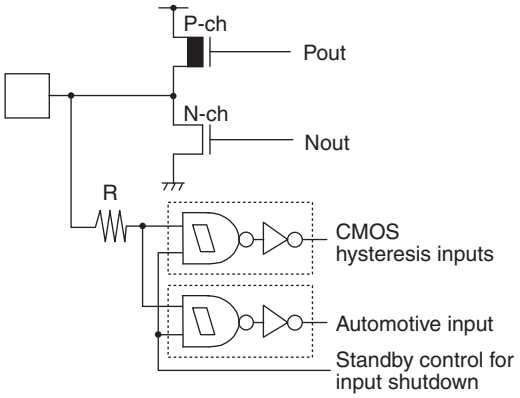
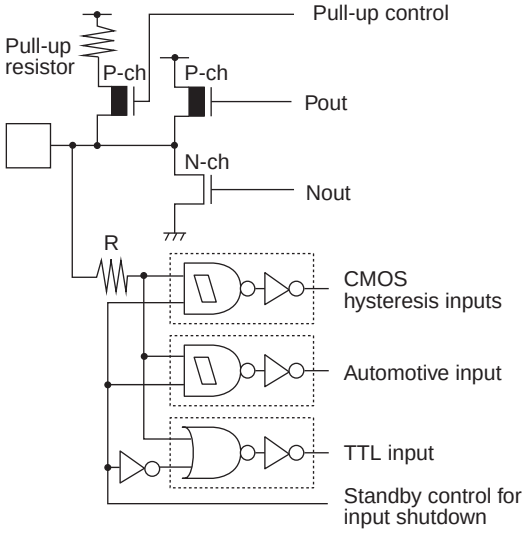
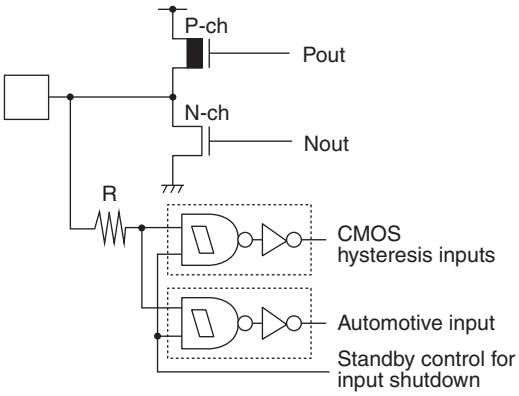
Pin No.	Pin name	I/O Circuit type*	Function
61	P37	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the CLK output disabled.
	CLK		CLK output pin. This function is enabled when both the external bus and CLK output are enabled.
	OUT7		Wave form output pin for output compare OCU7
62, 63	P60, P61	I	General purpose I/O ports
	AN0, AN1		Analog input pins for A/D converter
64	AV_{CC}	K	V_{CC} power input pin for analog circuits
2	AVRH	L	Reference voltage input for the A/D converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
1	AV_{SS}	K	V_{SS} power input pin for analog circuits
22, 23	MD1, MD0	C	Input pins for specifying the operating mode
21	MD2	D	Input pin for specifying the operating mode
49	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
18, 48	V_{SS}	—	Power (0 V) input pins
50	C	K	This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 μF ceramic capacitor.

* : For the I/O circuit type, refer to “I/O Circuit Type”.

Type	Circuit	Remarks
F		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS hysteresis inputs (With input shutdown function when is standby) ■ Automotive input (With the standby-time input shutdown function)
G		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ TTL input (With the standby-time input shutdown function) ■ Programmable pull-up resistor: approx. 50 kΩ
H		■ CMOS level output (I_{OL} = 3 mA, I_{OH} = −3 mA) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function)

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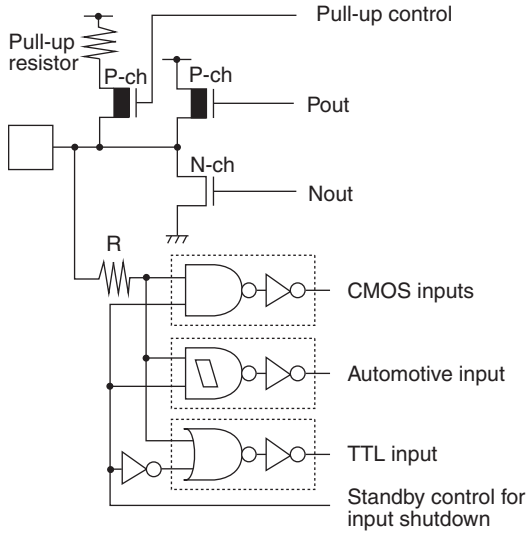
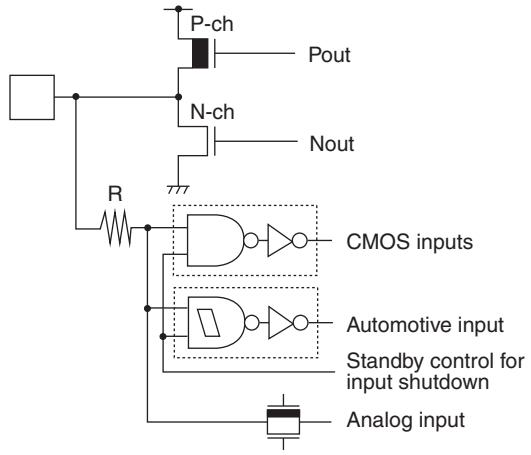
Type	Circuit	Remarks
N		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ TTL input (With the standby-time input shutdown function) ■ Programmable pull-up resistor: approx. 50 kΩ
O		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ Analog input for A/D converter

7. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions :

■A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.

■A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.

■The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

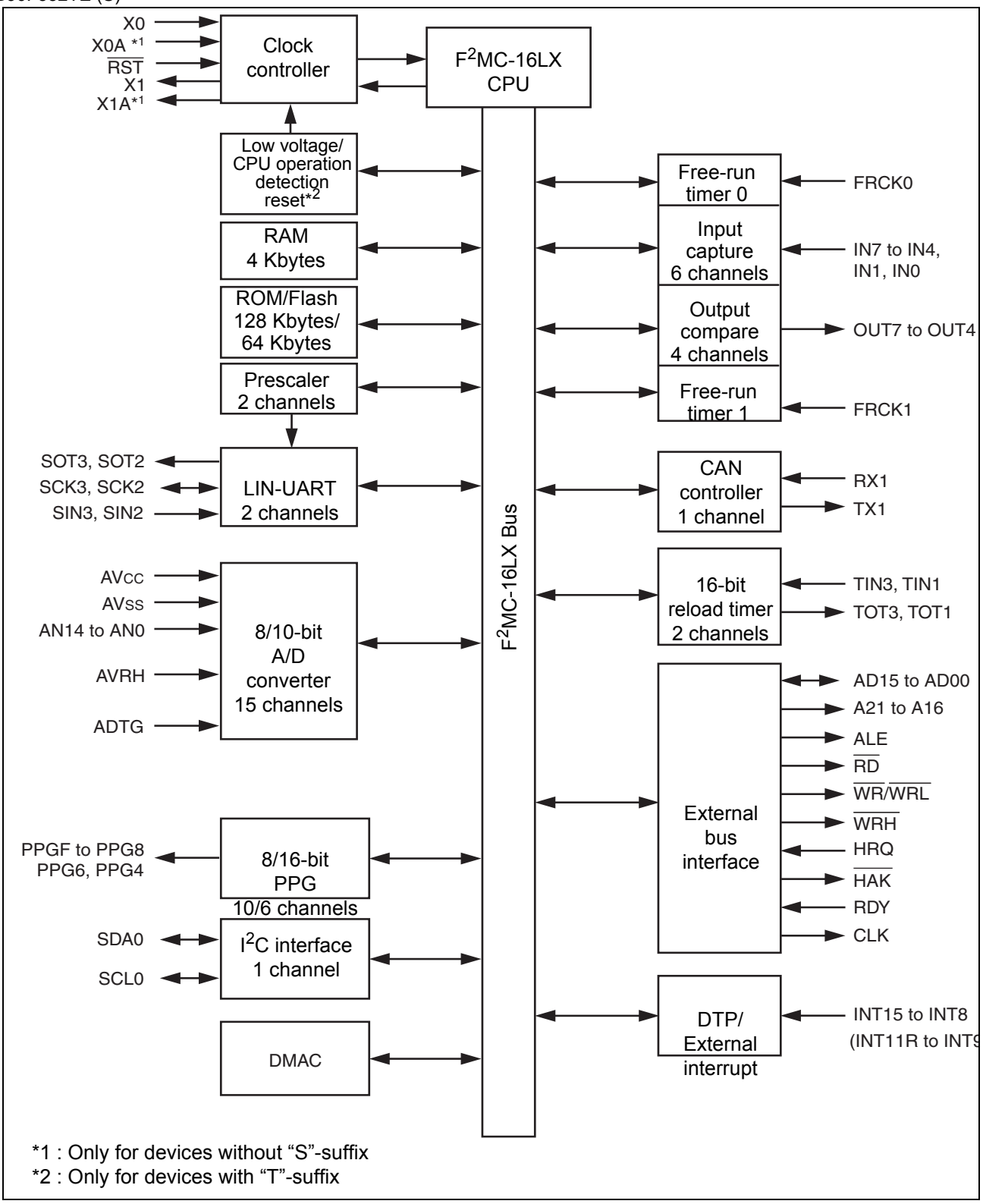
For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage (V_{CC}) .

2. Treatment of unused pins

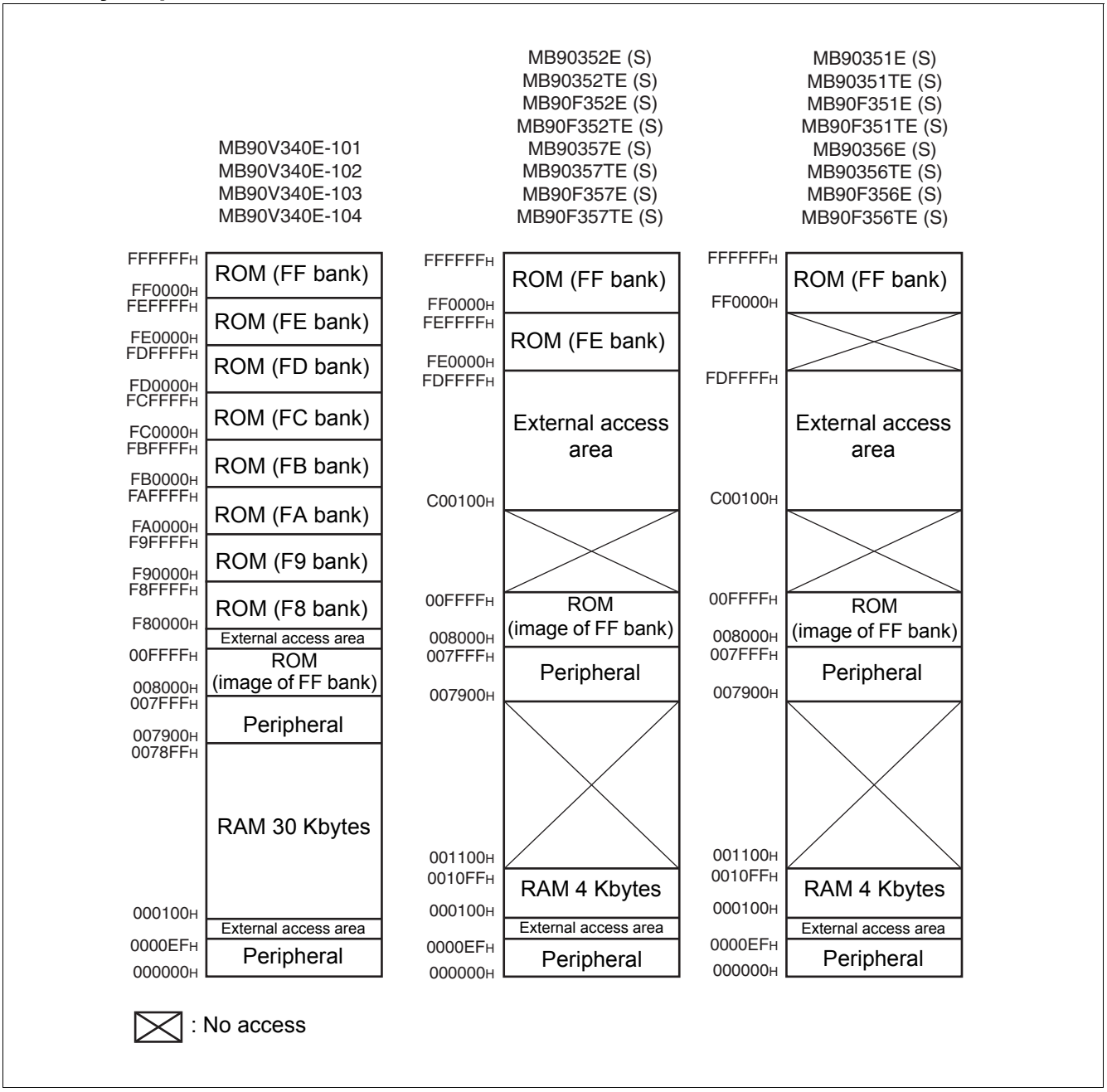
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

Unused I/O pins should be set to the output state and can be left open, or the input state with the above described connection.

■ MB90351E (S) , MB90351TE (S) , MB90F351E (S) , MB90F351TE (S) , MB90352E (S) , MB90352TE (S) , MB90F352E (S) MB90F352TE (S)



9. Memory Map



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access $00C000_H$ practically accesses the value at $FFC000_H$ in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

10. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
000000_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
000001_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
000002_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
000003_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
000004_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
000005_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
000006_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
000007_H to $00000A_H$	Reserved				
$00000B_H$	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111_B
$00000C_H$	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111_B
$00000D_H$	Reserved				
$00000E_H$	Input Level Select Register 0	ILSR0	R/W	Ports	00000000_B
$00000F_H$	Input Level Select Register 1	ILSR1	R/W	Ports	00000000_B
000010_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
000011_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
000012_H	Port 2 Direction Register	DDR2	R/W	Port 2	$XX000000_B$
000013_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
000014_H	Port 4 Direction Register	DDR4	R/W	Port 4	$XX000000_B$
000015_H	Port 5 Direction Register	DDR5	R/W	Port 5	$X0000000_B$
000016_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
000017_H to 000019_H	Reserved				
$00001A_H$	SIN input Level Setting Register	DDRA	W	UART2, UART3	$X00XXXXX_B$
$00001B_H$	Reserved				
$00001C_H$	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000_B
$00001D_H$	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000_B
$00001E_H$	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000_B
$00001F_H$	Port 3 Pull-up Control Register	PUCR3	R/W	Port 3	00000000_B
000020_H to 000037_H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007950_H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000_B
007951_H	Serial Control Register 3	SCR3	W, R/W		00000000_B
007952_H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000_B
007953_H	Serial Status Register 3	SSR3	R,R/W		00001000_B
007954_H	Extended Communication Control Register 3	ECCR3	R,W, R/W		$000000XX_B$
007955_H	Extended Status Control Register 3	ESCR3	R/W		00000100_B
007956_H	Baud Rate Generator Register 30	BGR30	R/W		00000000_B
007957_H	Baud Rate Generator Register 31	BGR31	R/W		00000000_B
007958_H, 007959_H	Reserved				
007960_H	Clock supervisor Control Register	CSVCR	R, R/W	Clock Supervisor	00011100_B
007961_H to $00796D_H$	Reserved				
$00796E_H$	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	$XXXXXXX0_B$
$00796F_H$	Reserved				
007970_H	I^2C Bus Status Register 0	IBSR0	R	I^2C Interface 0	00000000_B
007971_H	I^2C Bus Control Register 0	IBCR0	W,R/W		00000000_B
007972_H	I^2C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000_B
007973_H		ITBAH0	R/W		00000000_B
007974_H	I^2C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111_B
007975_H		ITMKH0	R/W		00111111_B
007976_H	I^2C 7-bit Slave Address Register 0	ISBA0	R/W		00000000_B
007977_H	I^2C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111_B
007978_H	I^2C data register 0	IDAR0	R/W		00000000_B
007979_H, $00797A_H$	Reserved				
$00797B_H$	I^2C Clock Control Register 0	ICCR0	R/W	I^2C Interface 0	00011111_B
$00797C_H$ to $0079A1_H$	Reserved				
$0079A2_H$	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000_B
$0079A3_H$	Flash Write Control Register 1	FWR1	R/W		00000000_B
$0079A4_H$	Sector Change Setting Register 0	SSR0	R/W		$00XXXXX0_B$
$0079A5_H$ to $0079C1_H$	Reserved				
$0079C2_H$	Clock modulator Control Register	CMCR	R, R/W	Clock Modulator	$0001X000_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
$0079C3_H$ to $0079DF_H$	Reserved				
$0079E0_H$	Detect Address Setting Register 0	PADR0	R/W	Address Match Detection 0	$XXXXXXXX_B$
$0079E1_H$	Detect Address Setting Register 0	PADR0	R/W		$XXXXXXXX_B$
$0079E2_H$	Detect Address Setting Register 0	PADR0	R/W		$XXXXXXXX_B$
$0079E3_H$	Detect Address Setting Register 1	PADR1	R/W		$XXXXXXXX_B$
$0079E4_H$	Detect Address Setting Register 1	PADR1	R/W		$XXXXXXXX_B$
$0079E5_H$	Detect Address Setting Register 1	PADR1	R/W		$XXXXXXXX_B$
$0079E6_H$	Detect Address Setting Register 2	PADR2	R/W		$XXXXXXXX_B$
$0079E7_H$	Detect Address Setting Register 2	PADR2	R/W		$XXXXXXXX_B$
$0079E8_H$	Detect Address Setting Register 2	PADR2	R/W		$XXXXXXXX_B$
$0079E9_H$ to $0079EF_H$	Reserved				
$0079F0_H$	Detect Address Setting Register 3	PADR3	R/W	Address Match Detection 1	$XXXXXXXX_B$
$0079F1_H$	Detect Address Setting Register 3	PADR3	R/W		$XXXXXXXX_B$
$0079F2_H$	Detect Address Setting Register 3	PADR3	R/W		$XXXXXXXX_B$
$0079F3_H$	Detect Address Setting Register 4	PADR4	R/W		$XXXXXXXX_B$
$0079F4_H$	Detect Address Setting Register 4	PADR4	R/W		$XXXXXXXX_B$
$0079F5_H$	Detect Address Setting Register 4	PADR4	R/W		$XXXXXXXX_B$
$0079F6_H$	Detect Address Setting Register 5	PADR5	R/W		$XXXXXXXX_B$
$0079F7_H$	Detect Address Setting Register 5	PADR5	R/W		$XXXXXXXX_B$
$0079F8_H$	Detect Address Setting Register 5	PADR5	R/W		$XXXXXXXX_B$
$0079F9_H$ to $007BFF_H$	Reserved				
$007C00_H$ to $007DFF_H$	Reserved for CAN controller 1. Refer to “CAN Controllers”				
$007E00_H$ to $007FFF_H$	Reserved				

Notes : ″ Initial value of “X” represents unknown value.
″ Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results reading unknown value.

11. CAN Controllers

■ Compliant with CAN standard Version2.0 Part A and Part B
- Supports tr12ansmission/reception in standard frame and extended frame formats

■ Supports transmitting of data frames by receiving remote frames

■ 16 transmitting/receiving message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration

■ Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats

■ Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

12. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI^{2}OS corresponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
Reserved	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
Reserved	N	—	#12	FFFFCC$_H$		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4$_H$		
I^{2}C	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Reserved	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG 4/5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG 6/7	N	—	#22	FFFFA4$_H$		
PPG 8/9/C/D	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N	—	#24	FFFF9C$_H$		
Timebase Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
Free-run Timer 0 / free-run Timer 1	N	—	#30	FFFF84$_H$		
Input Capture 4/5	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0/1	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 6/7	Y1	9	#34	FFFF74$_H$		
Reserved	N	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
Reserved	N	11	#36	FFFF6C$_H$		
UART 3 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 3 TX	Y1	13	#38	FFFF64$_H$		

(Continued)

13.3 DC Characteristics

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Pin inputs if TTL input levels are selected
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{IHI}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} − 0.3	—	V_{CC} + 0.3	V	MD input pin
"L" level input voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{ILA}	—	—	V_{SS} − 0.3	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected
	V_{ILT}	—	—	V_{SS} − 0.3	—	0.8	V	Pin inputs if TTL input levels are selected
	V_{ILS}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{ILI}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} − 0.3	—	V_{SS} + 0.3	V	MD input pin
Output "H" voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	V_{CC} − 0.5	—	—	V	
Output "H" voltage	V_{OHI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OH} = −3.0 mA	V_{CC} − 0.5	—	—	V	

(Continued)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCL}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub clock operation T_A = +25°C	—	70	140	µA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub clock operation T_A = +25°C	—	100	200	µA	MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T_A = +25°C	—	100	200	µA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub clock operation T_A = +25°C	—	120	240	µA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub clock operation T_A = +25°C	—	150	300	µA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T_A = +25°C	—	150	300	µA	MB90356TES MB90F356TES MB90357TES MB90F357TES

(Continued)

13.4.9 LIN-UART2/3

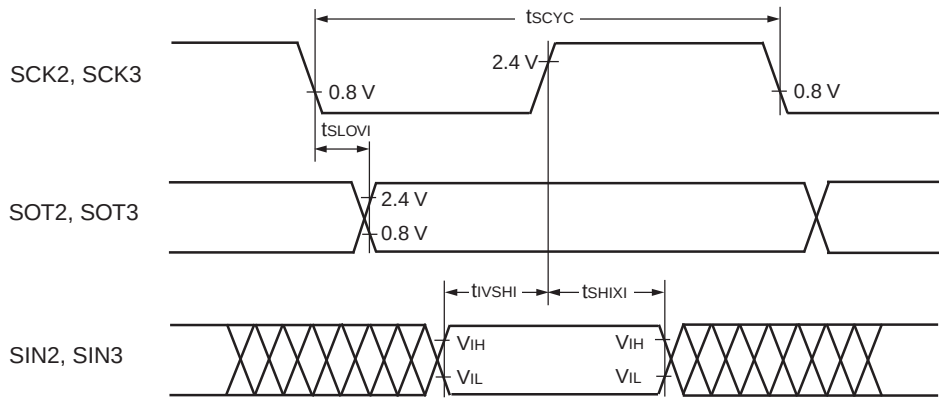
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

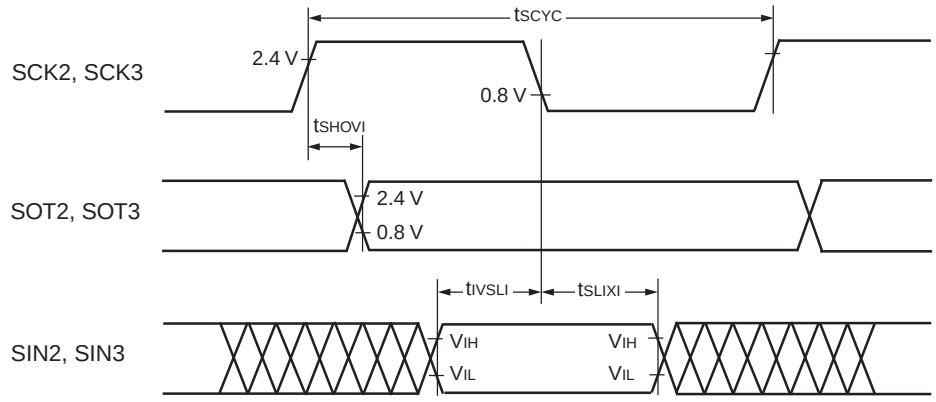
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal shift clock mode output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2, SCK3 SOT2, SOT3		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK2, SCK3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK2, SCK3		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK2, SCK3 SOT2, SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK2, SCK3 SIN2, SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK2, SCK3		—	10	ns
SCK rise time	t_R	SCK2, SCK3		—	10	ns

Notes :
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

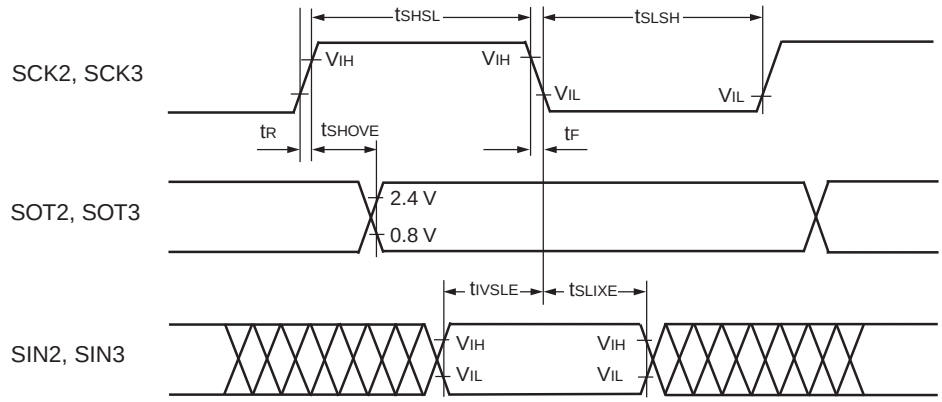
″ Internal Shift Clock Mode



• Internal Shift Clock Mode



• External Shift Clock Mode



■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal clock operation output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2, SCK3 SOT2, SOT3		–50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK2, SCK3 SOT2, SOT3		3 t_{CP} – 70	—	ns

Notes : • C_L is load capacity value of pins when testing.
• t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

13.5 A/D Converter

(T_A = −40°C to +125°C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	AV_{SS} − 1.5×LSB	AV_{SS} + 0.5×LSB	AV_{SS} + 2.5×LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN14	AVRH − 3.5×LSB	AVRH − 1.5×LSB	AVRH + 0.5×LSB	V	
Compare time	—	—	1.0	—	16500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			2.0				4.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	×	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			1.2				4.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN14	− 0.3	—	+ 0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AV_{SS}	—	AVRH	V	
Reference voltage range	—	AVRH	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between channels	—	AN0 to AN14	—	—	4	LSB	

* : If A/D converter is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Notes on A/D Converter Section

■ About the external impedance of the analog input and its sampling time

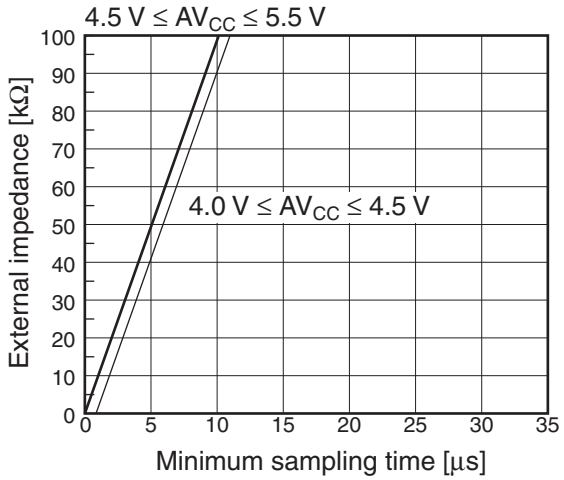
A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting
A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

■ MASK ROM device

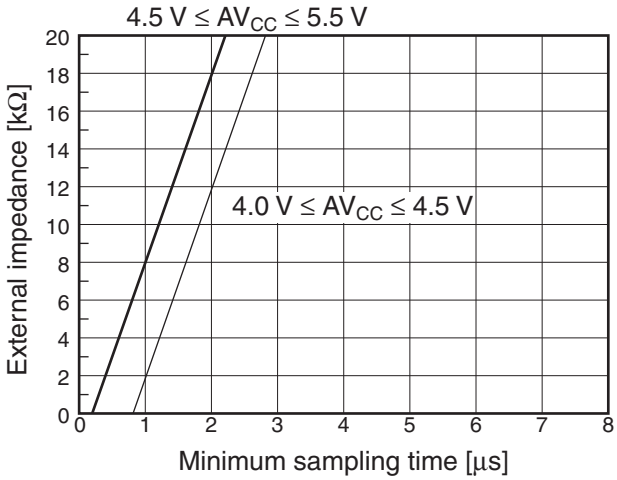
· Relation between External impedance and minimum sampling time

(MB90351E(S),MB90351TE(S),MB90352E(S),MB90352TE(S),MB90356E(S), MB90356TE(S),MB90357E(S),MB90357TE(S),MB90V340E-101/102/103/104)

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20kΩ]



■ About the error

Values of relative errors grow larger, as |AVRH − AV_{SS}| becomes smaller.

(Continued)

Part number	Package	Remarks
MB90F351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	Flash memory products (64 Kbytes)
MB90F351ESPMC1		
MB90F351TEPMC1		
MB90F351TESPMC1		
MB90F356EPMC1		
MB90F356ESPMC1		
MB90F356TEPMC1		
MB90F356TESPMC1		
MB90F352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ESPMC1		
MB90F352TEPMC1		
MB90F352TESPMC1		
MB90F357EPMC1		
MB90F357ESPMC1		
MB90F357TEPMC1		
MB90F357TESPMC1		
MB90351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	MASK ROM products (64 Kbytes)
MB90351ESPMC1		
MB90351TEPMC1		
MB90351TESPMC1		
MB90356EPMC1		
MB90356ESPMC1		
MB90356TEPMC1		
MB90356TESPMC1		
MB90352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	MASK ROM products (128 Kbytes)
MB90352ESPMC1		
MB90352TEPMC1		
MB90352TESPMC1		
MB90357EPMC1		
MB90357ESPMC1		
MB90357TEPMC1		
MB90357TESPMC1		
MB90V340E-101CR	299-pin ceramic PGA PGA-299C-A01	Device for evaluation
MB90V340E-102CR		
MB90V340E-103CR		
MB90V340E-104CR		