Infineon Technologies - MB90F356TESPMC1-GE1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f356tespmc1-ge1

Contents

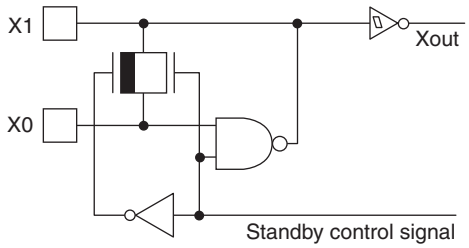
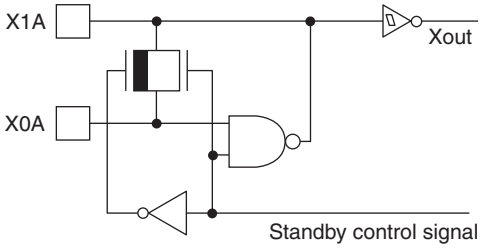
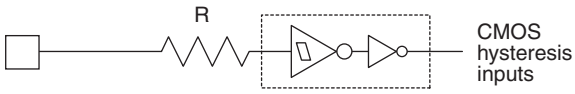
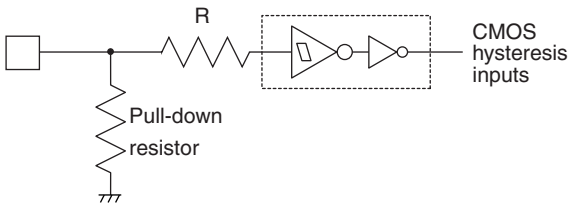
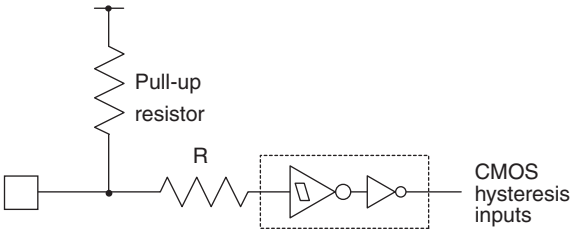
1. Product Lineup1 (Without Clock supervisor function)

■ Flash memory products

Parameter \ Part Number	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
Type	Flash memory products			
CPU	F^2MC-16LX CPU			
System clock	PLL clock multiplication circuit (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	64 Kbytes Flash memory : MB90F351E(S), MB90F351TE(S) 128 Kbytes Dual operation Flash memory (Erase/write and read can be operated at the same time) : MB90F352E(S), MB90F352TE(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No	
Clock supervisor	No			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus			
Operating temperature	−40°C to +125°C			
Package	LQFP-64			
LIN-UART	2 channels			
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	1 channel			
A/D converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit reload timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit Free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)			
16-bit output compare	4 channels			
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

(Continued)

6. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM device CMOS hysteresis input pin ■ Flash memory device CMOS input pin
D		■ MASK ROM device CMOS hysteresis input pin Pull-down resistor value: approx. 50 kΩ ■ Flash memory device CMOS input pin No Pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

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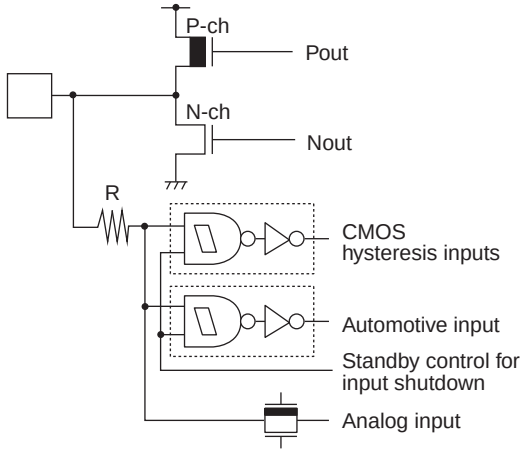
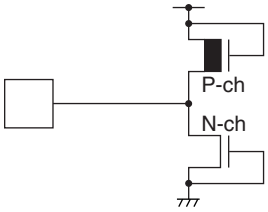
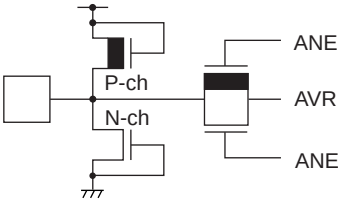
Type	Circuit	Remarks
I		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ Analog input for A/D converter
K		Protection circuit for power supply input
L		■ With the protection circuit of A/D converter reference voltage power input pin ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH.

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During an internal RAM write cycle, low voltage reset is generated after the completion of writing. During the output of this internal reset, the reset output from the low voltage detection reset circuit is suppressed.

(2) CPU operation detection reset circuit

The CPU operation detection reset circuit is a counter that prevents program runaway. The counter starts automatically after a power-on reset, and must be continually and regularly cleared within a given time. If the given time interval elapses and the counter has not been cleared, a cause such as infinite program looping is assumed and an internal reset signal is generated. The internal reset generated from the CPU operation detection circuit has a width of 5 machine cycles.

Interval time
$2^{20}/F_C$ (approx. 262 ms*)

* : This value assumes the interval time at an oscillation clock frequency of 4 MHz.
During recovery from standby mode, the detection period is the maximum interval plus 20 μs.

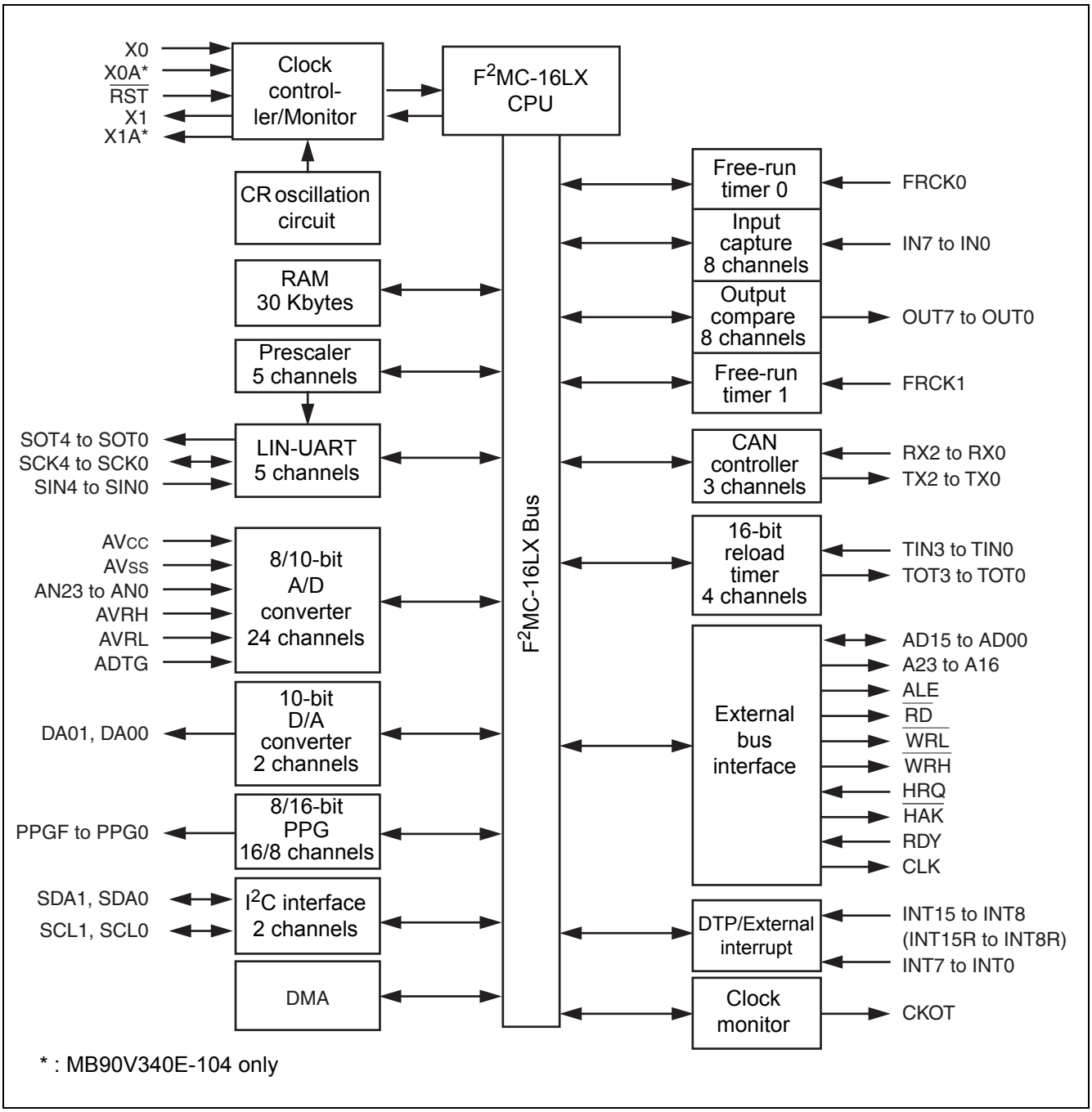
This circuit does not operate in modes where CPU operation is stopped.
The CPU operation detection reset circuit counter is cleared under any of the following conditions.

- ■“0” writing to CL bit of LVRC register
- ■Internal reset
- ■Main oscillation clock stop
- ■Transit to sleep mode
- ■Transit to timebase timer mode and watch mode

19. Internal CR oscillation circuit

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Oscillation frequency	f_{RC}	50	100	200	kHz
Oscillation stabilization wait time	tstab	—	—	100	μs

■ MB90V340E-103/104



List of Control Registers

Address CAN1	Register	Abbreviation	Access	Initial Value
000080_H	Message buffer enable register	BVALR	R/W	00000000_B 00000000_B
000081_H				
000082_H	Transmit request register	TREQR	R/W	00000000_B 00000000_B
000083_H				
000084_H	Transmit cancel register	TCANR	W	00000000_B 00000000_B
000085_H				
000086_H	Transmission complete register	TCR	R/W	00000000_B 00000000_B
000087_H				
000088_H	Receive complete register	RCR	R/W	00000000_B 00000000_B
000089_H				
$00008A_H$	Remote request receiving register	RRTRR	R/W	00000000_B 00000000_B
$00008B_H$				
$00008C_H$	Receive overrun register	ROVRR	R/W	00000000_B 00000000_B
$00008D_H$				
$00008E_H$	Reception interrupt enable register	RIER	R/W	00000000_B 00000000_B
$00008F_H$				

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List of Message Buffers (DLC Registers and Data Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C60_H$	DLC register 0	DLCR0	R/W	$XXXXXXXX_B$
$007C61_H$				
$007C62_H$	DLC register 1	DLCR1	R/W	$XXXXXXXX_B$
$007C63_H$				
$007C64_H$	DLC register 2	DLCR2	R/W	$XXXXXXXX_B$
$007C65_H$				
$007C66_H$	DLC register 3	DLCR3	R/W	$XXXXXXXX_B$
$007C67_H$				
$007C68_H$	DLC register 4	DLCR4	R/W	$XXXXXXXX_B$
$007C69_H$				
$007C6A_H$	DLC register 5	DLCR5	R/W	$XXXXXXXX_B$
$007C6B_H$				
$007C6C_H$	DLC register 6	DLCR6	R/W	$XXXXXXXX_B$
$007C6D_H$				
$007C6E_H$	DLC register 7	DLCR7	R/W	$XXXXXXXX_B$
$007C6F_H$				
$007C70_H$	DLC register 8	DLCR8	R/W	$XXXXXXXX_B$
$007C71_H$				
$007C72_H$	DLC register 9	DLCR9	R/W	$XXXXXXXX_B$
$007C73_H$				
$007C74_H$	DLC register 10	DLCR10	R/W	$XXXXXXXX_B$
$007C75_H$				
$007C76_H$	DLC register 11	DLCR11	R/W	$XXXXXXXX_B$
$007C77_H$				
$007C78_H$	DLC register 12	DLCR12	R/W	$XXXXXXXX_B$
$007C79_H$				
$007C7A_H$	DLC register 13	DLCR13	R/W	$XXXXXXXX_B$
$007C7B_H$				
$007C7C_H$	DLC register 14	DLCR14	R/W	$XXXXXXXX_B$
$007C7D_H$				
$007C7E_H$	DLC register 15	DLCR15	R/W	$XXXXXXXX_B$
$007C7F_H$				

(Continued)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C80_H$ to $007C87_H$	Data register 0 (8 bytes)	DTR0	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C88_H$ to $007C8F_H$	Data register 1 (8 bytes)	DTR1	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C90_H$ to $007C97_H$	Data register 2 (8 bytes)	DTR2	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C98_H$ to $007C9F_H$	Data register 3 (8 bytes)	DTR3	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CA0_H$ to $007CA7_H$	Data register 4 (8 bytes)	DTR4	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CA8_H$ to $007CAF_H$	Data register 5 (8 bytes)	DTR5	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CB0_H$ to $007CB7_H$	Data register 6 (8 bytes)	DTR6	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CB8_H$ to $007CBF_H$	Data register 7 (8 bytes)	DTR7	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CC0_H$ to $007CC7_H$	Data register 8 (8 bytes)	DTR8	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CC8_H$ to $007CCF_H$	Data register 9 (8 bytes)	DTR9	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CD0_H$ to $007CD7_H$	Data register 10 (8 bytes)	DTR10	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CD8_H$ to $007CDF_H$	Data register 11 (8 bytes)	DTR11	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CE0_H$ to $007CE7_H$	Data register 12 (8 bytes)	DTR12	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CE8_H$ to $007CEF_H$	Data register 13 (8 bytes)	DTR13	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

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Interrupt cause	EI^{2}OS corresponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX	Y2	14	#39	$FFFF60_H$	ICR14	$0000BE_H$
UART 2 TX	Y1	15	#40	$FFFF5C_H$		
Flash Memory	N	—	#41	$FFFF58_H$	ICR15	$0000BF_H$
Delayed Interrupt	N	—	#42	$FFFF54_H$		

Y1 : Usable

Y2 : Usable, with EI^{2}OS stop function

N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When the peripheral resources sharing the ICR register use extended intelligent I/O service, only one can use EI^{2}OS at a time.
- When either of the two peripheral resources sharing the ICR register specifies EI^{2}OS, the other one cannot use interrupts.

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVRH	V_{SS} − 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$*2
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6.0	V	*3
Maximum Clamp Current	I_{CLAMP}	−4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	—	40	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	50	mA	*4
“H” level maximum output current	I_{OH}	—	−15	mA	*4
“H” level average output current	I_{OHAV}	—	−4	mA	*4
“H” level maximum overall output current	ΣI_{OH}	—	−100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	−50	mA	*4
Power consumption	P_D	—	454	mW	
Operating temperature	T_A	−40	+105	°C	
		−40	+125	°C	*6
Storage temperature	T_{STG}	−55	+150	°C	

(Continued)

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCLS}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub sleep T_A = +25°C	—	20	50	µA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep T_A = +25°C	—	60	200	µA	MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	—	60	200	µA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, At sub sleep T_A = +25°C	—	70	150	µA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep T_A = +25°C	—	110	300	µA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	—	110	300	µA	MB90356TES MB90F356TES MB90357TES MB90F357TES

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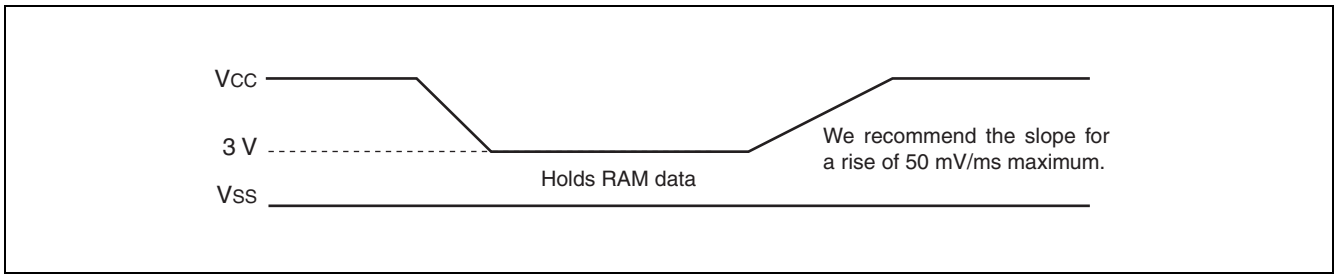
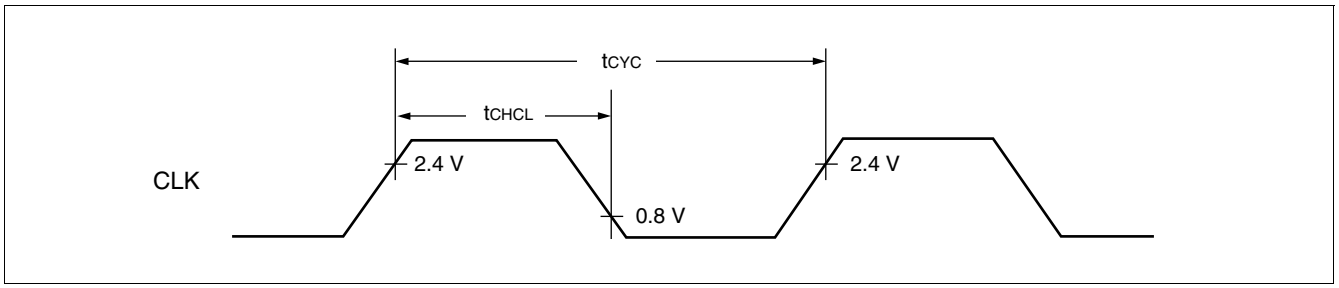
Note : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within
1 V/s, you can operate while using the PLL clock.



13.4.4 Clock Output Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

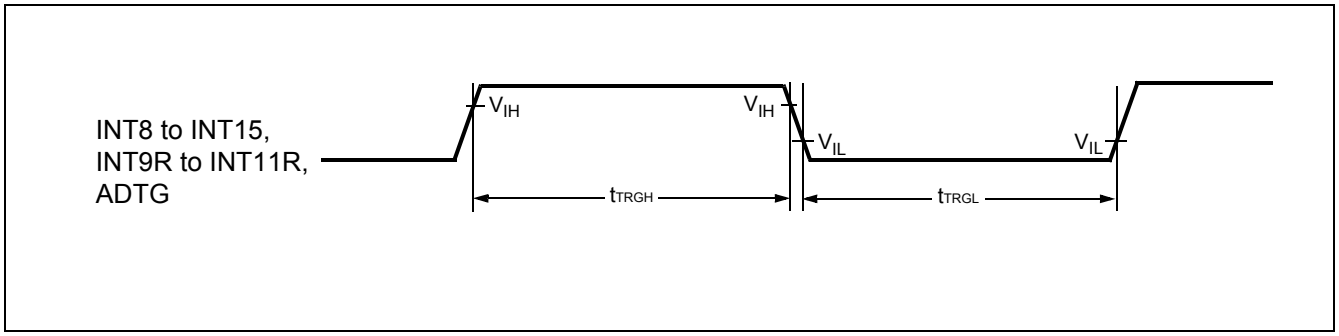
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	f_{CP} = 16 MHz
				41.67	—	ns	f_{CP} = 24 MHz
CLK↑ →CLK ↓	t_{CHCL}	CLK	—	20	—	ns	f_{CP} = 16 MHz
				13	—	ns	f_{CP} = 24 MHz



13.4.10 Trigger Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

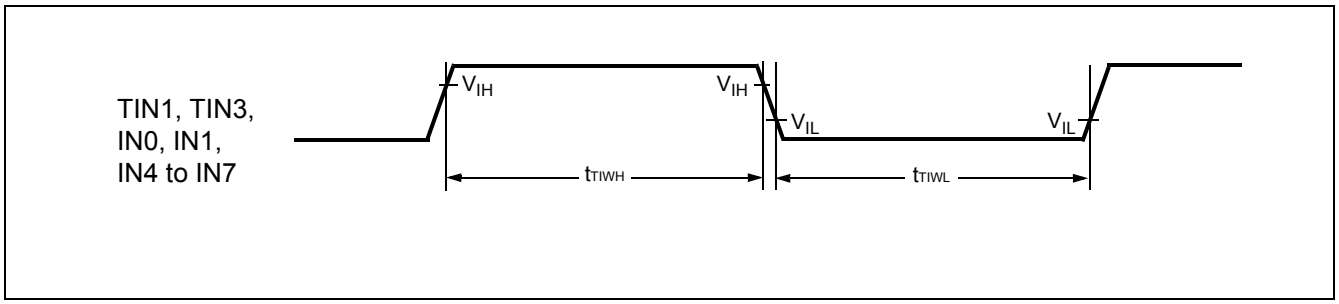
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	5 t_{CP}	—	ns



13.4.11 Timer Related Resource Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

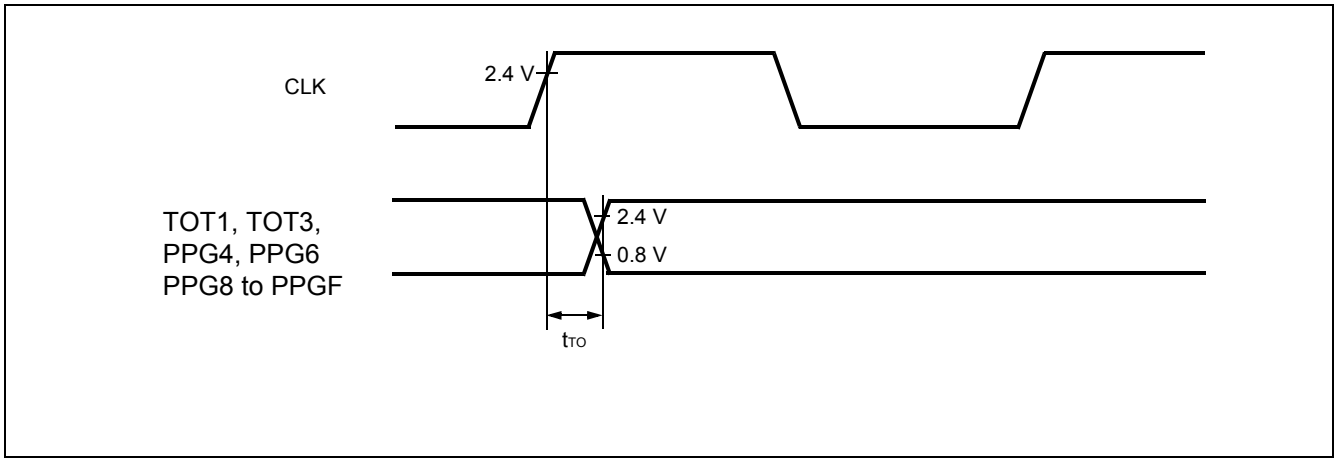
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN1, TIN3,IN0, IN1, IN4 to IN7	—	4 t_{CP}	—	ns



13.4.12 Timer Related Resource Output Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT1, TOT3, PPG4, PPG6, PPG8 to PPGF	—	30	—	ns



13.4.13 I^2C Timing

(T_A = −40°C to +125°C, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time for (repeated) START condition SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250*5	—	100*5	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

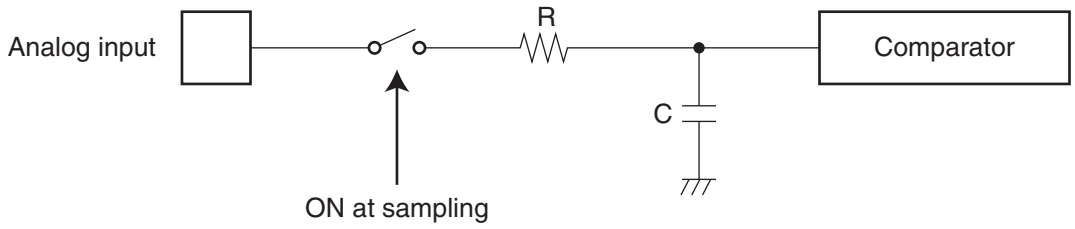
*2 : The maximum t_{HDDAT} has to meet at least that the device does not exceed the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I^2C -bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

*5 : Refer to "• Note of SDA, SCL set-up time".

· Analog input equivalence circuit



MB90F351E(S),MB90F351TE(S),MB90F352E(S),MB90F352TE(S),
MB90F356E(S),MB90F356TE(S),MB90F357E(S),MB90F357TE(S)

	R	C
4.5 V ≤ AV_{CC} ≤ 5.5 V	2.0 kΩ (Max)	16.0 pF (Max)
4.0 V ≤ AV_{CC} ≤ 4.5 V	8.2 kΩ (Max)	16.0 pF (Max)

MB90351E(S),MB90351TE(S),MB90352E(S),MB90352TE(S),
MB90356E(S),MB90356TE(S),MB90357E(S),MB90357TE(S),
MB90V340E-101/102/103/104

	R	C
4.5 V ≤ AV_{CC} ≤ 5.5 V	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AV_{CC} ≤ 4.5 V	8.2 kΩ (Max)	14.4 pF (Max)

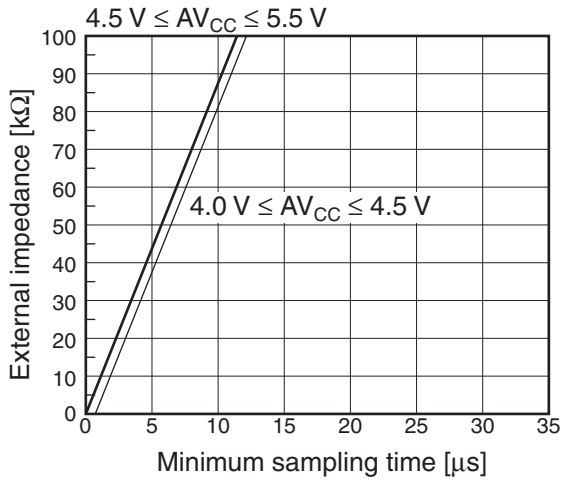
Note : The value is reference value.

■ Flash memory device

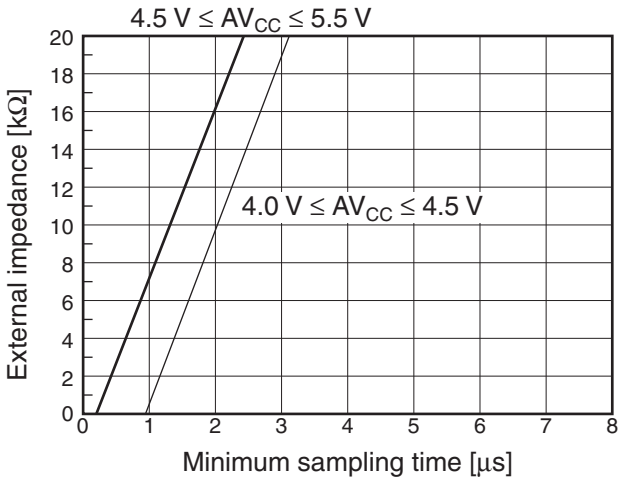
· Relation between External impedance and minimum sampling time

(MB90F351E(S),MB90F351TE(S),MB90F352E(S),MB90F352TE(S),
MB90F356E(S),MB90F356TE(S),MB90F357E(S),MB90F357TE(S))

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]



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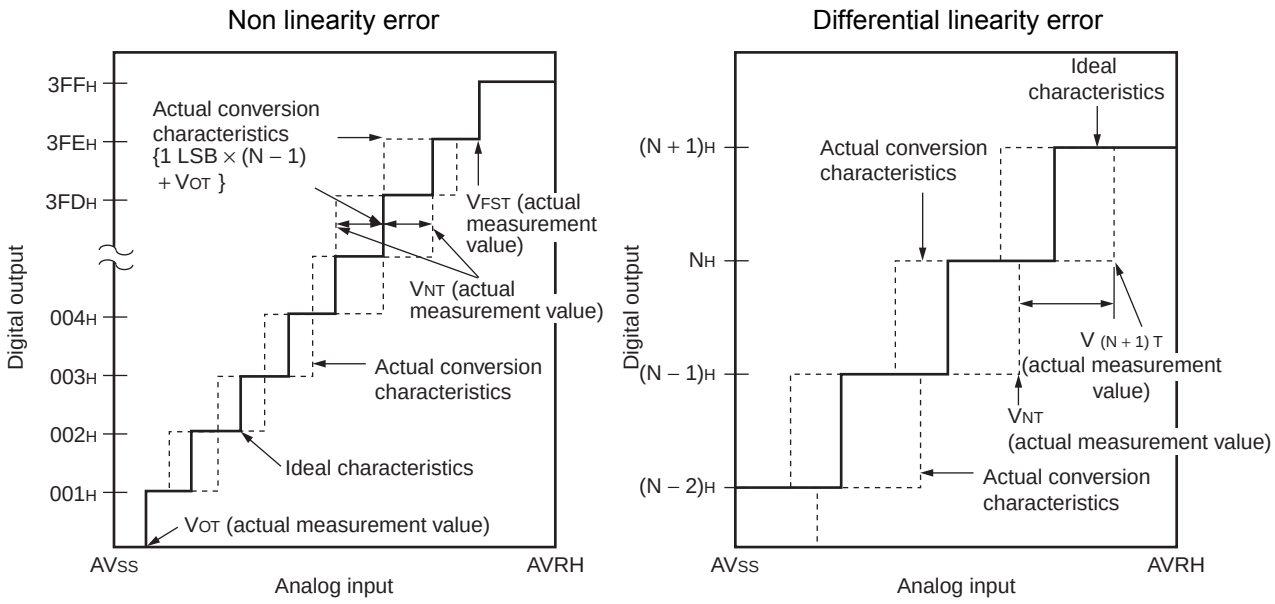

$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H".
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$".

13.7 Flash Memory Program/Erase Characteristics

■ Dual Operation Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T_A = +25°C V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10000	—	—	cycle	

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Flash memory Data Retention Time	Average T_A = +85°C	20	—	—	year	*

* : Corresponding value comes from the technology reliability evaluation result.
(Using Arrhenius equation to translate high temperature measurements test result into normalized value at +85°C)

14. Ordering Information

Part number	Package	Remarks
MB90F351EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	Flash memory products (64 Kbytes)
MB90F351ESPMC		
MB90F351TEPMC		
MB90F351TESPMC		
MB90F356EPMC		
MB90F356ESPMC		
MB90F356TEPMC		
MB90F356TESPMC		
MB90F352EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ESPMC		
MB90F352TEPMC		
MB90F352TESPMC		
MB90F357EPMC		
MB90F357ESPMC		
MB90F357TEPMC		
MB90F357TESPMC		
MB90351EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	MASK ROM products (64 Kbytes)
MB90351ESPMC		
MB90351TEPMC		
MB90351TESPMC		
MB90356EPMC		
MB90356ESPMC		
MB90356TEPMC		
MB90356TESPMC		
MB90352EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	MASK ROM products (128 Kbytes)
MB90352ESPMC		
MB90352TEPMC		
MB90352TESPMC		
MB90357EPMC		
MB90357ESPMC		
MB90357TEPMC		
MB90357TESPMC		

(Continued)

(Continued)

Part number	Package	Remarks
MB90F351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	Flash memory products (64 Kbytes)
MB90F351ESPMC1		
MB90F351TEPMC1		
MB90F351TESPMC1		
MB90F356EPMC1		
MB90F356ESPMC1		
MB90F356TEPMC1		
MB90F356TESPMC1		
MB90F352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ESPMC1		
MB90F352TEPMC1		
MB90F352TESPMC1		
MB90F357EPMC1		
MB90F357ESPMC1		
MB90F357TEPMC1		
MB90F357TESPMC1		
MB90351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	MASK ROM products (64 Kbytes)
MB90351ESPMC1		
MB90351TEPMC1		
MB90351TESPMC1		
MB90356EPMC1		
MB90356ESPMC1		
MB90356TEPMC1		
MB90356TESPMC1		
MB90352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	MASK ROM products (128 Kbytes)
MB90352ESPMC1		
MB90352TEPMC1		
MB90352TESPMC1		
MB90357EPMC1		
MB90357ESPMC1		
MB90357TEPMC1		
MB90357TESPMC1		
MB90V340E-101CR	299-pin ceramic PGA PGA-299C-A01	Device for evaluation
MB90V340E-102CR		
MB90V340E-103CR		
MB90V340E-104CR		

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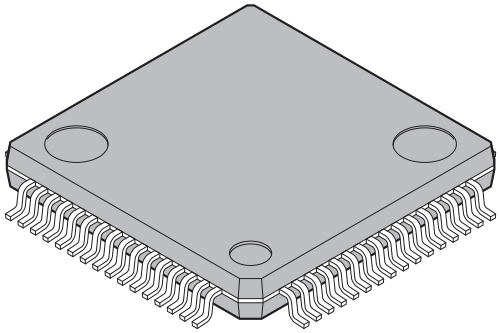
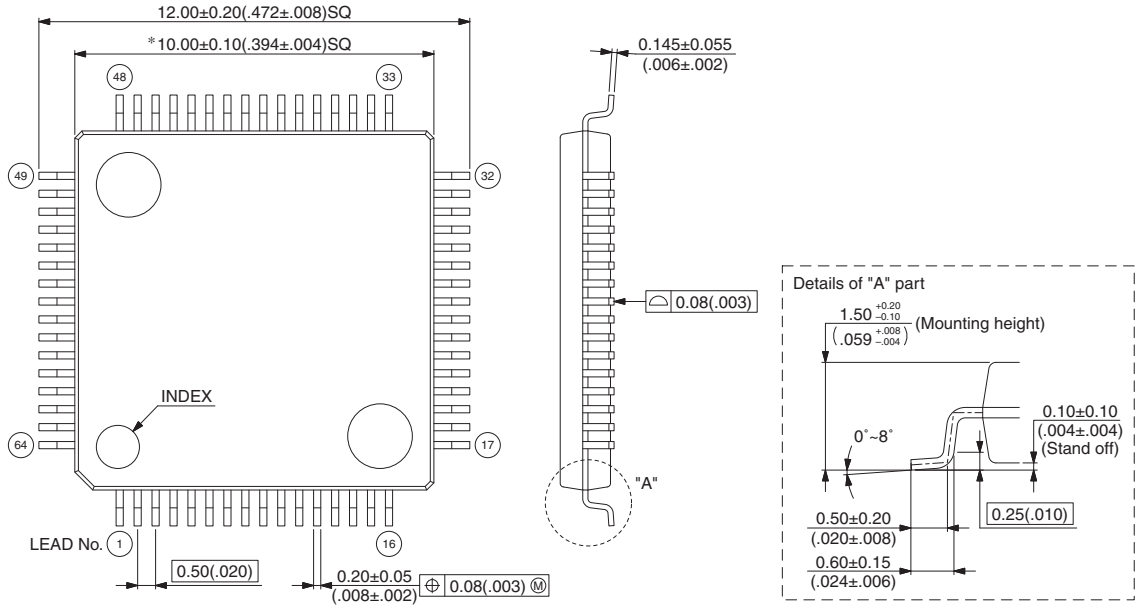
64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-64P-M24)	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

15. Major Changes

Page	Section	Change Results
—	—	The following names are changed. UART → LIN-UART 16-bit I/O timer → 16-bit free-run timer
26	Handling Devices	Added the section ”13. Serial Communication”.
51	Electrical Characteristics Absolute Maximum Ratings	Changed the maximum value of power consumption.
63	Electrical Characteristics AC Characteristics	Changed the "(4) Clock Output Timing". Changed the Minimum value of cycle time. (41.76 → 41.67)
69 to 73		Changed the notation of “(9) LIN-UART”.
78	A/D Converter	Changed the notation of “Zero reading voltage” and “full scale reading voltage”.
85	Ordering Information	Changed the part number; MB90V340E-101 → MB90V340E-101CR MB90V340E-102 → MB90V340E-102CR MB90V340E-103 → MB90V340E-103CR MB90V340E-104 → MB90V340E-104CR

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90350E Series F^{2}MC-16LX 16-bit Microcontrollers Document Number: 002-04493				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	10/12/2006	Migrated to Cypress and assigned document number 002-04993. No change to document contents or format.
*A	5193077	AKIH	04/07/2016	Updated to Cypress template