



Welcome to **E-XFL.COM**

What is "Embedded - Microcontrollers"?

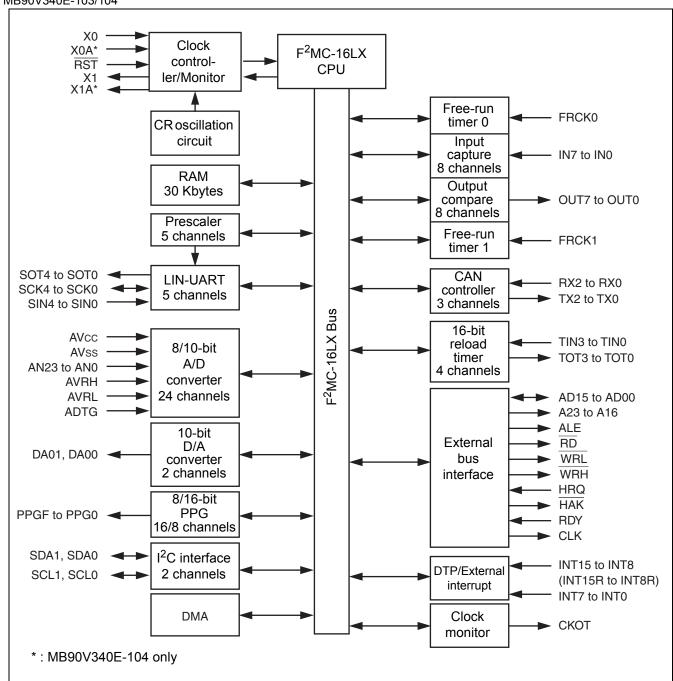
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f357tespmc1-gse1

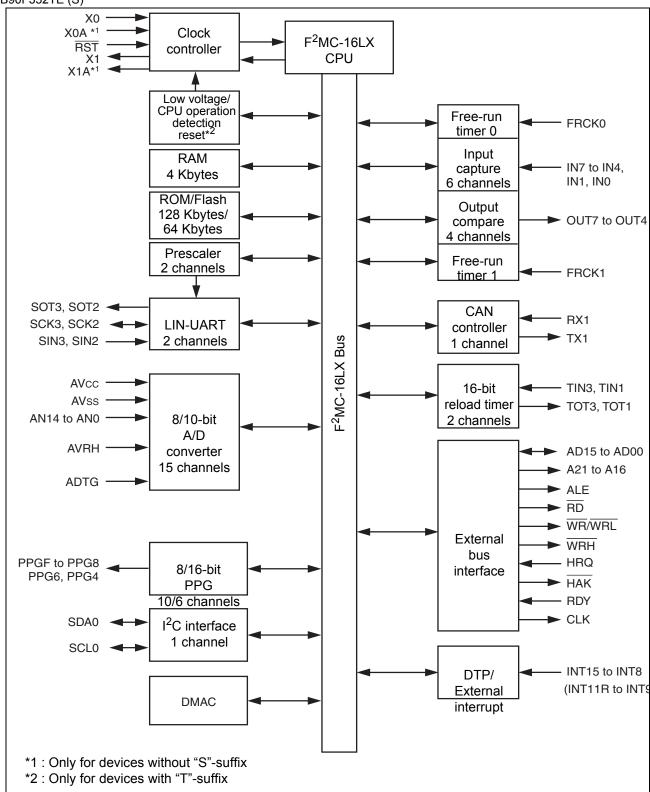


■ MB90V340E-103/104





■ MB90351E (S), MB90351TE (S), MB90F351E (S), MB90F351TE (S), MB90352E (S), MB90352TE (S), MB90F352E (S)





Address	Register	Abbreviation	Access	Resource name	Initial value
000058 _H		1			
to 00005B _H		Reserved			
00005C _H	Output Compare Control Status Register 4	OCS4	R/W		0000XX00 _B
00005D _H	Output Compare Control Status Register 5	OCS5	R/W	Output Compare 4/5	0XX00000 _B
00005E _H	Output Compare Control Status Register 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B
00005F _H	Output Compare Control Status Register 7	OCS7	R/W	Output Compare 6/7	0XX00000 _B
000060 _H	Timer Control Status Register 0	TMCSR0	R/W	40 hit Daland Times 0	00000000 _B
000061 _H	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	XXXX0000 _B
000062 _H	Timer Control Status Register 1	TMCSR1	R/W	4C hit Daland Times 4	00000000 _B
000063 _H	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	XXXX0000 _B
000064 _H	Timer Control Status Register 2	TMCSR2	R/W	40 hit Daland Times 0	00000000 _B
000065 _H	Timer Control Status Register 2	TMCSR2	R/W	16-bit Reload Timer 2	XXXX0000 _B
000066 _H	Timer Control Status Register 3	TMCSR3	R/W	40.1 " D 1 1 1 1 1 2	00000000 _B
000067 _H	Timer Control Status Register 3	TMCSR3	R/W	16-bit Reload Timer 3	XXXX0000 _B
000068 _H	A/D Control Status Register 0	ADCS0	R/W		000XXXX0 _B
000069 _H	A/D Control Status Register 1	ADCS1	R/W		0000000X _B
00006A _H	A/D Data Register 0	ADCR0	R	A /D O	00000000 _B
00006B _H	A/D Data Register 1	ADCR1	R	A/D Converter	XXXXXX00 _B
00006C _H	ADC Setting Register 0	ADSR0	R/W		00000000 _B
00006D _H	ADC Setting Register 1	ADSR1	R/W		00000000 _B
00006E _H	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low Voltage/CPU Operation Detection Reset	00111000 _B
00006F _H	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	XXXXXXX1 _B
000070 _H to 00007F _H		Reserved			
000080 _H to 00008F _H	Reserved for CAN controller 1. Refer to "CAN C	ontrollers"			
000090 _H to 00009A _H		Reserved			



Address	Register	Abbreviation	Access	Resource name	Initial value
00009B _H	DMA Descriptor Channel Specification Register	DCSR	R/W		00000000 _B
00009C _H	DMA Status Register L Register	DSRL	R/W	DMA	00000000 _B
00009D _H	DMA Status Register H Register	DSRH	R/W		00000000 _B
00009E _H	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000 _B
00009F _H	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	XXXXXXX0 _B
0000A0 _H	Low-power Consumption Mode Control Register	LPMCR	W,R/W	Low Power Consumption Control Circuit	00011000 _B
0000A1 _H	Clock Selection Register	CKSCR	R,R/W	Low Power Consumption Control Circuit	11111100 _B
0000A2 _H , 0000A3 _H		Reserved			
0000A4 _H	DMA Stop Status Register	DSSR	R/W	DMA	00000000 _B
0000A5 _H	Automatic Ready Function Selection Register	ARSR	W	External Memory	0011XX00 _B
0000A6 _H	External Address Output Control Register	HACR	W	Access	00000000 _B
0000A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B
0000A8 _H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXX111 _B
0000A9 _H	Timebase Timer Control Register	ТВТС	W,R/W	Timebase timer	1XX00100 _B
0000AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
0000AB _H		Reserved			
0000AC _H	DMA Enable Register L Register	DERL	R/W	DMA	00000000 _B
0000AD _H	DMA Enable Register H Register	DERH	R/W	DIVIA	00000000 _B
0000AE _H	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash memory	000X0000 _B
0000AF _H		Reserved	•		
0000B0 _H	Interrupt Control Register 00	ICR00	W,R/W		00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W,R/W	Interrupt Control	00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B



Address	Register	Abbreviation	Access	Resource name	Initial value
0000B9 _H	Interrupt Control Register 09	ICR09	W,R/W		00000111 _B
0000BA _H	Interrupt Control Register 10	ICR10	W,R/W		00000111 _B
0000BB _H	Interrupt Control Register 11	ICR11	W,R/W		00000111 _B
0000BC _H	Interrupt Control Register 12	ICR12	W,R/W	Interrupt Control	00000111 _B
0000BD _H	Interrupt Control Register 13	ICR13	W,R/W		00000111 _B
0000BE _H	Interrupt Control Register 14	ICR14	W,R/W		00000111 _B
0000BF _H	Interrupt Control Register 15	ICR15	W,R/W		00000111 _B
0000C0 _H to 0000C9 _H		Reserved			
0000CA _H	External Interrupt Enable Register 1	ENIR1	R/W		00000000 _B
0000CB _H	External Interrupt Source Register 1	EIRR1	R/W		XXXXXXXX
0000CC _H	External Interrupt Level Register 1	ELVR1	R/W	External Interrupt 1	00000000 _B
0000CD _H	External Interrupt Level Register 1	ELVR1	R/W	External interrupt 1	00000000 _B
0000CE _H	External Interrupt Source Select Register	EISSR	R/W		00000000 _B
0000CF _H	PLL/Sub clock Control register	PSCCR	W	PLL	XXXX0000 _B
0000D0 _H	DMA Buffer Address Pointer L Register	BAPL	R/W		XXXXXXXX _B
0000D1 _H	DMA Buffer Address Pointer M Register	ВАРМ	R/W		XXXXXXXX _B
0000D2 _H	DMA Buffer Address Pointer H Register	ВАРН	R/W		XXXXXXXX _B
0000D3 _H	DMA Control Register	DMACS	R/W	DMA	XXXXXXXX _B
0000D4 _H	I/O Register Address Pointer L Register	IOAL	R/W		XXXXXXXX _B
0000D5 _H	I/O Register Address Pointer H Register	IOAH	R/W		XXXXXXXX _B
0000D6 _H	Data Counter L Register	DCTL	R/W		XXXXXXXX
0000D7 _H	Data Counter H Register	DCTH	R/W		XXXXXXXX
0000D8 _H	Serial Mode Register 2	SMR2	W,R/W		00000000 _B
0000D9 _H	Serial Control Register 2	SCR2	W,R/W		00000000 _B
0000DA _H	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000 _B
0000DB _H	Serial Status Register 2	SSR2	R,R/W	UART2	00001000 _B
0000DC _H	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX _B
0000DD _H	Extended Status/Control Register 2	ESCR2	R/W		00000100 _B
0000DE _H	Baud Rate Generator Register 20	BGR20	R/W		00000000 _B



Address	Register	Abbreviation	Access	Initial Value
CAN1	Negistei	Abbieviation	Access	illitiai value
007C40 _H				XXXXXXXX _B
007C41 _H	ID register 8	IDR8	R/W	XXXXXXXX _B
007C42 _H	ib register o	IDRO	INVV	XXXXXXXX _B
007C43 _H				XXXXXXXX _B
007C44 _H				XXXXXXXX _B
007C45 _H	ID register 9	IDR9	R/W	XXXXXXXX _B
007C46 _H	ib register 9	IDIX9	1000	XXXXXXXX _B
007C47 _H				XXXXXXXX _B
007C48 _H				XXXXXXXX _B
007C49 _H	ID register 10	IDR10	R/W	XXXXXXXX _B
007C4A _H	ID register to	ואטו	R/W	XXXXXXXX _B
007C4B _H				XXXXXXXXB
007C4C _H				XXXXXXXX _B
007C4D _H	ID register 11	IDR11	R/W	$XXXXXXXX_B$
007C4E _H		IDKTI		XXXXXXXX _B
007C4F _H				$XXXXXXXX_B$
007C50 _H			R/W	XXXXXXXX _B
007C51 _H	ID register 12	IDR12		$XXXXXXXX_B$
007C52 _H	ID register 12	IDR12		XXXXXXXX _B
007C53 _H				$XXXXXXXX_B$
007C54 _H				XXXXXXXX _B
007C55 _H	ID register 13	IDR13	R/W	$XXXXXXXX_B$
007C56 _H	ib register 13	IDK13	F/VV	XXXXXXXX _B
007C57 _H				XXXXXXXXB
007C58 _H				XXXXXXXX _B
007C59 _H	ID register 14	IDR14	R/W	XXXXXXXX _B
007C5A _H	ID register 14	IDK 14	17/1/	XXXXXXXX _B
007C5B _H				XXXXXXXXB
007C5C _H				XXXXXXXX _B
007C5D _H	ID register 15	IDR15	R/W	XXXXXXXXB
007C5E _H	ID register 15	פואטו	TV VV	XXXXXXXX _B
007C5F _H				XXXXXXXXB

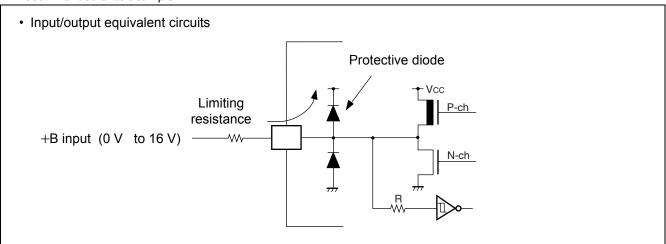


List of Message Buffers (DLC Registers and Data Registers)

Address	Docietes	Abbrevietien	A 0.000	Initial Value	
CAN1	Register	Abbreviation	Access	Initial Value	
007C60 _H	DLC register 0	DLCR0	R/W	VVVVVVV	
007C61 _H	DLC register 0	DLCRU	R/VV	XXXXXXXX _B	
007C62 _H	DLC register 1	DLCR1	R/W	VVVVVVV	
007C63 _H	DLC register 1	DLCKT	F/VV	XXXXXXXX _B	
007C64 _H	DLC register 2	DLCR2	R/W	XXXXXXXX _B	
007C65 _H	DLC register 2	DLCKZ	IN/VV	~~~~~~B	
007C66 _H	DLC register 3	DLCR3	R/W	XXXXXXXX _B	
007C67 _H	DLC register 3	DLCKS	IN/VV	~~~~~~B	
007C68 _H	DLC register 4	DLCR4	R/W	XXXXXXXX _B	
007C69 _H	DLC register 4	DLCK4	IN/VV	~~~~~~B	
007C6A _H	DLC register 5	DLCR5	R/W	VVVVVVV	
007C6B _H	DLC register 5	DLCRS	F/VV	XXXXXXXX _B	
007C6C _H	DLC register 6	DLCR6	R/W	VVVVVVV	
007C6D _H	DLC register 6	DLCRO	F/VV	XXXXXXXX _B	
007C6E _H	DLC register 7	DLCR7	R/W	XXXXXXXX _B	
007C6F _H	DLC register 7	DLCR/	R/VV	NAVANA B	
007C70 _H	DI C register 9	DLCR8	R/W	VVVVVVV	
007C71 _H	DLC register 8	DLCRo	F/VV	XXXXXXXX _B	
007C72 _H	DLC register 0	DLCR9	DAM	VVVVVVV	
007C73 _H	DLC register 9	DLCR9	R/W	XXXXXXXX _B	
007C74 _H	DLC register 10	DLCR10	R/W	VVVVVVV	
007C75 _H	DLC register 10	DLCKIU	F/VV	XXXXXXXX _B	
007C76 _H	DLC register 11	DLCR11	R/W	XXXXXXXX _B	
007C77 _H	DLC register 11	DLORTI	F/VV	^^^^^A	
007C78 _H	DLC register 12	DI CB12	R/W	VVVVVV-	
007C79 _H	DLC register 12	DLCR12	FV/ VV	XXXXXXX _B	
007C7A _H	DI C register 13	DLCR13	R/W	YYYY VVV-	
007C7B _H	DLC register 13	DLONIS	FV/ VV	XXXXXXXX _B	
007C7C _H	DLC register 14	DLCR14	R/W	YYYYYY	
007C7D _H	DLC register 14	DLCK14	FX/VV	XXXXXXXX _B	
007C7E _H	DI C register 15	DI CP15	D/M/	YYYYYY	
007C7F _H	DLC register 15	DLCR15	R/W	XXXXXXXX _B	



- *1: This parameter is based on $V_{SS} = AV_{SS} = 0 \text{ V}$
- *2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.
- *3: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.
- *4: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56, P60 to P67
- *5: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56 (for evaluation device : P50 to P55), P60 to P67
 - " Use within recommended operating conditions.
 - " Use at DC voltage (current)
 - " The +B signal should always be applied a connecting limit resistance between the +B signal and the microcontroller.
 - " The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - " Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - " Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
 - " Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
 - " Care must be taken not to leave the +B input pin open.
 - " Recommended circuit sample:



*6 : If used exceeding $T_A = +105$ °C, be sure to contact Cypress for reliability limitations.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

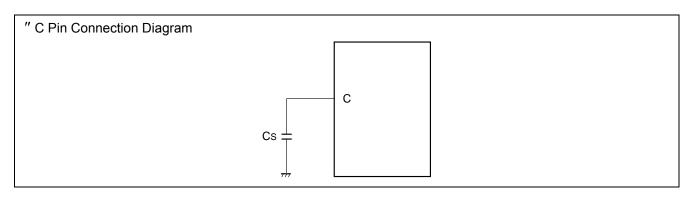


13.2 Recommended Operating Conditions

 $(V_{SS} = AV_{SS} = 0 V)$

Parameter	Symbol		Value		Unit	Remarks
raiailletei	Syllibol	Min	Тур	Max	Oilit	Remarks
		4.0	5.0	5.5	V	Under normal operation
Power supply voltage	V _{CC} , AV _{CC}	3.5	5.0	5.5	٧	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	_	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C _S	0.1	_	1.0	μF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V _{CC} pin should be greater than this capacitor.
Operating temperature	T _A	-40	_	+125	°C	*

 $^{^*}$: If used exceeding $T_A = +105^{\circ}C$, be sure to contact Cypress for reliability limitations.



WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



13.3 DC Characteristics

(T_A = -40 °C to +125 °C, V_{CC} = 5.0 V \pm 10%, $f_{CP} \leq$ 24 MHz, $V_{SS} = AV_{SS} = 0$ V)

D	0	mbol Bin Condition			Value		1114	Barranta	
Parameter	Symbol	Pin	Condition	Min	Тур	Max	Unit	Remarks	
	V _{IHS}	_	_	0.8 V _{CC}	_	V _{CC} + 0.3	V	Pin inputs if CMOS hysteresis input levels are se- lected (except P12, P15, P44, P45, P50)	
"H" level	V _{IHA}	_	_	0.8 V _{CC}	_	V _{CC} + 0.3	V	Pin inputs if Automotive input levels are selected	
input voltage	V _{IHT}	_	_	2.0	_	V _{CC} + 0.3	V	Pin inputs if TTL input levels are selected	
(At V _{CC} = 5 V ± 10%)	V _{IHS}	_	_	0.7 V _{CC}	_	V _{CC} + 0.3	٧	P12, P15, P50 inputs if CMOS input levels are selected	
	V _{IHI}	_	_	0.7 V _{CC}	_	V _{CC} + 0.3	٧	P44, P45 inputs if CMOS hysteresis input levels are selected	
	V _{IHR}	_	_	0.8 V _{CC}	1	V _{CC} + 0.3	>	RST input pin (CMOS hysteresis)	
	V_{IHM}	_	_	V _{CC} - 0.3	_	V _{CC} + 0.3	V	MD input pin	
	V _{ILS}	_	_	V _{SS} – 0.3	_	0.2 V _{CC}	٧	Pin inputs if CMOS hysteresis input levels are se- lected (except P12, P15, P44, P45, P50)	
"L" level	V _{ILA}	_	_	V _{SS} – 0.3	_	0.5 V _{CC}	٧	Pin inputs if Automotive input levels are selected	
input voltage	V _{ILT}	_	_	V _{SS} - 0.3	_	0.8	V	Pin inputs if TTL input levels are selected	
(At V _{CC} = 5 V ± 10%)	V _{ILS}	_	_	V _{SS} - 0.3	_	0.3 V _{CC}	٧	P12, P15, P50 inputs if CMOS input levels are selected	
	V _{ILI}	_	_	V _{SS} – 0.3	_	0.3 V _{CC}	٧	P44, P45 inputs if CMOS hysteresis input levels are selected	
	V _{ILR}		_	V _{SS} - 0.3	_	0.2 V _{CC}	V	RST input pin (CMOS hysteresis)	
	V _{ILM}	_	_	V _{SS} - 0.3	_	V _{SS} + 0.3	V	MD input pin	
Output "H" voltage	V _{OH}	Normal out- puts	$V_{CC} = 4.5 \text{ V},$ $I_{OH} = -4.0 \text{ mA}$	V _{CC} - 0.5	ı	_	٧		
Output "H" voltage	V _{OHI}	I ² C current outputs	$V_{CC} = 4.5 \text{ V},$ $I_{OH} = -3.0 \text{ mA}$	V _{CC} - 0.5			V		



(T_A = -40°C to +125°C, V_{CC} = 5.0 V \pm 10%, $f_{CP} \leq$ 24 MHz, $V_{SS} = AV_{SS} = 0$ V)

	Sym-		(7 _A 10 0 to 1120 to		Value			
Parameter	bol	Pin	Condition		Тур	Max	Unit	Remarks
			V _{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub sleep T _A = +25°C	_	20	50	μА	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90F357E
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep T_A = +25°C	_	60	200	μА	MB90356E MB90F356E MB90357E MB90F357E
Power supply	Power supply current I _{CCLS}	V _{CC}	V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	_	60	200	μА	MB90356ES MB90F356ES MB90357ES MB90F357ES
current		vcc	V _{CC} = 5.0 V, Internal frequency: 8 kHz, At sub sleep T _A = +25°C	_	70	150	μА	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90F356TE MB90F356TE MB90F357TE MB90F357TE
	V _{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep T _A = +25°C	_	110	300	μА	MB90356TE MB90F356TE MB90357TE MB90F357TE		
		V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	_	110	300	μА	MB90356TES MB90F356TES MB90357TES MB90F357TES	



13.4.5 Bus Timing (Read)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V \pm 10 %, V_{SS} = 0.0 V, f_{CP} \leq 24 MHz)

Parameter	Sym-	Pin	Condition	Va	lue	Unit
Faranteter	bol	FIII	Condition	Min	Max	ns
ALE pulse width	t _{LHLL}	ALE		t _{CP} /2 - 10	_	ns
Valid address $ ightarrow$ ALE \downarrow time	t _{AVLL}	ALE, A21 to A16, AD15 to AD00		t _{CP} /2 – 20	_	ns
ALE $\downarrow \rightarrow$ Address valid time	t _{LLAX}	ALE, AD15 to AD00		t _{CP} /2 - 15	_	ns
$Valid\;address\to\overline{RD}\;\downarrow\;time$	t _{AVRL}	A21 to A16, AD15 to AD00, RD		t _{CP} – 15	_	ns
Valid address → Valid data input	t _{AVDV}	A21 to A16, AD15 to AD00		_	5 t _{CP} /2 – 60	ns
RD pulse width	t _{RLRH}	RD		(n*+3/2) t _{CP} - 20	_	ns
$\overline{RD} \downarrow \to Valid$ data input	t _{RLDV}	RD, AD15 to AD00	_	_	(n*+3/2) t _{CP} - 50	ns
$\overline{RD} \uparrow \to Data \; hold \; time$	t _{RHDX}	RD, AD15 to AD00		0	_	ns
$\overline{RD} \uparrow \to ALE \uparrow time$	t _{RHLH}	RD, ALE		t _{CP} /2 - 15	_	ns
$\overline{RD} \uparrow \to Address$ valid time	t _{RHAX}	RD, A21 to A16		t _{CP} /2 - 10	_	ns
Valid address → CLK ↑ time	t _{AVCH}	A21 to A16, AD15 to AD00, CLK		t _{CP} /2 – 16	_	ns
$\overline{RD} \downarrow \to CLK \uparrow time$	t _{RLCH}	RD, CLK		t _{CP} /2 – 15	_	ns
$ALE \downarrow \to \overline{RD} \downarrow time$	t _{LLRL}	ALE, RD		t _{CP} /2 – 15	_	ns

^{*:} Number of ready cycles



13.4.9 LIN-UART2/3

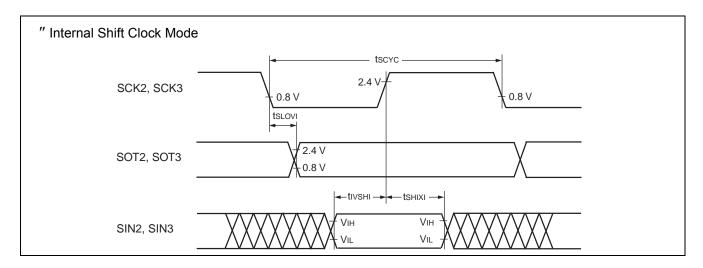
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

 $(T_A = -40^{\circ}C$ to +125°C, $V_{CC} = 5.0~V \pm 10\%, f_{CP} \leq 24~MHz, \, V_{SS} = 0~V)$

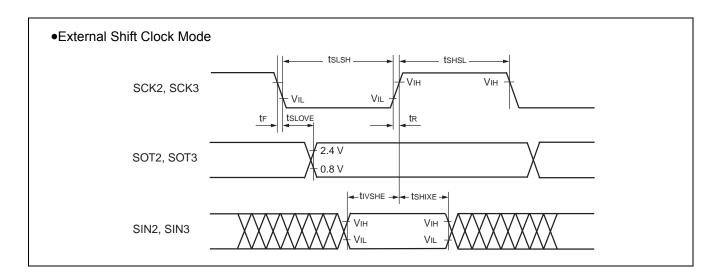
Parameter	Symbol	Pin	Condition	Value		Unit	
Parameter	Symbol	PIII	Condition	Min	Max	O.iii	
Serial clock cycle time	t _{SCYC}	SCK2, SCK3		5 t _{CP}	_	ns	
$SCK \downarrow \to SOT$ delay time	t _{SLOVI}	SCK2, SCK3 SOT2, SOT3	Internal shift clock	-50	+50	ns	
Valid SIN → SCK ↑	t _{IVSHI}	SCK2, SCK3 SIN2, SIN3	mode output pins are CL = 80 pF + 1 TTL.	t _{CP} + 80	_	ns	
SCK ↑ → Valid SIN hold time	t _{SHIXI}	SCK2, SCK3 SIN2, SIN3		0	_	ns	
Serial clock "L" pulse width	t _{SHSL}	SCK2, SCK3		3 t _{CP} - t _R	_	ns	
Serial clock "H" pulse width	t _{SLSH}	SCK2, SCK3		t _{CP} + 10	_	ns	
$SCK \downarrow \to SOT$ delay time	t _{SLOVE}	SCK2, SCK3 SOT2, SOT3		_	2 t _{CP} + 60	ns	
Valid SIN → SCK ↑	t _{IVSHE}	SCK2, SCK3 SIN2, SIN3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	30	_	ns	
SCK ↑ → Valid SIN hold time	t _{SHIXE}	SCK2, SCK3 SIN2, SIN3		t _{CP} + 30	_	ns	
SCK fall time	t _F	SCK2, SCK3		_	10	ns	
SCK rise time	t _R	SCK2, SCK3		_	10	ns	

Notes: • AC characteristic in CLK synchronized mode.

- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".







■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0

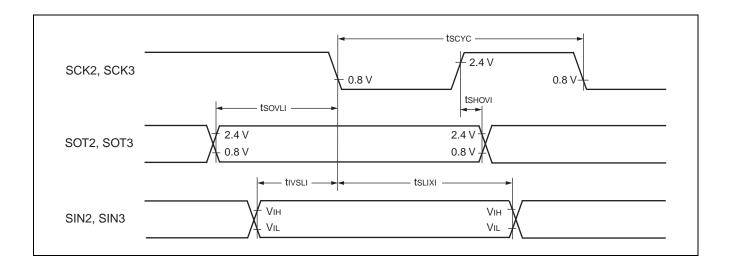
 $(T_A = -40^{\circ}C~to~+125^{\circ}C,~V_{CC} = 5.0~V \pm 10\%,~f_{CP} \leq 24~MHz,~V_{SS} = 0~V)$

Dorometer	Cumbal	Pin	Condition		alue	
Parameter	Symbol	PIII	Condition	Min	Max	Unit
Serial clock cycle time	t _{SCYC}	SCK2, SCK3		5 t _{CP}	=	ns
$SCK \uparrow \rightarrow SOT$ delay time	t _{shovi}	SCK2, SCK3 SOT2, SOT3	Internal shift clock	-50	+50	ns
Valid SIN → SCK \downarrow	t _{IVSLI}	SCK2, SCK3 SIN2, SIN3	mode output pins are CL = 80 pF + 1 TTL.	t _{CP} + 80	=	ns
$SCK \downarrow \to Valid \; SIN \; hold \; time$	t _{SLIXI}	SCK2, SCK3 SIN2, SIN3		0	=	ns
Serial clock "H" pulse width	t _{SHSL}	SCK2, SCK3		3 t _{CP} - t _R	-	ns
Serial clock "L" pulse width	t _{SLSH}	SCK2, SCK3		t _{CP} + 10	-	ns
$SCK \uparrow \rightarrow SOT$ delay time	t _{SHOVE}	SCK2, SCK3 SOT2, SOT3		_	2 t _{CP} + 60	ns
Valid SIN → SCK \downarrow	t _{IVSLE}	SCK2, SCK3 SIN2, SIN3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	30	_	ns
$SCK \downarrow \to Valid \; SIN \; hold \; time$	t _{SLIXE}	SCK2, SCK3 SIN2, SIN3		t _{CP} + 30	_	ns
SCK fall time	t _F	SCK2, SCK3		=	10	ns
SCK rise time	t _R	SCK2, SCK3			10	ns

Notes : $\, \bullet \, C_L$ is load capacity value of pins when testing.

• t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".





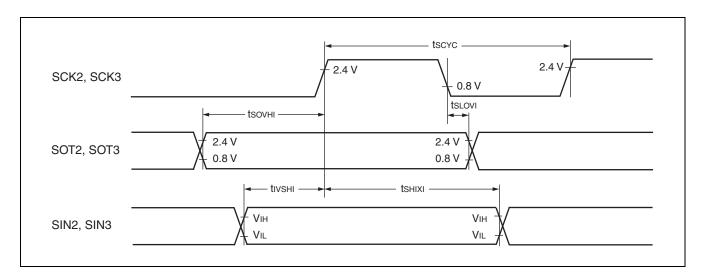
■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1

$$(T_A = -40^{\circ}C \text{ to } +125^{\circ}C,\, V_{CC} = 5.0 \text{ V} \pm 10\%,\, f_{CP} \leq 24 \text{ MHz},\, V_{SS} = 0 \text{ V})$$

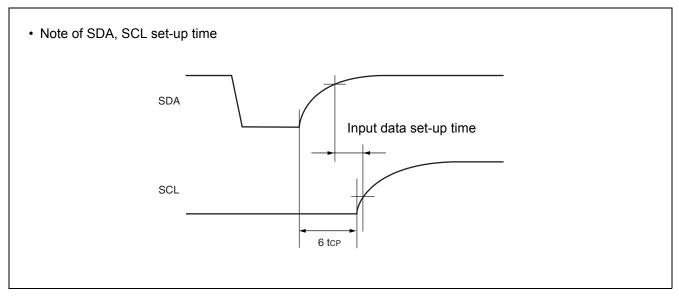
Parameter	Symbol	Pin	Condition	Value		Unit
Farameter	Symbol	FIII	Condition	Min	Max	Oilit
Serial clock cycle time	t _{SCYC}	SCK2, SCK3		5 t _{CP}	ı	ns
$SCK \downarrow \rightarrow SOT$ delay time	t _{SLOVI}	SCK2, SCK3 SOT2, SOT3	Internal clock operation output pins are	-50	+50	ns
Valid SIN → SCK ↑	t _{IVSHI}	SCK2, SCK3 SIN2, SIN3		t _{CP} + 80	_	ns
SCK ↑ → Valid SIN hold time	t _{SHIXI}	SCK2, SCK3 SIN2, SIN3	CL = 80 pF + 1 TTL.	0	_	ns
$SOT \rightarrow SCK \uparrow delay time$	t _{SOVHI}	SCK2, SCK3 SOT2, SOT3		3 t _{CP} – 70	_	ns

Notes: \bullet C_L is load capacity value of pins when testing.

[•]t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".

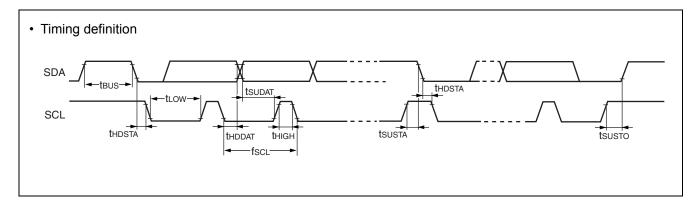




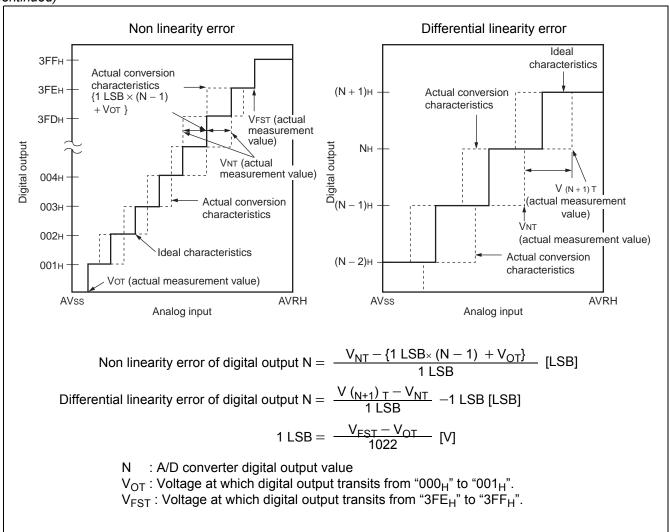


Note: The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.

Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.







13.7 Flash Memory Program/Erase Characteristics

■ Dual Operation Flash Memory

Parameter	Conditions	Value			Unit	Remarks
	Conditions	Min	Тур	Max	Oilit	Remarks
Sector erase time (4 Kbytes sector)		_	0.2	0.5	S	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)	T _A = +25°C	_	0.5	7.5	S	Excludes programming prior to erasure
Chip erase time	$T_A = +25^{\circ}C$ $V_{CC} = 5.0 \text{ V}$	_	4.6	_	s	Excludes programming prior to erasure
Word (16-bit width) programming time		_	64	3600	μS	Except for the overhead time of the system level
Program/Erase cycle	_	10000	_	_	cycle	



Part number	Package	Remarks		
MB90F351EPMC1				
MB90F351ESPMC1				
MB90F351TEPMC1				
MB90F351TESPMC1	64-pin plastic LQFP	Flash memory products (64 Kbytes)		
MB90F356EPMC1	FPT-64P-M24 10.0 mm , 0.50 mm pitch			
MB90F356ESPMC1	7			
MB90F356TEPMC1				
MB90F356TESPMC1				
MB90F352EPMC1				
MB90F352ESPMC1				
MB90F352TEPMC1				
MB90F352TESPMC1	64-pin plastic LQFP FPT-64P-M24	Dual operation		
MB90F357EPMC1	10.0 mm , 0.50 mm pitch	Flash memory products (128 Kbytes)		
MB90F357ESPMC1				
MB90F357TEPMC1				
MB90F357TESPMC1				
MB90351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm			
MB90351ESPMC1				
MB90351TEPMC1		MASK ROM products (64 Kbytes)		
MB90351TESPMC1				
MB90356EPMC1				
MB90356ESPMC1				
MB90356TEPMC1				
MB90356TESPMC1				
MB90352EPMC1				
MB90352ESPMC1				
MB90352TEPMC1				
MB90352TESPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm	MASK ROM products (128 Kbytes)		
MB90357EPMC1				
MB90357ESPMC1				
MB90357TEPMC1				
MB90357TESPMC1				
MB90V340E-101CR				
MB90V340E-102CR	299-pin ceramic PGA	Device for evaluation		
MB90V340E-103CR	PGA-299C-A01			
MB90V340E-104CR				



15. Major Changes

Page	Section	Change Results
_	_	The following names are changed. UART → LIN-UART 16-bit I/O timer → 16-bit free-run timer
26	Handling Devices	Added the section "13. Serial Communication".
51	Electrical Characteristics Absolute Maximum Ratings	Changed the maximum value of power consumption.
63	Electrical Characteristics AC Characteristics	Changed the "(4) Clock Output Timing". Changed the Minimum value of cycle time. (41.76 → 41.67)
69 to 73		Changed the notation of "(9) LIN-UART".
78	A/D Converter	Changed the notation of "Zero reading voltage" and "full scale reading voltage".
85	Ordering Information	Changed the part number; MB90V340E-101 → MB90V340E-101CR MB90V340E-102 → MB90V340E-102CR MB90V340E-103 → MB90V340E-103CR MB90V340E-104 → MB90V340E-104CR

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB90350E Series F ² MC-16LX 16-bit Microcontrollers Document Number: 002-04493					
Revision	ECN	Orig. of Change	Submission Date	Description of Change	
**	_	AKIH		Migrated to Cypress and assigned document number 002-04993. No change to document contents or format.	
*A	5193077	AKIH	04/07/2016	Updated to Cypress template	



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers

Automotive

Clocks & Buffers

Interface

Lighting & Power Control

Memory

PSoC

cypress.com/automotive

cypress.com/clocks

cypress.com/interface

cypress.com/powerpsoc

cypress.com/pesoc

cypress.com/psoc

Touch Sensing cypress.com/touch
USB Controllers cypress.com/usb
Wireless/RF cypress.com/wireless

PSoC® Solutions

cypress.com/psoc PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2006-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.