Infineon Technologies - MB90F357TESPMC1-GSE1 Datasheet

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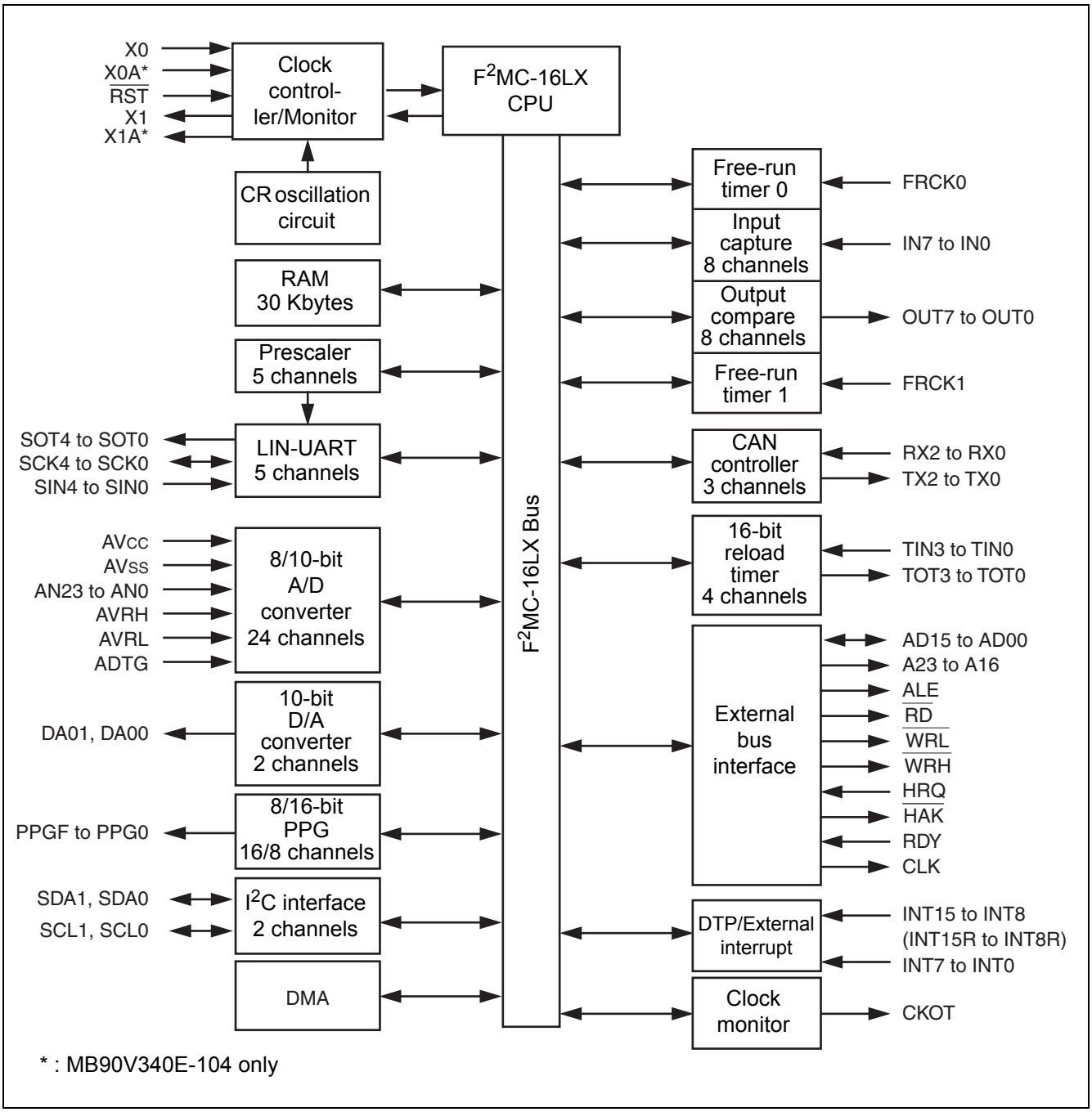
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

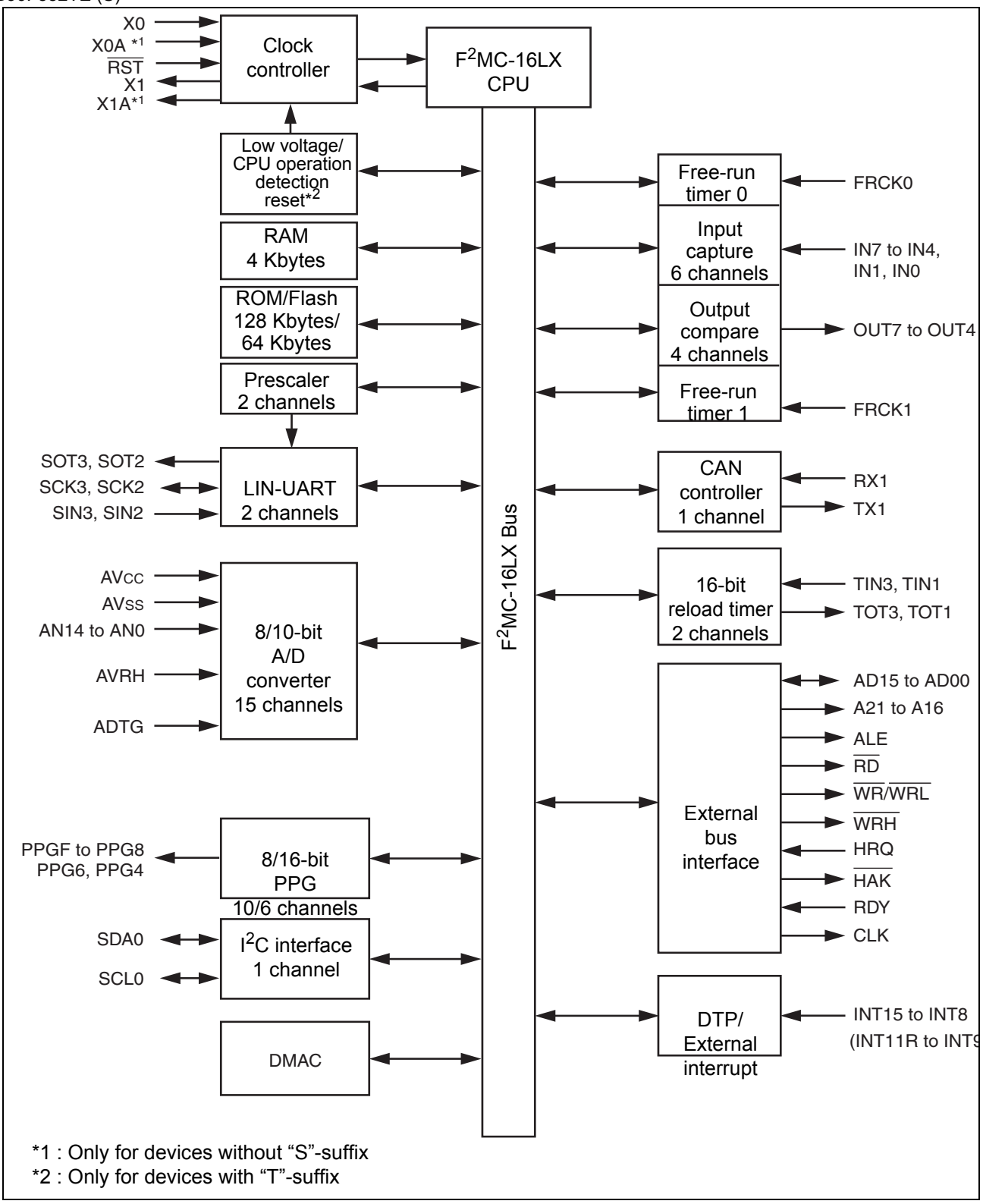
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f357tespmc1-gse1

■ MB90V340E-103/104



■ MB90351E (S) , MB90351TE (S) , MB90F351E (S) , MB90F351TE (S) , MB90352E (S) , MB90352TE (S) , MB90F352E (S) MB90F352TE (S)



Address	Register	Abbreviation	Access	Resource name	Initial value
000058_H to $00005B_H$	Reserved				
$00005C_H$	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	$0000XX00_B$
$00005D_H$	Output Compare Control Status Register 5	OCS5	R/W		$0XX00000_B$
$00005E_H$	Output Compare Control Status Register 6	OCS6	R/W	Output Compare 6/7	$0000XX00_B$
$00005F_H$	Output Compare Control Status Register 7	OCS7	R/W		$0XX00000_B$
000060_H	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000_B
000061_H	Timer Control Status Register 0	TMCSR0	R/W		$XXXX0000_B$
000062_H	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000_B
000063_H	Timer Control Status Register 1	TMCSR1	R/W		$XXXX0000_B$
000064_H	Timer Control Status Register 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000_B
000065_H	Timer Control Status Register 2	TMCSR2	R/W		$XXXX0000_B$
000066_H	Timer Control Status Register 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000_B
000067_H	Timer Control Status Register 3	TMCSR3	R/W		$XXXX0000_B$
000068_H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	$000XXXX0_B$
000069_H	A/D Control Status Register 1	ADCS1	R/W		$0000000X_B$
$00006A_H$	A/D Data Register 0	ADCR0	R		00000000_B
$00006B_H$	A/D Data Register 1	ADCR1	R		$XXXXXX00_B$
$00006C_H$	ADC Setting Register 0	ADSR0	R/W		00000000_B
$00006D_H$	ADC Setting Register 1	ADSR1	R/W		00000000_B
$00006E_H$	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low Voltage/CPU Operation Detection Reset	00111000_B
$00006F_H$	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	$XXXXXXX1_B$
000070_H to $00007F_H$	Reserved				
000080_H to $00008F_H$	Reserved for CAN controller 1. Refer to “CAN Controllers”				
000090_H to $00009A_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$00009B_H$	DMA Descriptor Channel Specification Register	DCSR	R/W	DMA	00000000_B
$00009C_H$	DMA Status Register L Register	DSRL	R/W		00000000_B
$00009D_H$	DMA Status Register H Register	DSRH	R/W		00000000_B
$00009E_H$	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000_B
$00009F_H$	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	$XXXXXXX0_B$
$0000A0_H$	Low-power Consumption Mode Control Register	LPMCR	W,R/W	Low Power Consumption Control Circuit	00011000_B
$0000A1_H$	Clock Selection Register	CKSCR	R,R/W	Low Power Consumption Control Circuit	11111100_B
$0000A2_H$, $0000A3_H$	Reserved				
$0000A4_H$	DMA Stop Status Register	DSSR	R/W	DMA	00000000_B
$0000A5_H$	Automatic Ready Function Selection Register	ARSR	W	External Memory Access	$0011XX00_B$
$0000A6_H$	External Address Output Control Register	HACR	W		00000000_B
$0000A7_H$	Bus Control Signal Selection Register	ECSR	W		$0000000X_B$
$0000A8_H$	Watchdog Control Register	WDTC	R,W	Watchdog Timer	$XXXXX111_B$
$0000A9_H$	Timebase Timer Control Register	TBTC	W,R/W	Timebase timer	$1XX00100_B$
$0000AA_H$	Watch Timer Control Register	WTC	R,R/W	Watch Timer	$1X001000_B$
$0000AB_H$	Reserved				
$0000AC_H$	DMA Enable Register L Register	DERL	R/W	DMA	00000000_B
$0000AD_H$	DMA Enable Register H Register	DERH	R/W		00000000_B
$0000AE_H$	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash memory	$000X0000_B$
$0000AF_H$	Reserved				
$0000B0_H$	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111_B
$0000B1_H$	Interrupt Control Register 01	ICR01	W,R/W		00000111_B
$0000B2_H$	Interrupt Control Register 02	ICR02	W,R/W		00000111_B
$0000B3_H$	Interrupt Control Register 03	ICR03	W,R/W		00000111_B
$0000B4_H$	Interrupt Control Register 04	ICR04	W,R/W		00000111_B
$0000B5_H$	Interrupt Control Register 05	ICR05	W,R/W		00000111_B
$0000B6_H$	Interrupt Control Register 06	ICR06	W,R/W		00000111_B
$0000B7_H$	Interrupt Control Register 07	ICR07	W,R/W		00000111_B
$0000B8_H$	Interrupt Control Register 08	ICR08	W,R/W		00000111_B

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Address	Register	Abbreviation	Access	Resource name	Initial value
$0000B9_H$	Interrupt Control Register 09	ICR09	W,R/W	Interrupt Control	00000111_B
$0000BA_H$	Interrupt Control Register 10	ICR10	W,R/W		00000111_B
$0000BB_H$	Interrupt Control Register 11	ICR11	W,R/W		00000111_B
$0000BC_H$	Interrupt Control Register 12	ICR12	W,R/W		00000111_B
$0000BD_H$	Interrupt Control Register 13	ICR13	W,R/W		00000111_B
$0000BE_H$	Interrupt Control Register 14	ICR14	W,R/W		00000111_B
$0000BF_H$	Interrupt Control Register 15	ICR15	W,R/W		00000111_B
$0000C0_H$ to $0000C9_H$	Reserved				
$0000CA_H$	External Interrupt Enable Register 1	ENIR1	R/W	External Interrupt 1	00000000_B
$0000CB_H$	External Interrupt Source Register 1	EIRR1	R/W		$XXXXXXXX_B$
$0000CC_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000_B
$0000CD_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000_B
$0000CE_H$	External Interrupt Source Select Register	EISSR	R/W		00000000_B
$0000CF_H$	PLL/Sub clock Control register	PSCCR	W	PLL	$XXXX0000_B$
$0000D0_H$	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	$XXXXXXXX_B$
$0000D1_H$	DMA Buffer Address Pointer M Register	BAPM	R/W		$XXXXXXXX_B$
$0000D2_H$	DMA Buffer Address Pointer H Register	BAPH	R/W		$XXXXXXXX_B$
$0000D3_H$	DMA Control Register	DMACS	R/W		$XXXXXXXX_B$
$0000D4_H$	I/O Register Address Pointer L Register	IOAL	R/W		$XXXXXXXX_B$
$0000D5_H$	I/O Register Address Pointer H Register	IOAH	R/W		$XXXXXXXX_B$
$0000D6_H$	Data Counter L Register	DCTL	R/W		$XXXXXXXX_B$
$0000D7_H$	Data Counter H Register	DCTH	R/W		$XXXXXXXX_B$
$0000D8_H$	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000_B
$0000D9_H$	Serial Control Register 2	SCR2	W,R/W		00000000_B
$0000DA_H$	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000_B
$0000DB_H$	Serial Status Register 2	SSR2	R,R/W		00001000_B
$0000DC_H$	Extended Communication Control Register 2	ECCR2	R,W, R/W		$000000XX_B$
$0000DD_H$	Extended Status/Control Register 2	ESCR2	R/W		00000100_B
$0000DE_H$	Baud Rate Generator Register 20	BGR20	R/W		00000000_B

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Address CAN1	Register	Abbreviation	Access	Initial Value
$007C40_H$	ID register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C41_H$				
$007C42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C43_H$				
$007C44_H$	ID register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C45_H$				
$007C46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C47_H$				
$007C48_H$	ID register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C49_H$				
$007C4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C4B_H$				
$007C4C_H$	ID register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C4D_H$				
$007C4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C4F_H$				
$007C50_H$	ID register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C51_H$				
$007C52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C53_H$				
$007C54_H$	ID register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C55_H$				
$007C56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C57_H$				
$007C58_H$	ID register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C59_H$				
$007C5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C5B_H$				
$007C5C_H$	ID register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007C5D_H$				
$007C5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007C5F_H$				

List of Message Buffers (DLC Registers and Data Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C60_H$	DLC register 0	DLCR0	R/W	$XXXXXXXX_B$
$007C61_H$				
$007C62_H$	DLC register 1	DLCR1	R/W	$XXXXXXXX_B$
$007C63_H$				
$007C64_H$	DLC register 2	DLCR2	R/W	$XXXXXXXX_B$
$007C65_H$				
$007C66_H$	DLC register 3	DLCR3	R/W	$XXXXXXXX_B$
$007C67_H$				
$007C68_H$	DLC register 4	DLCR4	R/W	$XXXXXXXX_B$
$007C69_H$				
$007C6A_H$	DLC register 5	DLCR5	R/W	$XXXXXXXX_B$
$007C6B_H$				
$007C6C_H$	DLC register 6	DLCR6	R/W	$XXXXXXXX_B$
$007C6D_H$				
$007C6E_H$	DLC register 7	DLCR7	R/W	$XXXXXXXX_B$
$007C6F_H$				
$007C70_H$	DLC register 8	DLCR8	R/W	$XXXXXXXX_B$
$007C71_H$				
$007C72_H$	DLC register 9	DLCR9	R/W	$XXXXXXXX_B$
$007C73_H$				
$007C74_H$	DLC register 10	DLCR10	R/W	$XXXXXXXX_B$
$007C75_H$				
$007C76_H$	DLC register 11	DLCR11	R/W	$XXXXXXXX_B$
$007C77_H$				
$007C78_H$	DLC register 12	DLCR12	R/W	$XXXXXXXX_B$
$007C79_H$				
$007C7A_H$	DLC register 13	DLCR13	R/W	$XXXXXXXX_B$
$007C7B_H$				
$007C7C_H$	DLC register 14	DLCR14	R/W	$XXXXXXXX_B$
$007C7D_H$				
$007C7E_H$	DLC register 15	DLCR15	R/W	$XXXXXXXX_B$
$007C7F_H$				

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*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

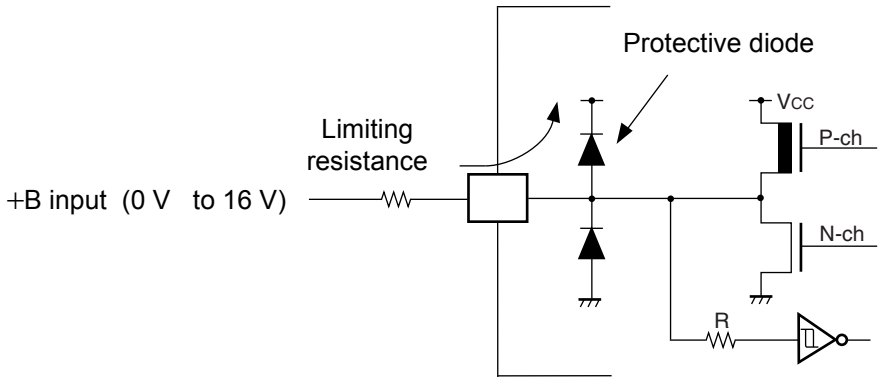
*3: V_I and V_O should not exceed $V_{CC} + 0.3$ V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56, P60 to P67

*5: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56 (for evaluation device : P50 to P55) , P60 to P67

- ″ Use within recommended operating conditions.
- ″ Use at DC voltage (current)
- ″ The +B signal should always be applied a connecting limit resistance between the +B signal and the microcontroller.
- ″ The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- ″ Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- ″ Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- ″ Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- ″ Care must be taken not to leave the +B input pin open.
- ″ Recommended circuit sample:

• Input/output equivalent circuits



*6 : If used exceeding $T_A = +105°C$, be sure to contact Cypress for reliability limitations.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

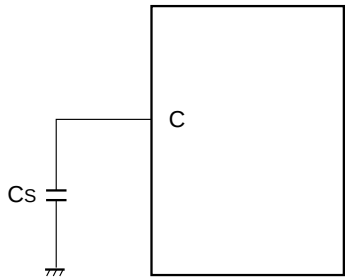
13.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	−40	—	+125	°C	*

* : If used exceeding T_A = +105°C, be sure to contact Cypress for reliability limitations.

″ C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

13.3 DC Characteristics

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Pin inputs if TTL input levels are selected
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{IHI}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} − 0.3	—	V_{CC} + 0.3	V	MD input pin
"L" level input voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{ILA}	—	—	V_{SS} − 0.3	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected
	V_{ILT}	—	—	V_{SS} − 0.3	—	0.8	V	Pin inputs if TTL input levels are selected
	V_{ILS}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{ILI}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} − 0.3	—	V_{SS} + 0.3	V	MD input pin
Output "H" voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	V_{CC} − 0.5	—	—	V	
Output "H" voltage	V_{OHI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OH} = −3.0 mA	V_{CC} − 0.5	—	—	V	

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(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCLS}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub sleep T_A = +25°C	—	20	50	µA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep T_A = +25°C	—	60	200	µA	MB90356E MB90F356E MB90357E MB90F357E
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	—	60	200	µA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, At sub sleep T_A = +25°C	—	70	150	µA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep T_A = +25°C	—	110	300	µA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	—	110	300	µA	MB90356TES MB90F356TES MB90357TES MB90F357TES

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13.4.5 Bus Timing (Read)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, $f_{CP} \leq$ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE	–	$t_{CP}/2 - 10$	–	ns
Valid address → ALE ↓ time	t_{AVLL}	ALE, A21 to A16, AD15 to AD00		$t_{CP}/2 - 20$	–	ns
ALE ↓ → Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	–	ns
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	A21 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	–	ns
Valid address → Valid data input	t_{AVDV}	A21 to A16, AD15 to AD00		–	$5\ t_{CP}/2 - 60$	ns
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$(n^*+3/2)\ t_{CP} - 20$	–	ns
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		–	$(n^*+3/2)\ t_{CP} - 50$	ns
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	–	ns
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	–	ns
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A21 to A16		$t_{CP}/2 - 10$	–	ns
Valid address → CLK ↑ time	t_{AVCH}	A21 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	–	ns
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	–	ns
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	–	ns

* : Number of ready cycles

13.4.9 LIN-UART2/3

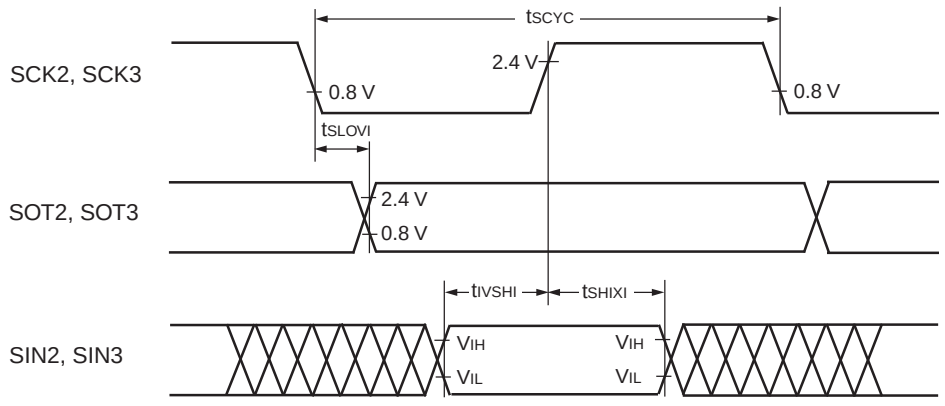
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

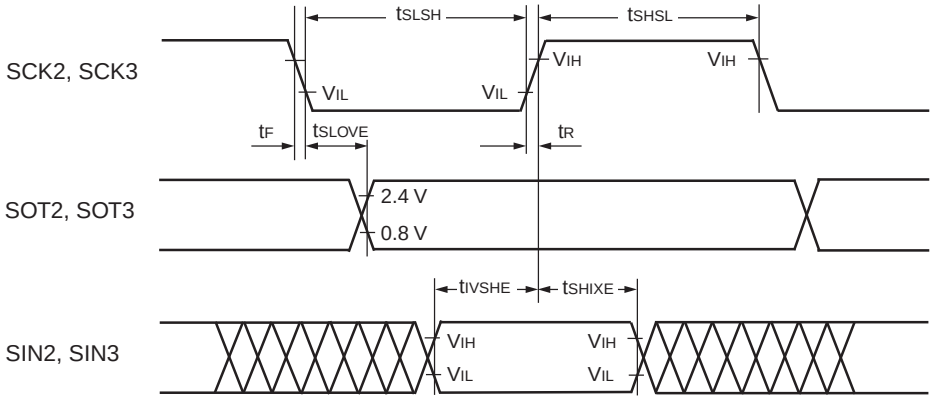
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal shift clock mode output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2, SCK3 SOT2, SOT3		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK2, SCK3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK2, SCK3		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK2, SCK3 SOT2, SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK2, SCK3 SIN2, SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK2, SCK3		—	10	ns
SCK rise time	t_R	SCK2, SCK3		—	10	ns

Notes :
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

″ Internal Shift Clock Mode



●External Shift Clock Mode

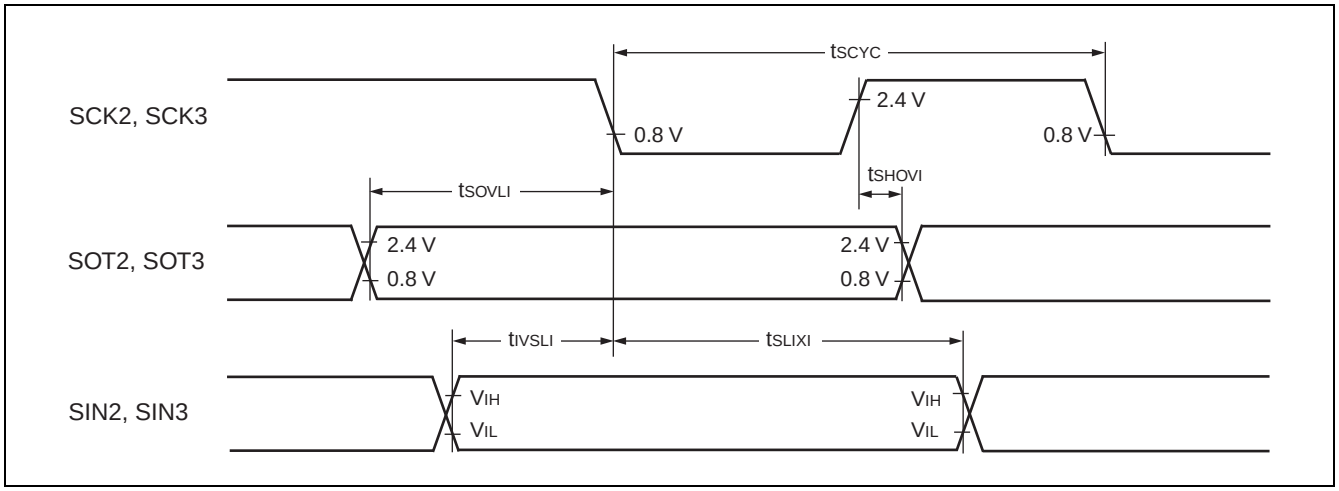


■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal shift clock mode output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	–	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2, SCK3 SOT2, SOT3		−50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK2, SCK3 SIN2, SIN3		0	–	ns
Serial clock “H” pulse width	t_{SHSL}	SCK2, SCK3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	3 t_{CP} - t_R	–	ns
Serial clock “L” pulse width	t_{SLSH}	SCK2, SCK3		t_{CP} + 10	–	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK2, SCK3 SOT2, SOT3		–	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK2, SCK3 SIN2, SIN3		30	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 30	–	ns
SCK fall time	t_F	SCK2, SCK3		–	10	ns
SCK rise time	t_R	SCK2, SCK3		–	10	ns

Notes :
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.



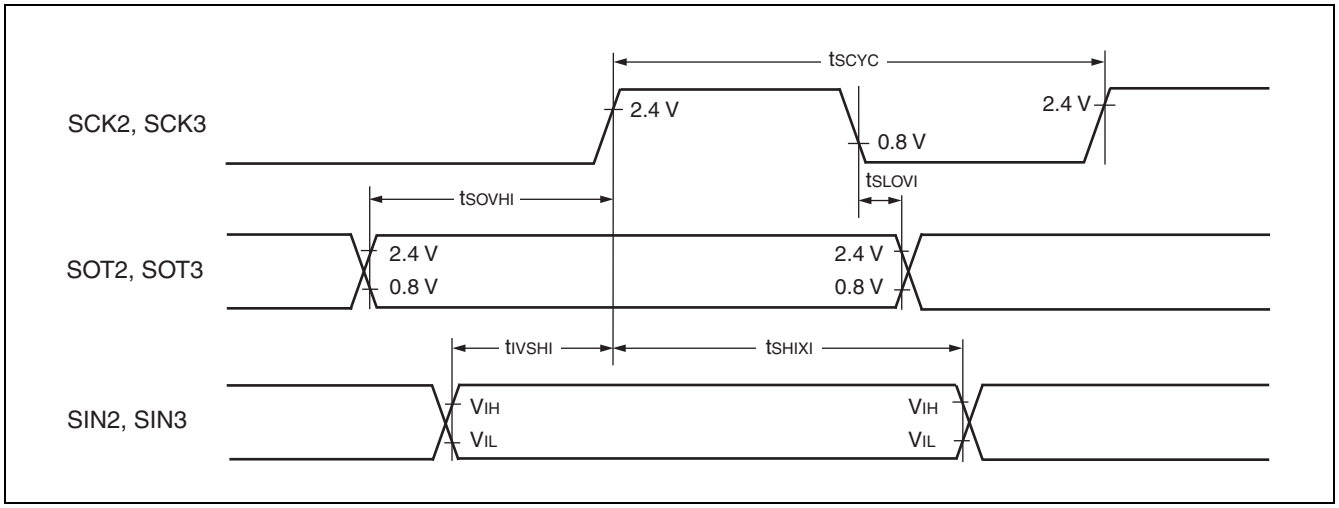
■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

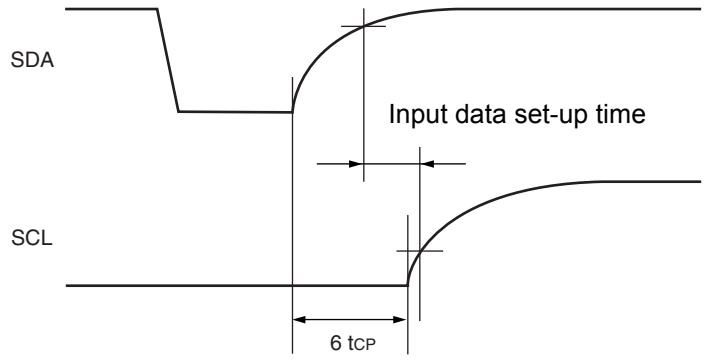
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal clock operation output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2, SCK3 SOT2, SOT3		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK2, SCK3 SOT2, SOT3		3 t_{CP} – 70	—	ns

Notes : • C_L is load capacity value of pins when testing.

•t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

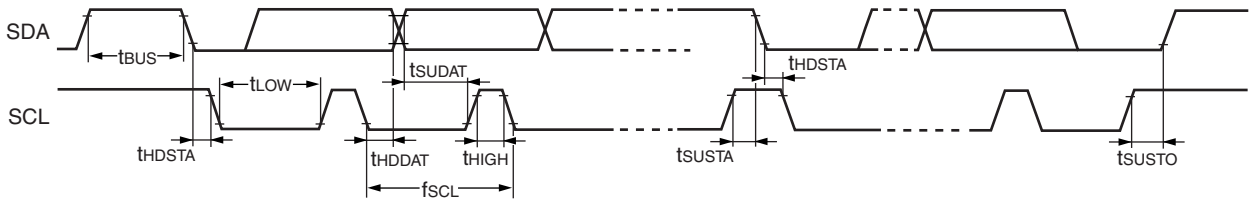


• Note of SDA, SCL set-up time

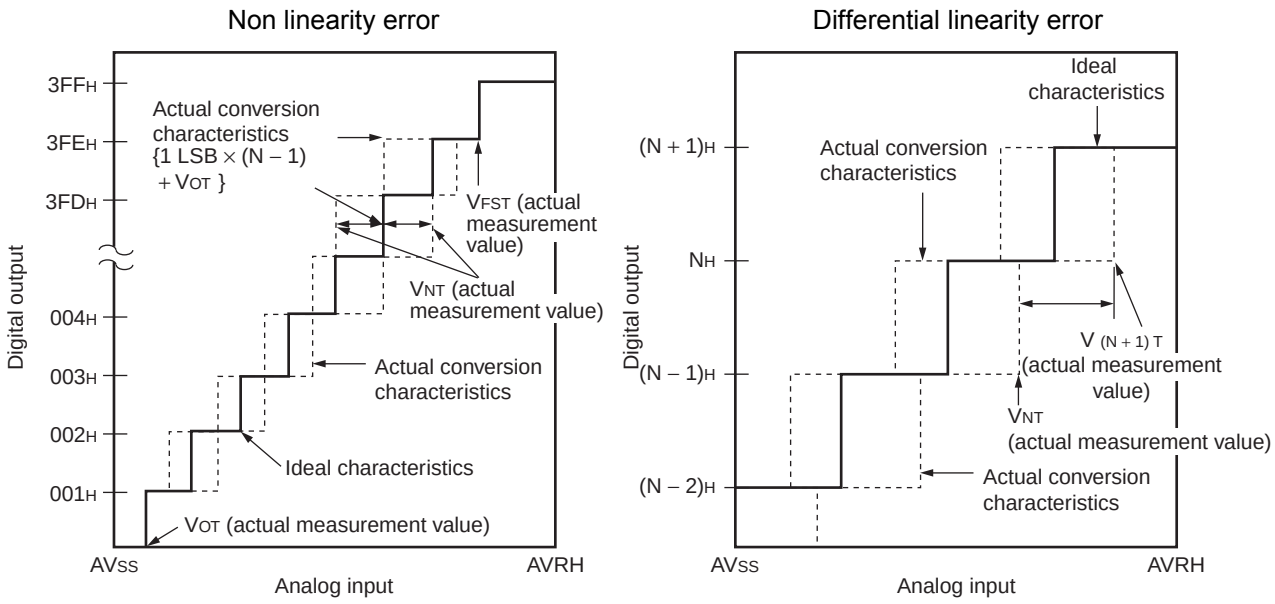


Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition



(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H".
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$".

13.7 Flash Memory Program/Erase Characteristics

■ Dual Operation Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T_A = +25°C V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10000	—	—	cycle	

(Continued)

Part number	Package	Remarks
MB90F351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	Flash memory products (64 Kbytes)
MB90F351ESPMC1		
MB90F351TEPMC1		
MB90F351TESPMC1		
MB90F356EPMC1		
MB90F356ESPMC1		
MB90F356TEPMC1		
MB90F356TESPMC1		
MB90F352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ESPMC1		
MB90F352TEPMC1		
MB90F352TESPMC1		
MB90F357EPMC1		
MB90F357ESPMC1		
MB90F357TEPMC1		
MB90F357TESPMC1		
MB90351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	MASK ROM products (64 Kbytes)
MB90351ESPMC1		
MB90351TEPMC1		
MB90351TESPMC1		
MB90356EPMC1		
MB90356ESPMC1		
MB90356TEPMC1		
MB90356TESPMC1		
MB90352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □, 0.50 mm pitch	MASK ROM products (128 Kbytes)
MB90352ESPMC1		
MB90352TEPMC1		
MB90352TESPMC1		
MB90357EPMC1		
MB90357ESPMC1		
MB90357TEPMC1		
MB90357TESPMC1		
MB90V340E-101CR	299-pin ceramic PGA PGA-299C-A01	Device for evaluation
MB90V340E-102CR		
MB90V340E-103CR		
MB90V340E-104CR		

15. Major Changes

Page	Section	Change Results
—	—	The following names are changed. UART → LIN-UART 16-bit I/O timer → 16-bit free-run timer
26	Handling Devices	Added the section ”13. Serial Communication”.
51	Electrical Characteristics Absolute Maximum Ratings	Changed the maximum value of power consumption.
63	Electrical Characteristics AC Characteristics	Changed the "(4) Clock Output Timing". Changed the Minimum value of cycle time. (41.76 → 41.67)
69 to 73		Changed the notation of “(9) LIN-UART”.
78	A/D Converter	Changed the notation of “Zero reading voltage” and “full scale reading voltage”.
85	Ordering Information	Changed the part number; MB90V340E-101 → MB90V340E-101CR MB90V340E-102 → MB90V340E-102CR MB90V340E-103 → MB90V340E-103CR MB90V340E-104 → MB90V340E-104CR

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90350E Series F^{2}MC-16LX 16-bit Microcontrollers Document Number: 002-04493				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	10/12/2006	Migrated to Cypress and assigned document number 002-04993. No change to document contents or format.
*A	5193077	AKIH	04/07/2016	Updated to Cypress template

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