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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x16b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51mm128cmb

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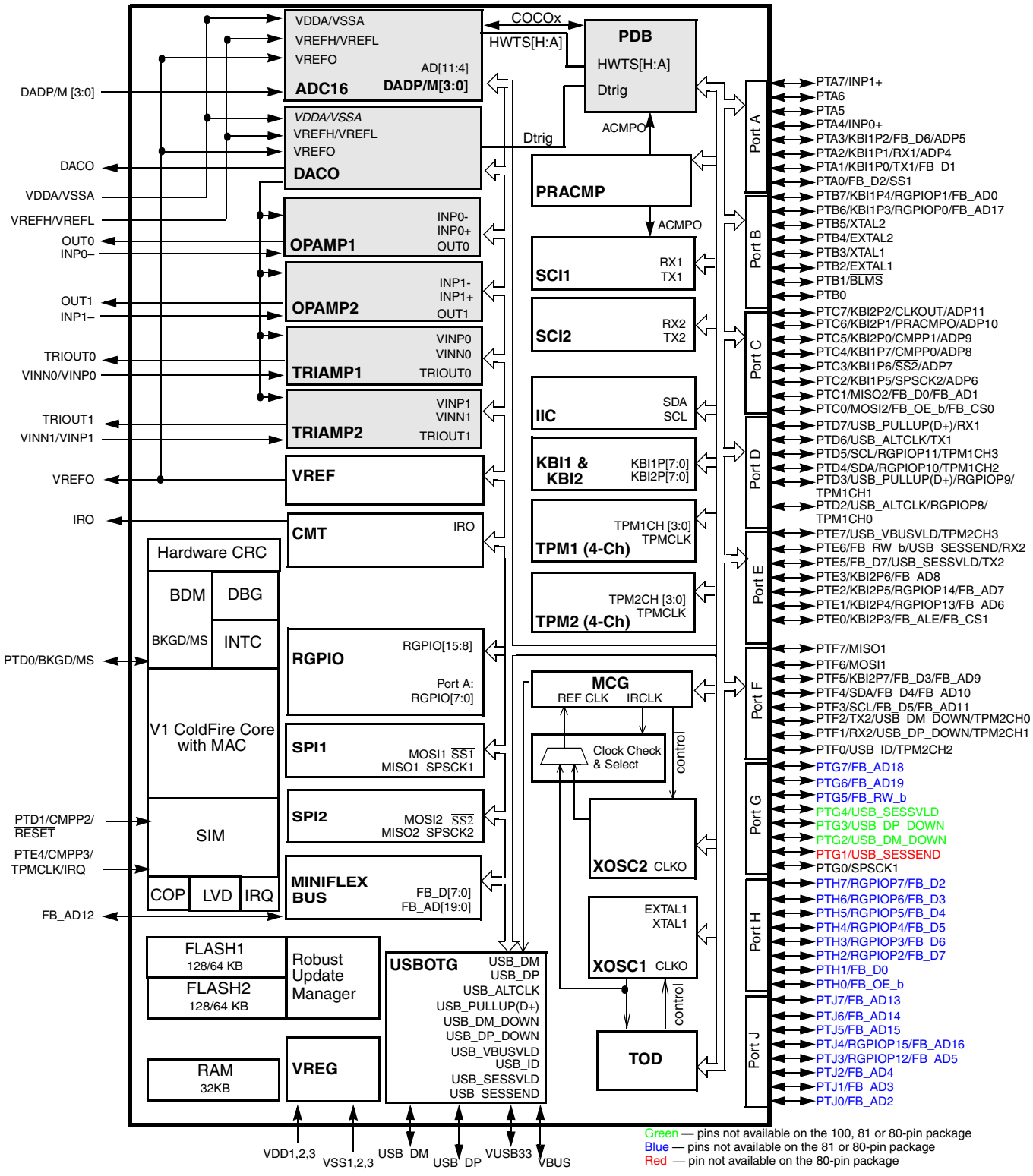


Figure 1. MCF51MM256 Series Block Diagram

The following table describes the functional units of the MCF51MM256/128.

Table 2. MCF51MM256/128 Functional Units

Unit	Function
Measurement Engine	DAC (digital to analog converter) — Used to output voltage levels.
	16-BIT SAR ADC (analog-to-digital converter) — Measures analog voltages at up to 16 bits of resolution. The ADC has up to four differential and 8 single-ended inputs.
	OPAMP — General purpose op amp used for signal filtering or amplification.
	TRIAMP —- Transimpedance amplifier optimized for converting small currents into voltages.
	Measurement Engine PDB — The measurement engine PDB is used to precisely trigger the DAC and the ADC modules to complete sensor biasing and measuring.
Mini-FlexBus	Provides expansion capability for off-chip memory and peripherals.
USB On-the-Go	Supports the USB On-the-Go dual-role controller.
CMT (Carrier Modulator Timer)	Infrared output used for the Remote Controller operation.
MCG (Multipurpose Clock Generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources.
BDM (Background Debug Module)	Provides single pin debugging interface (part of the V1 ColdFire core).
CF1 CORE (V1 ColdFire Core)	Executes programs and interrupt handlers.
PRACMP	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (Computer Operating Properly)	Software Watchdog.
IRQ (Interrupt Request)	Single-pin high-priority interrupt (part of the V1 ColdFire core).
CRC (Cyclic Redundancy Check)	High-speed CRC calculation.
DBG (Debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire. core)
FLASH (Flash Memory)	Provides storage for program code, constants, and variables.
IIC (Inter-integrated Circuits)	Supports standard IIC communications protocol and SMBus.
INTC (Interrupt Controller)	Controls and prioritizes all device interrupts.
KBI1 & KBI2	Keyboard Interfaces 1 and 2.
LVD (Low-voltage Detect)	Provides an interrupt to the ColdFire V1 CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event.
VREF (Voltage Reference)	The Voltage Reference output is available for both on- and off-chip use.
RAM (Random-Access Memory)	Provides stack and variable storage.
RGPIO (Rapid General-purpose Input/output)	Allows for I/O port access at CPU clock speeds. RGPIO is used to implement GPIO functionality.

2.4 80-Pin LQFP

The following figure shows the 80-pin LQFP pinout configuration.

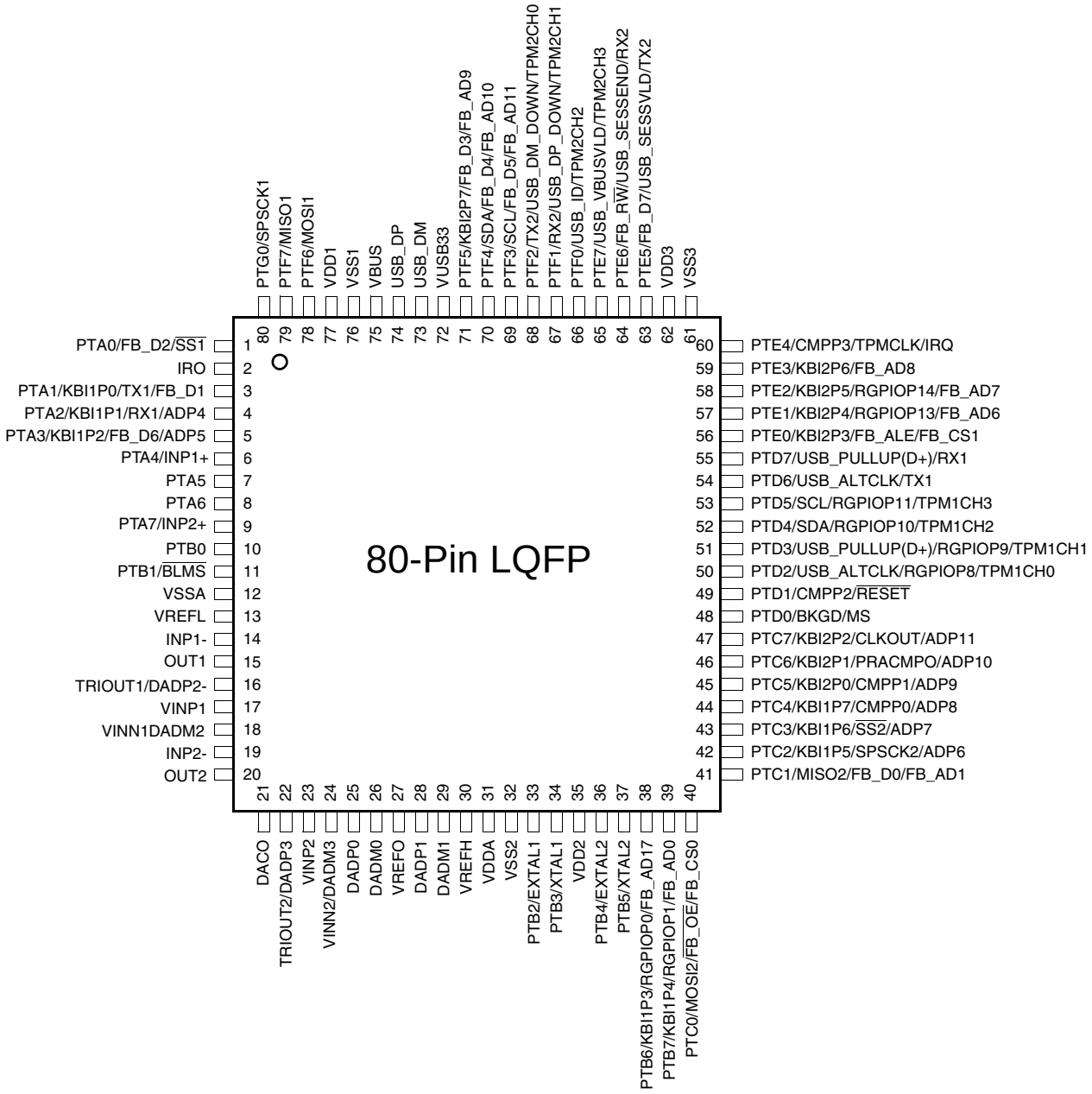


Figure 5. 80-Pin LQFP

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
H11	61	E7	50	PTD2	USB_ALTCLK	RGPIOP8	TPM1CH0	PTD2/USB_ALTCLK/RGPIOP8/TPM1CH0
H10	62	E8	51	PTD3	USB_PULLUP (D+)	RGPIOP9	TPM1CH1	PTD3/USB_PULLUP(D+)/RGPIOP9/TPM1CH1
H9	63	F9	52	PTD4	SDA	RGPIOP10	TPM1CH2	PTD4/SDA/RGPIOP10/TPM1CH2
G9	64	D7	53	PTD5	SCL	RGPIOP11	TPM1CH3	PTD5/SCL/RGPIOP11/TPM1CH3
J8	65	E9	54	PTD6	USB_ALTCLK	TX1	—	PTD6/USB_ALTCLK/TX1
G10	66	D8	55	PTD7	USB_PULLUP (D+)	RX1	—	PTD7/USB_PULLUP(D+) /RX1
G11	67	D9	56	PTE0	KBI2P3	FB_ALE	FB_CS1	PTE0/KBI2P3/FB_ALE/FB_CS1
F10	68	—	—	PTJ0	FB_AD2	—	—	PTJ0/FB_AD2
F11	69	—	—	PTJ1	FB_AD3	—	—	PTJ1/FB_AD3
F9	70	—	—	PTJ2	FB_AD4	—	—	PTJ2/FB_AD4
E10	71	—	—	PTJ3	RGPIOP12	FB_AD5	—	PTJ3/RGPIOP12/FB_AD5
E11	72	C9	57	PTE1	KBI2P4	RGPIOP13	FB_AD6	PTE1/KBI2P4/RGPIOP13/FB_AD6
D11	73	C8	58	PTE2	KBI2P5	RGPIOP14	FB_AD7	PTE2/KBI2P5/RGPIOP14/FB_AD7
D10	74	B9	59	PTE3	KBI2P6	FB_AD8	—	PTE3/KBI2P6/FB_AD8
C9	75	A9	60	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/IRQ
H8	76	F5	61	VSS3	—	—	—	VSS3
D8	77	E5	62	VDD3	—	—	—	VDD3
B8	78	C7	63	PTE5	FB_D7	USB_ SESSVLD	TX2	PTE5/FB_D7/USB_SESSVLD/TX2
C10	79	C6	64	PTE6	FB_R$\overline{W}$	USB_ SESSEND	RX2	PTE6/FB_R$\overline{W}$/USB_SESSEND/RX2
C11	80	B6	65	PTE7	USB_ VBUSVLD	TPM2CH3	—	PTE7/USB_VBUSVLD/TPM2CH3
B9	81	B8	66	PTF0	USB_ID	TPM2CH2	—	PTF0/USB_ID/TPM2CH2
B10	82	B7	67	PTF1	RX2	USB_DP_D OWN	TPM2CH1	PTF1/RX2/USB_DP_DOWN/TPM2CH1
B11	83	C5	68	PTF2	TX2	USB_DM_ DOWN	TPM2CH0	PTF2/TX2/USB_DM_DOWN/TPM2CH0
A11	84	—	—	PTJ4	RGPIOP15	FB_AD16	—	PTJ4/RGPIOP15/FB_AD16
A10	85	—	—	PTJ5	FB_AD15	—	—	PTJ5/FB_AD15
B6	86	—	—	PTJ6	FB_AD14	—	—	PTJ6/FB_AD14
A9	87	—	—	PTJ7	FB_AD13	—	—	PTJ7/FB_AD13

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to +3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating	Value	Unit
1	T_A	Operating temperature range (packaged):		°C
		MCF51MM256	–40 to 105	
		MCF51MM128	–40 to 105	
2	T_{JMAX}	Maximum junction temperature	135	°C
3	θ_{JA}	Thermal resistance[1,2,3,4] Single-layer board — 1s		°C/W
		104-pin MBGA	67	
		100-pin LQFP	53	
		81-pin MBGA	67	
		80-pin LQFP	53	
4	θ_{JA}	Thermal resistance[1, 2, 3, 4] Four-layer board — 2s2p		°C/W
		104-pin MBGA	39	
		100-pin LQFP	41	
		81-pin MBGA	39	
		80-pin LQFP	39	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Junction to Ambient Natural Convection
3 1s — Single layer board, one signal layer
4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

3.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
1	RI_{DD}	Run supply current FEI mode; all modules ON[2]							
			25.165 MHz	3	44	48	mA	–40 to 25	P
			25.165 MHz	3	44	48	mA	105	P
			20 MHz	3	32.3	—	mA	–40 to 105	T
			8 MHz	3	16.4	—	mA	–40 to 105	T
			1 MHz	3	2.9	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode; all modules OFF[3]							
			25.165 MHz	3	29	29.6	mA	–40 to 105	C
			20 MHz	3	25.4	—	mA	–40 to 105	T
			8 MHz	3	12.7	—	mA	–40 to 105	T
			1 MHz	3	2.4	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPR=0; all modules OFF[3]							
			16 kHz FBI	3	232	280	µA	–40 to 105	T
			16 kHz FBE	3	231	296	µA	–40 to 105	T
4	RI_{DD}	Run supply current LPR=1, all modules OFF[3]							
			16 kHz BLPE	3	74	75	µA	0 to 70	T
			16 kHz BLPE	3	74	120	µA	–40 to 105	T

Table 10. Supply Current Characteristics (continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
8	$S3I_{DD}$	Stop3 mode supply current[4] No clocks active	n/a	3	0.750	1.3	μA	–40 to 25	P
					8.5	18		70	C
					20	28		85	C
					53	63		105	P
				2	0.400	0.900		–40 to 25	C
					8.2	16		70	C
					18	26		85	C
					47	59		105	C

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 ON = System Clock Gating Control registers turn on system clock to the corresponding modules.

3 OFF = System Clock Gating Control registers turn off system Clock to the corresponding modules.

4 All digital pins must be configured to a known state to prevent floating pins from adding current. Smaller packages may have some pins that are not bonded out; however, software must still be configured to the largest pin package available so that all pins are in a known state. Otherwise, floating pins that are not bonded in the smaller packages may result in a higher current draw. NOTE: I/O pins are configured to output low; input-only pins are configured to pullup-enabled. IRO pin connects to ground. FB_AD12 pin is pullup-enabled. TRIAMPx, OPAMPx, DACO, and VREFO pins are at reset state and unconnected.

Table 11. Typical Stop Mode Adders

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600	650	750	850	1000	nA	D
3	IREFSTEN[1]	—	—	73	80	93	125	μA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D
5	LVD[1]	LVDSE = 1	116	117	126	132	172	μA	T
6	PRACMP[1]	Not using the bandgap (BGBE = 0)	17	18	24	35	74	μA	T
7	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	190	195	210	220	260	μA	T
8	DAC[1]	High-Power mode; no load on DACO	339	345	346	346	360	μA	T
		Low-Power mode	41	43	43	44	50	μA	T
9	OPAMP[1]	High-Power mode	276	350	370	376	390	μA	T
		Low-Power mode	42	49	57	58	68	μA	T
10	TRIAMP[1]	High-Power mode	420	432	433	438	478	μA	T
		Low-Power mode	52	52	52	55	60	μA	T

1 Not available in stop2 mode.

3.7 PRACMP Electricals

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V_{PWR}	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	80	μA	D
3	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	μA	D
4	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA	D
5	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V	D
6	Analog input offset voltage	VAIO	—	5	40	mV	D
7	Analog comparator hysteresis	V_H	3.0	—	20.0	mV	D
8	Analog input leakage current	I_{ALKG}	—	—	1	nA	D
9	Analog comparator initialization delay	tAINIT	—	—	1.0	μs	D
10	Programmable reference generator inputs	V_{In2} (V_{DD25})	1.8	—	2.75	V	D
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	μs	D
12	Programmable reference generator step size	Vstep	0.75	1	1.25	LSB	D
13	Programmable reference generator voltage range	Vprgout	V_{In}/32	—	V_{in}	V	P

3.8 12-Bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	V_{DDA}	1.8	3.6	V	P	
2	Reference voltage	V_{DACR}	1.15	3.6	V	C	
3	Temperature	T_A	–40	105	°C	C	
4	Output load capacitance	C_L	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	I_L	—	1	mA	C	

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Min	Typ	Max	Unit	C	Notes
1	Resolution	N	12	—	12	bit	T	

Table 14. DAC 12-Bit Operating Behaviors (continued)

#	Characteristic	Symbol	Min	Typ	Max	Unit	C	Notes
2	Supply current low-power mode	I_{DDA_DACLP}	—	50	100	µA	T	
3	Supply current high-power mode	I_{DDA_DACHP}	—	345	500	µA	T	
4	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$Ts_{FS}LP$	—	—	200	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
5	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$Ts_{FS}HP$	—	—	30	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
6	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$Ts_{C-C}LP$	—	—	5	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
7	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode (3 V at Room Temperature)	$Ts_{C-C}HP$	—	1	—	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
8	DAC output voltage range low (high-power mode, no load, DAC set to 0) (3 V at Room Temperature)	$V_{dacoutl}$	—	—	100	mV	T	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	V_{DACR} -100	—	—	mV	T	
10	Integral non-linearity error	INL	—	—	± 8	LSB	T	
11	Differential non-linearity error VDACR is > 2.4 V	DNL	—	—	± 1	LSB	T	
12	Offset error	E_O	—	±0.4	± 3	%FSR	T	Calculated by a best fit curve from V_{SS} + 100mV to V_{REFH} –100mV
13	Gain error, $V_{REFH} = V_{ext} = V_{DD}$	E_G	—	±0.1	± 0.5	%FSR	T	Calculated by a best fit curve from V_{SS} + 100mV to V_{REFH} –100mV

Table 15. 16-Bit ADC Operating Conditions (continued)

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
5	V_{REFL}	Ref Voltage Low		V_{SSA}	V_{SSA}	V_{SSA}	V	D	
6	V_{ADIN}	Input Voltage		V_{REFL}	—	V_{REFH}	V	D	
7	C_{ADIN}	Input Capacitance	16-bit modes 8/10/12-bit modes	—	8 4	10 5	pF	T	
8	R_{ADIN}	Input Resistance		—	2	5	kΩ	T	
9	R_{AS}	Analog Source Resistance							External to MCU Assumes ADLSMP=0
		16-bit mode	f_{ADCK} > 8 MHz	—	—	0.5	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	1	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	2	kΩ	T	
		13/12-bit mode	f_{ADCK} > 8 MHz	—	—	1	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	2	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	5	kΩ	T	
		11/10-bit mode	f_{ADCK} > 8 MHz	—	—	2	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	10	kΩ	T	
		9/8-bit mode	f_{ADCK} > 8 MHz	—	—	5	kΩ	T	
			f_{ADCK} < 8 MHz	—	—	10	kΩ	T	
10	f_{ADCK}	ADC Conversion Clock Frequency							
		ADLPC=0, ADHSC=1		1.0	—	8.0	MHz	D	
		ADLPC=0, ADHSC=0		1.0	—	5.0	MHz	D	
		ADLPC=1, ADHSC=0		1.0	—	2.5	MHz	D	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq$ 8 MHz, –40 to 85 °C) (continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
14	Total Harmonic Distortion	16-bit differential mode Avg=32	THD	—	–91.5	–74.3	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	–85.5	—		D	
15	Spurious Free Dynamic Range	16-bit differential mode Avg=32	SFDR	75.0	92.2	—	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	86.2	—		D	
16	Input Leakage Error	all modes	E_{IL}	$I_{In} * R_{AS}$			mV	D	I_{In} = leakage current (refer to DC characteristics)
17	Temp Sensor Slope	–40°C – 25°C	m	—	1.646	—	mV/×C	C	
		25°C – 125°C		—	1.769	—			
18	Temp Sensor Voltage	25°C	V_{TEMP25}	—	718.2	—	mV	C	

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}$

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

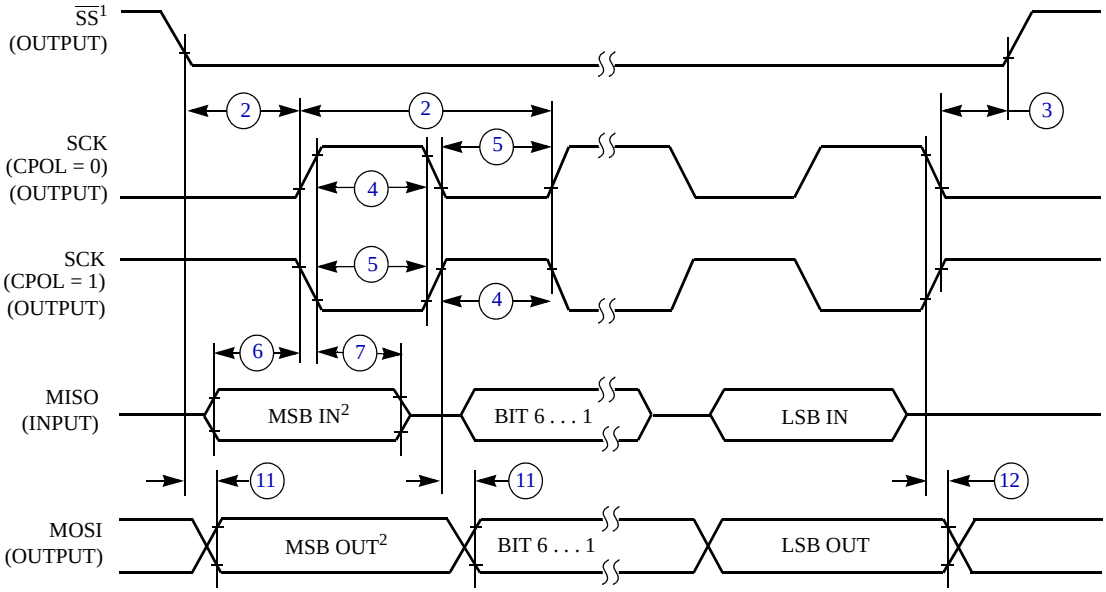
5 625 ns represents 5 time quanta for CAN applications, under worst-case conditions of 8 MHz CAN bus clock, 1 Mbps CAN Bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

6 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

7 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

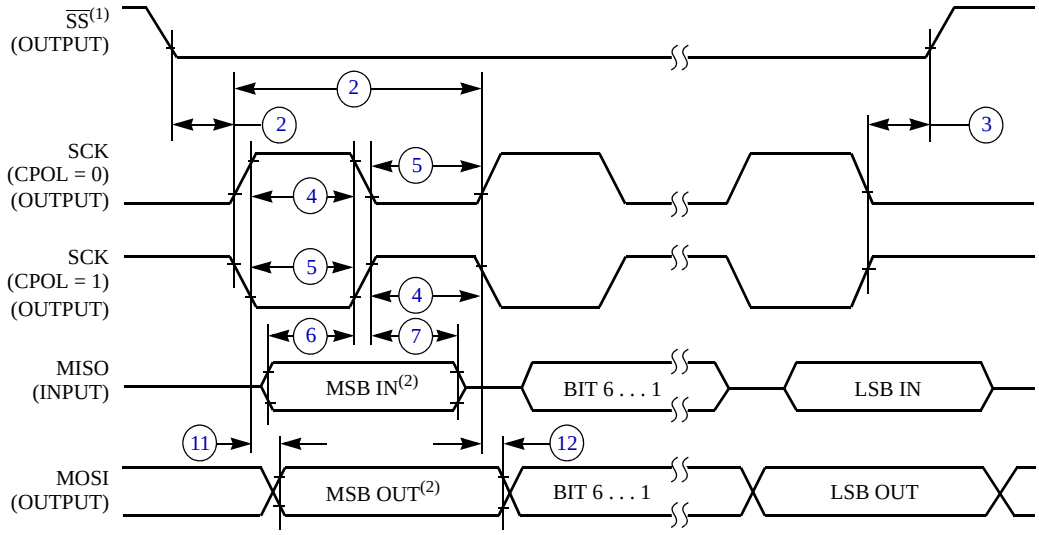
Table 19. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit	C
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz	D
		• High range (RANGE = 1), • FEE or FBE mode [2]	f_{hi-fll}	1	—	5	MHz	D
		• High range (RANGE = 1), • PEE or PBE mode [3]	f_{hi-pll}	1	—	16	MHz	D
		• High range (RANGE = 1), • High gain (HGO = 1), • BLPE mode	f_{hi-hgo}	1	—	16	MHz	D
		• High range (RANGE = 1), • Low power (HGO = 0), • BLPE mode	f_{hi-lp}	1	—	8	MHz	D
2	Load capacitors		C_1 C_2	See crystal or resonator manufacturer's recommendation.				D
3	Feedback resistor	• Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ	D
		• High range (1 MHz to 16 MHz)	—	—	1	—		D
4	Series resistor — Low range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)		—	100	—		D
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)						D
		≥ 8 MHz		—	0	0		D
		4 MHz		—	0	10		D
		1 MHz		—	0	20		D



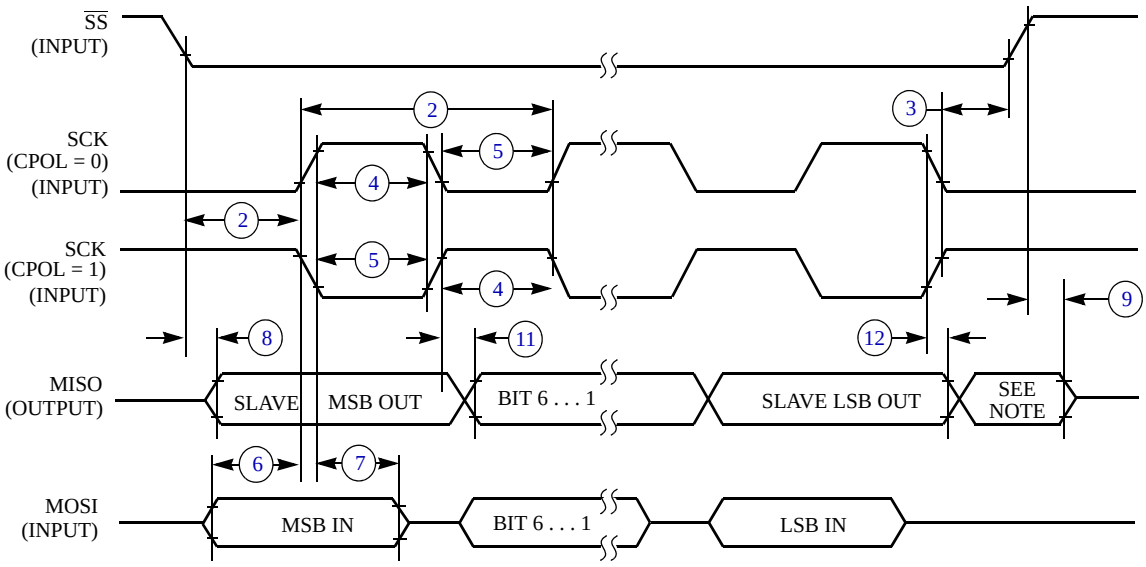
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

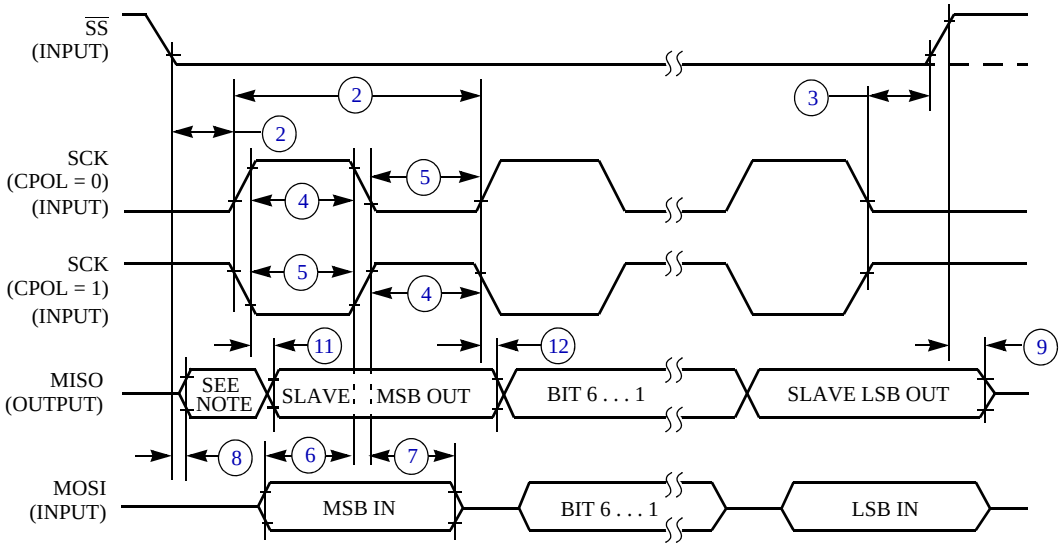
Figure 16. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined, but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51MM256RM).

Table 24. Flash Characteristics

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage for program/erase –40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 25. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

3.17 TRIAMP Electrical Parameters

Table 28. TRIAMP Characteristics 1.8–3.6 V, –40°C~105°C

#	Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit	C
1	Operating Voltage	V_{DD}	1.8	—	3.6	V	C
2	Supply Current (I_{OUT}=0mA, CL=0) Low-power mode	I_{SUPPLY}	—	52	60	μA	T
3	Supply Current (I_{OUT}=0mA, CL=0) High-speed mode	I_{SUPPLY}	—	432	480	μA	T
4	Input Offset Voltage	V_{OS}	—	± 1	± 5	mV	T
5	Input Offset Voltage Temperature Drift	α_{VOS}	—	600	—	μV	T
6	Input Offset Current	I_{OS}	—	±120	500	pA	T
7	Input Bias Current (0 ~ 50°C)	I_{BIAS}	—	< 350	< ±500	pA	T
8	Input Bias Current (–40 ~ 105°C)	I_{BIAS}	—	3	6.55	nA	T
9	Input Common Mode Voltage Low	V_{CML}	0	—	—	V	T
10	Input Common Mode Voltage High	V_{CMH}	—	—	V_{DD}–1.4	V	T
11	Input Resistance	R_{IN}	500	—	—	MΩ	T
12	Input Capacitances	C_{IN}	—	—	5	pF	D
13	AC Input Impedance (f_{IN}=100kHz)	$\|X_{IN}\|$	—	1	—	MΩ	D
14	Input Common Mode Rejection Ratio	CMRR	60	70	—	dB	T
15	Power Supply Rejection Ration	PSRR	60	70	—	dB	T
16	Slew Rate (ΔV_{IN}=100mV) Low-power mode	SR	—	0.1	—	V/μs	T
17	Slew Rate (ΔV_{IN}=100mV) High-speed mode	SR	—	1	—	V/μs	T
18	Unity Gain Bandwidth (Low-power mode) 50pF	GBW	0.15	0.25	—	MHz	T
19	Unity Gain Bandwidth (High-speed mode) 50pF	GBW	—	1.6	—	MHz	T
20	DC Open Loop Voltage Gain	A_V	—	80	—	dB	T
21	Load Capacitance Driving Capability	CL(max)	—	—	100	pF	T
22	Output Impedance AC Open Loop (@100 kHz Low-power mode)	R_{OUT}	—	1.4	—	kΩ	D
23	Output Impedance AC Open Loop (@100 kHz High-speed mode)	R_{OUT}	—	184	—	Ω	D
24	Output Voltage Range	triout	0.15	—	V_{DD} – 0.15	V	T
25	Output Drive Capability	I_{OUT}	—	± 1.0	—	mA	T
26	Gain Margin	GM	20	—	—	dB	D
27	Phase Margin	PM	45	55	—	deg	T

4 Ordering Information

This section contains ordering information for the device numbering system. See Table 1 for feature summary by package information.

4.1 Part Numbers

Table 30. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51MM256VML	MCF51MM256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 105 °C
MCF51MM256VLL	MCF51MM256 ColdFire Microcontroller	256K/32K	100 LQFP	–40 to 105 °C
MCF51MM256VMB	MCF51MM256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 105 °C
MCF51MM256VLK	MCF51MM256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 105 °C
MCF51MM128VMB	MCF51MM128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 105 °C
MCF51MM128VLK	MCF51MM128 ColdFire Microcontroller	128K/32K	80 LQFP	–40 to 105 °C

4.2 Package Information

Table 31. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
100	Low Quad Flat Package	LQFP	LL	983-03	98ASS23308W
80	Low Quad Flat Package	LQFP	LK	1418	98ASS23174W
104	MAP BGA Package	MAPBGA	ML	1285-02	98ARH98267A
81	MAP BGA Package	MAPBGA	MB	1662-01	98ASA10670D

4.3 Mechanical Drawings

Table 31 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51MM256/128 Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 31, or
- Open a browser to the Freescale website (http://www.freescale.com), and enter the appropriate document number (from Table 31) in the “Enter Keyword” search box at the top of the page.

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