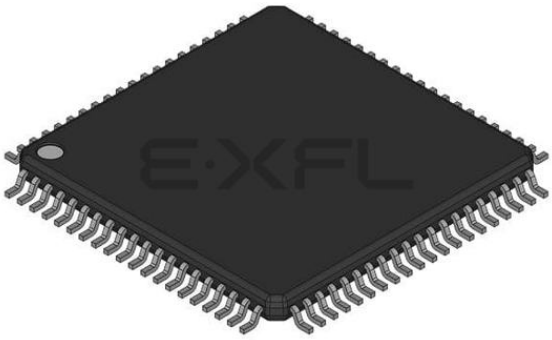

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x16b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51mm128vlk

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The following table describes the functional units of the MCF51MM256/128.

Table 2. MCF51MM256/128 Functional Units

Unit	Function
Measurement Engine	DAC (digital to analog converter) — Used to output voltage levels.
	16-BIT SAR ADC (analog-to-digital converter) — Measures analog voltages at up to 16 bits of resolution. The ADC has up to four differential and 8 single-ended inputs.
	OPAMP — General purpose op amp used for signal filtering or amplification.
	TRIAMP —- Transimpedance amplifier optimized for converting small currents into voltages.
	Measurement Engine PDB — The measurement engine PDB is used to precisely trigger the DAC and the ADC modules to complete sensor biasing and measuring.
Mini-FlexBus	Provides expansion capability for off-chip memory and peripherals.
USB On-the-Go	Supports the USB On-the-Go dual-role controller.
CMT (Carrier Modulator Timer)	Infrared output used for the Remote Controller operation.
MCG (Multipurpose Clock Generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources.
BDM (Background Debug Module)	Provides single pin debugging interface (part of the V1 ColdFire core).
CF1 CORE (V1 ColdFire Core)	Executes programs and interrupt handlers.
PRACMP	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (Computer Operating Properly)	Software Watchdog.
IRQ (Interrupt Request)	Single-pin high-priority interrupt (part of the V1 ColdFire core).
CRC (Cyclic Redundancy Check)	High-speed CRC calculation.
DBG (Debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire. core)
FLASH (Flash Memory)	Provides storage for program code, constants, and variables.
IIC (Inter-integrated Circuits)	Supports standard IIC communications protocol and SMBus.
INTC (Interrupt Controller)	Controls and prioritizes all device interrupts.
KBI1 & KBI2	Keyboard Interfaces 1 and 2.
LVD (Low-voltage Detect)	Provides an interrupt to the ColdFire V1 CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event.
VREF (Voltage Reference)	The Voltage Reference output is available for both on- and off-chip use.
RAM (Random-Access Memory)	Provides stack and variable storage.
RGPIO (Rapid General-purpose Input/output)	Allows for I/O port access at CPU clock speeds. RGPIO is used to implement GPIO functionality.

Table 2. MCF51MM256/128 Functional Units (continued)

Unit	Function
SCI1, SCI2 (Serial Communications Interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols.
SIM (system integration unit)	
SPI1 (FIFO), SPI2 (Serial Peripheral Interfaces)	SPI1 and SPI2 provide standard master/slave capability. SPI contains a FIFO buffer in order to increase the throughput for this peripheral.
TPM1, TPM2 (Timer/PWM Module)	Timer/PWM module can be used for a variety of generic timer operations as well as pulse-width modulation.
VREG (Voltage Regulator)	Controls power management across the device.
XOSC1 and XOSC2 (Crystal Oscillators)	These devices incorporate redundant crystal oscillators. One is intended primarily for use by the TOD, and the other by the CPU and other peripherals.

2.5 Pin Assignments

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
B2	1	B2	1	PTA0	FB_D2	$\overline{SS1}$	—	PTA0/FB_D2/$\overline{SS1}$
C1	2	A1	2	IRO	—	—	—	IRO
C6	3	—	—	PTG5	FB_$\overline{RW}$	—	—	PTG5/FB_$\overline{RW}$
C5	4	—	—	PTG6	FB_AD19	—	—	PTG6/FB_AD19
C7	5	—	—	PTG7	FB_AD18	—	—	PTG7/FB_AD18
B7	6	—	—	PTH0	$\overline{FB\_OE}$	—	—	PTH0/$\overline{FB\_OE}$
C8	7	—	—	PTH1	FB_D0	—	—	PTH1/FB_D0
D9	8	C4	3	PTA1	KBI1P0	TX1	FB_D1	PTA1/KBI1P0/TX1/FB_D1
E9	9	D5	4	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
H3	10	D6	5	PTA3	KBI1P2	FB_D6	ADP5	PTA3/KBI1P2/FB_D6/ADP5
D2	11	C1	6	PTA4	INP1+	—	—	PTA4/INP1+
D1	12	C2	7	PTA5	—	—	—	PTA5
C3	13	C3	8	PTA6	—	—	—	PTA6
E2	14	D2	9	PTA7	INP2+	—	—	PTA7/INP2+
E3	15	D3	10	PTB0	—	—	—	PTB0
D3	16	D4	11	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
E1	17	J1	12	VSSA	—	—	—	VSSA
F1	18	J2	13	VREFL	—	—	—	VREFL
F2	19	D1	14	INP1-	—	—	—	INP1-
G2	20	E1	15	OUT1	—	—	—	OUT1
G1	21	F2	16	DADP2	TRIOUT1	—	—	DADP2/TRIOUT1
H1	22	F1	17	VINP1	—	—	—	VINP1
H2	23	E2	18	DADM2	VINN1	—	—	DADM2/VINN1
F3	24	F3	19	INP2-	—	—	—	INP2-
G3	25	E3	20	OUT2	—	—	—	OUT2
L2	26	G2	21	DACO	—	—	—	DACO
L1	27	G3	22	DADP3	TRIOUT2	—	—	DADP3/TRIOUT2
K1	28	H4	23	VINP2	—	—	—	VINP2
K2	29	G4	24	DADM3	VINN2	—	—	DADM3/VINN2

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
A8	88	—	—	FB_AD12	—	—	—	FB_AD12
A7	89	A8	69	PTF3	SCL	FB_D5	FB_AD11	PTF3/SCL/FB_D5/FB_AD11
A6	90	A7	70	PTF4	SDA	FB_D4	FB_AD10	PTF4/SDA/FB_D4/FB_AD10
B5	91	B5	71	PTF5	KBI2P7	FB_D3	FB_AD9	PTF5/KBI2P7/FB_D3/FB_AD9
A5	92	A6	72	VUSB33	—	—	—	VUSB33
A4	93	B4	73	USB_DM	—	—	—	USB_DM
A3	94	A4	74	USB_DP	—	—	—	USB_DP
B4	95	A5	75	VBUS	—	—	—	VBUS
H4	96	F6	76	VSS1	—	—	—	VSS1
D4	97	E6	77	VDD1	—	—	—	VDD1
A1	98	A3	78	PTF6	MOSI1	—	—	PTF6/MOSI1
A2	99	B1	79	PTF7	MISO1	—	—	PTF7/MISO1
B1	100	A2	80	PTG0	SPSCK1	—	—	PTG0/SPSCK1
F4	—	A1	—	PTG1	USB_ SESSEND	—	—	PTG1/USB_SESSEND
C4	—	—	—	PTG2	USB_DM_ DOWN	—	—	PTG2/USB_DM_DOWN
B3	—	—	—	PTG3	USB_DP_ DOWN	—	—	PTG3/USB_DP_DOWN
C2	—	—	—	PTG4	USB_SESSVLD	—	—	PTG4/USB_SESSVLD

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to +3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

3.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
1	—	Operating Voltage	—	1.8[2]	—	3.6	V	—
2	V_{OH}	Output high voltage	All I/O pins, low-drive strength					
			$V_{DD} \geq 1.8$ V, $I_{Load} = -600$ μA	$V_{DD} - 0.5$	—	—	V	C
			All I/O pins, high-drive strength					
			$V_{DD} \geq 2.7$ V, $I_{Load} = -10$ mA	$V_{DD} - 0.5$	—	—	V	P
			$V_{DD} \geq 2.3$ V, $I_{Load} = -6$ mA	$V_{DD} - 0.5$	—	—	V	T
			$V_{DD} \geq 1.8$V, $I_{Load} = -3$ mA	$V_{DD} - 0.5$	—	—	V	C
3	I_{OHT}	Output high current	Max total I_{OH} for all ports					
			—	—	—	100	mA	D
4	V_{OL}	Output low voltage	All I/O pins, low-drive strength					
			$V_{DD} \geq 1.8$ V, $I_{Load} = 600$ μA	—	—	0.5	V	C
			All I/O pins, high-drive strength					
			$V_{DD} \geq 2.7$ V, $I_{Load} = 10$ mA	—	—	0.5	V	P
			$V_{DD} \geq 2.3$ V, $I_{Load} = 6$ mA	—	—	0.5	V	T
			$V_{DD} \geq 1.8$ V, $I_{Load} = 3$ mA	—	—	0.5	V	C
5	I_{OLT}	Output low current	Max total I_{OL} for all ports	—	—	—	100	mA	D
6	V_{IH}	Input high voltage	all digital inputs					
			$V_{DD} > 2.7$ V	0.70 x V_{DD}	—	—	V	P
			$V_{DD} > 1.8$ V	0.85 x V_{DD}	—	—	V	C

Table 9. DC Characteristics (continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
7	V_{IL}	Input low voltage — all digital inputs						
			V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	V	P
			V_{DD} >1.8 V	—	—	0.30 x V_{DD}	V	C
8	V_{hys}	Input hysteresis — all digital inputs	—	0.06 x V_{DD}	—	—	mV	C
9	$\|I_{In}\|$	Input leakage current — all input only pins (Per pin)	V_{In} = V_{DD} or V_{SS}	—	—	0.5	μA	P
10	$\|I_{OZ}\|$	Hi-Z (off-state) leakage current[3] — all digital input/output (per pin)	V_{In} = V_{DD} or V_{SS}	—	0.003	0.5	μA	P
11	R_{PU}	Pull-up resistors — all digital inputs, when enabled	—	17.5	—	52.5	kΩ	P
12	R_{PD}	Internal pull-down resistors[4]	—	17.5	—	52.5	kΩ	P
13	I_{IC}	DC injection current [5, 6, 7] — Single pin limit						
			V_{SS} > V_{IN} > V_{DD}	–0.2	—	0.2	mA	D
		Total MCU limit, includes sum of all stressed pins						
			V_{SS} > V_{IN} > V_{DD}	–5	—	5	mA	D
14	C_{In}	Input Capacitance, all pins	—	—	—	8	pF	C
15	V_{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C
16	V_{POR}	POR re-arm voltage[8]	—	0.9	1.4	1.79	V	C
17	t_{POR}	POR re-arm time	—	10	—	—	μs	D
18	V_{LVDH}[9]	Low-voltage detection threshold — high range — V_{DD} falling						
			—	2.11	2.16	2.22	V	P
		V_{DD} rising						
			—	2.16	2.21	2.27	V	P
19	V_{LVDL}	Low-voltage detection threshold — low range[9] — V_{DD} falling						
			—	1.80	1.82	1.91	V	P
		V_{DD} rising						
			—	1.86	1.90	1.99	V	P

3.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
1	RI_{DD}	Run supply current FEI mode; all modules ON[2]							
			25.165 MHz	3	44	48	mA	–40 to 25	P
			25.165 MHz	3	44	48	mA	105	P
			20 MHz	3	32.3	—	mA	–40 to 105	T
			8 MHz	3	16.4	—	mA	–40 to 105	T
			1 MHz	3	2.9	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode; all modules OFF[3]							
			25.165 MHz	3	29	29.6	mA	–40 to 105	C
			20 MHz	3	25.4	—	mA	–40 to 105	T
			8 MHz	3	12.7	—	mA	–40 to 105	T
			1 MHz	3	2.4	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPR=0; all modules OFF[3]							
			16 kHz FBI	3	232	280	µA	–40 to 105	T
			16 kHz FBE	3	231	296	µA	–40 to 105	T
4	RI_{DD}	Run supply current LPR=1, all modules OFF[3]							
			16 kHz BLPE	3	74	75	µA	0 to 70	T
			16 kHz BLPE	3	74	120	µA	–40 to 105	T

Table 10. Supply Current Characteristics (continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	16.5	—	mA	–40 to 105	C
			20 MHz	3	10.3	—	mA	–40 to 105	T
			8 MHz	3	6.6	—	mA	–40 to 105	T
			1 MHz	3	1.7	—	mA	–40 to 105	T
6	$LPWI_{DD}$	Low-Power Wait mode supply current							
			16 KHz	3	28	62	µA	–40 to 105	T
7	$S2I_{DD}$	Stop2 mode supply current[4]							
			N/A	3	0.410	1.00	µA	–40 to 25	P
			N/A	3	3.7	10	µA	70	C
			N/A	3	10	20	µA	85	C
			N/A	3	21	31.5	µA	105	P
			N/A	2	0.410	0.640	µA	–40 to 25	C
			N/A	2	3.4	9	µA	70	C
			N/A	2	9.5	18	µA	85	C
			N/A	2	20	30	µA	105	C

Table 14. DAC 12-Bit Operating Behaviors (continued)

#	Characteristic	Symbol	Min	Typ	Max	Unit	C	Notes
14	Power supply rejection ratio $V_{DD} \geq 2.4$ V	PSRR	60	—	—	dB	T	
15	Temperature drift of offset voltage (DAC set to 0x0800)	T_{co}	—	—	2	mV	T	See Typical Drift figure that follows.
16	Offset aging coefficient	A_c	—	—	8	µV/yr	T	

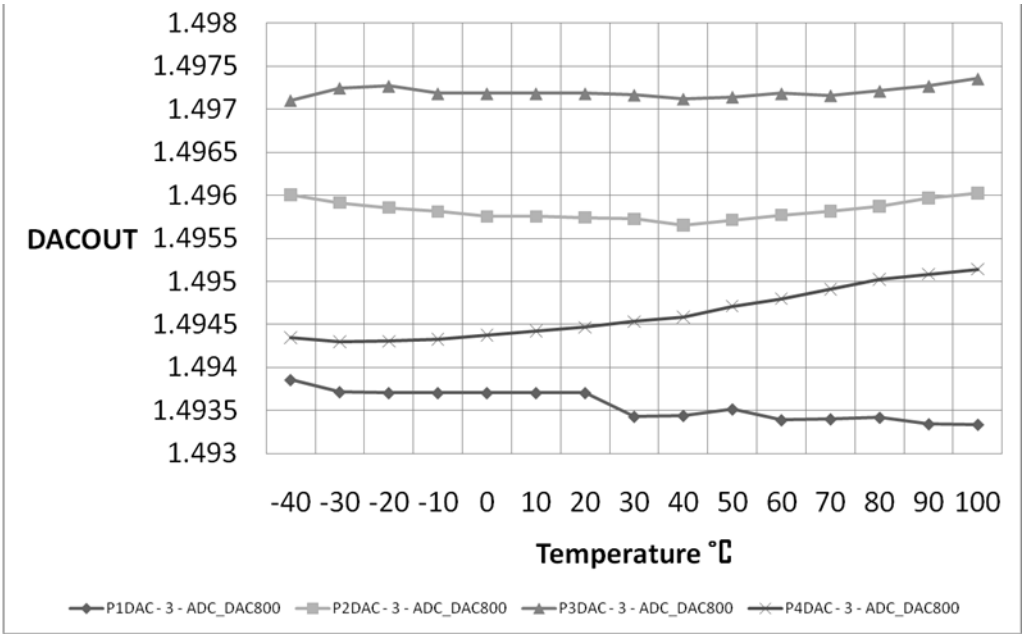


Figure 7. Offset at Half Scale vs Temperature

3.9 ADC Characteristics

Table 15. 16-Bit ADC Operating Conditions

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
1	V_{DDA}	Supply voltage	Absolute	1.8	—	3.6	V	D	
2	ΔV_{DDA}		Delta to V_{DD} (V_{DD}–V_{DDA})[2]	–100	0	+100	mV	D	
3	ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	–100	0	+100	mV	D	
4	V_{REFH}	Ref Voltage High		1.15	V_{DDA}	V_{DDA}	V	D	

Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq$ 8 MHz, –40 to 85 °C)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	215	—	μA	T	ADLSMP =0 ADCO=1
		ADLPC=0, ADHSC=0		—	470	—			
		ADLPC=0, ADHSC=1		—	610	—			
2	Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	—	μA	T	
3	ADC Asynchronous Clock Source	ADLPC=1, ADHSC=0	f_{ADACK}	—	2.4	—	MHz	C	$t_{ADACK} = 1/f_{ADACK}$
		ADLPC=0, ADHSC=0		—	5.2	—			
		ADLPC=0, ADHSC=1		—	6.2	—			
4	Sample Time	See Reference Manual for sample times							
5	Conversion Time	See Reference Manual for conversion times							
6	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+48/ –40 +56/ –28	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±3.0 ±3.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.5 ±1.5		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
7	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	+5/–3 +5/–3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, $f_{ADACK} \leq 4$ MHz, ADHSC = 1) (continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
5	Full-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	T	$V_{ADIN} = V_{DDA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
6	Quantization Error	16-bit modes	E_Q	—	–1 to 0	—	LSB[2]	D	
		≤13-bit modes		—	—	±0.5			
7	Effective Number of Bits	16-bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	ENOB	 14.3 13.8 13.4 13.1 12.4	 14.5 14.0 13.7 13.4 12.6	 — — — — —	Bits	C	$F_{in} = F_{sample}/100$
8	Signal to Noise plus Distortion	See ENOB	SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB		
9	Total Harmonic Distortion	16-bit differential mode Avg=32	THD	—	–95.8	–90.4	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
10	Spurious Free Dynamic Range	16-bit differential mode Avg=32	SFDR	91.0	96.5	—	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
11	Input Leakage Error	all modes	E_{IL}	$I_{In} * R_{AS}$			mV	D	I_{In} = leakage current (refer to DC characteristics)

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}$

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

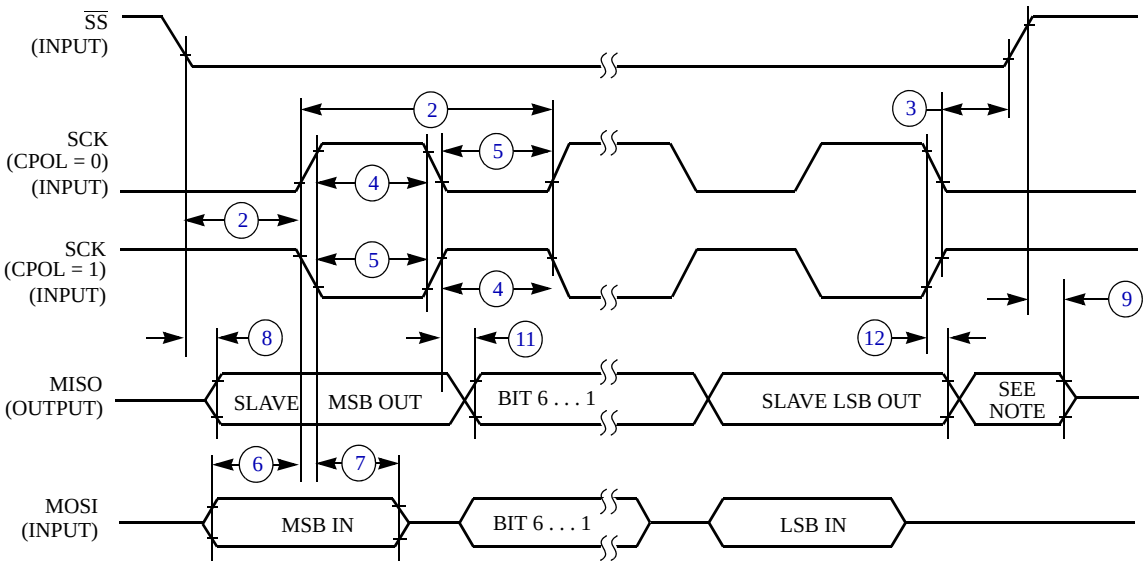
5 625 ns represents 5 time quanta for CAN applications, under worst-case conditions of 8 MHz CAN bus clock, 1 Mbps CAN Bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

6 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

7 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

Table 19. XOSC (Temperature Range = –40 to 105°C Ambient)

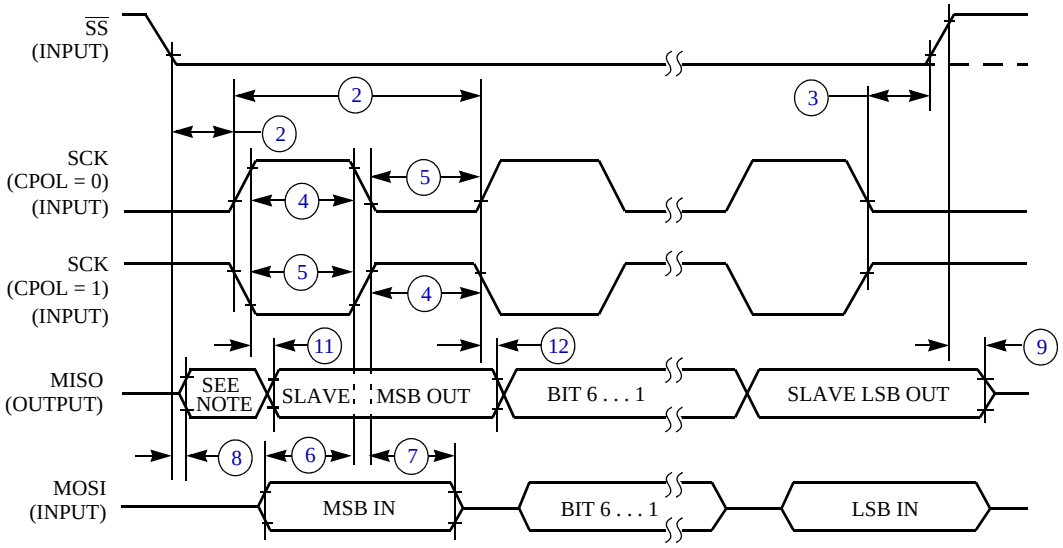
#	Characteristic		Symbol	Min	Typ[1]	Max	Unit	C
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz	D
		• High range (RANGE = 1), • FEE or FBE mode [2]	f_{hi-fll}	1	—	5	MHz	D
		• High range (RANGE = 1), • PEE or PBE mode [3]	f_{hi-pll}	1	—	16	MHz	D
		• High range (RANGE = 1), • High gain (HGO = 1), • BLPE mode	f_{hi-hgo}	1	—	16	MHz	D
		• High range (RANGE = 1), • Low power (HGO = 0), • BLPE mode	f_{hi-lp}	1	—	8	MHz	D
2	Load capacitors		C_1 C_2	See crystal or resonator manufacturer's recommendation.				D
3	Feedback resistor	• Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ	D
		• High range (1 MHz to 16 MHz)	—	—	1	—		D
4	Series resistor — Low range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)		—	100	—		D
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)						D
		≥ 8 MHz		—	0	0		D
		4 MHz		—	0	10		D
		1 MHz		—	0	20		D



NOTE:

1. Not defined, but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51MM256RM).

Table 24. Flash Characteristics

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage for program/erase –40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 25. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

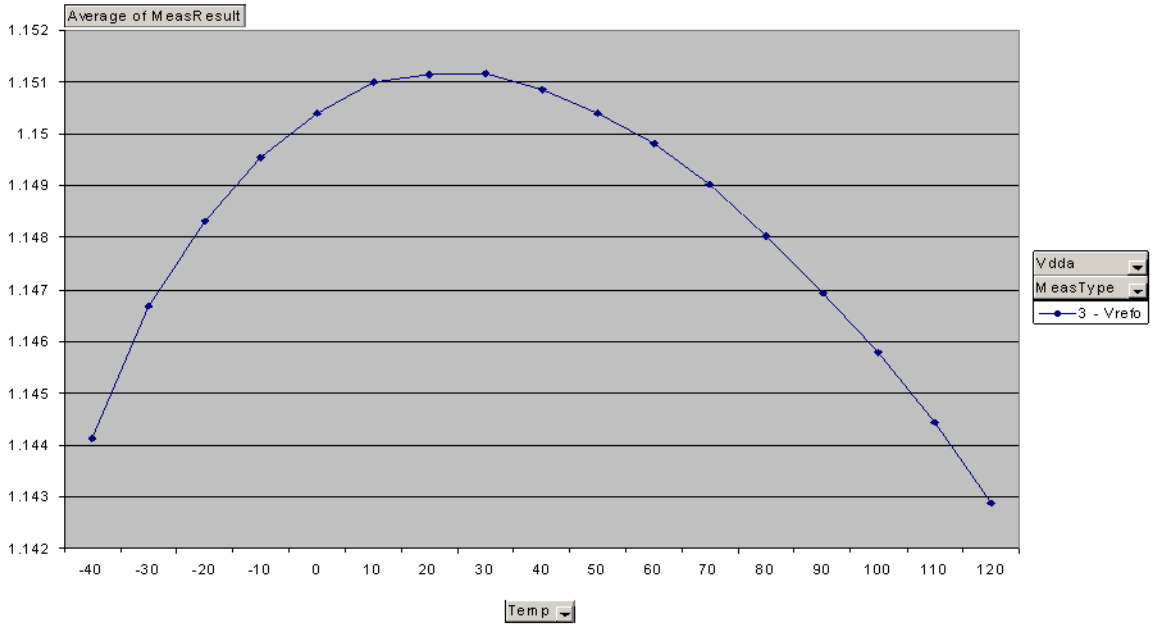


Figure 19. Typical VREF Output vs. Temperature

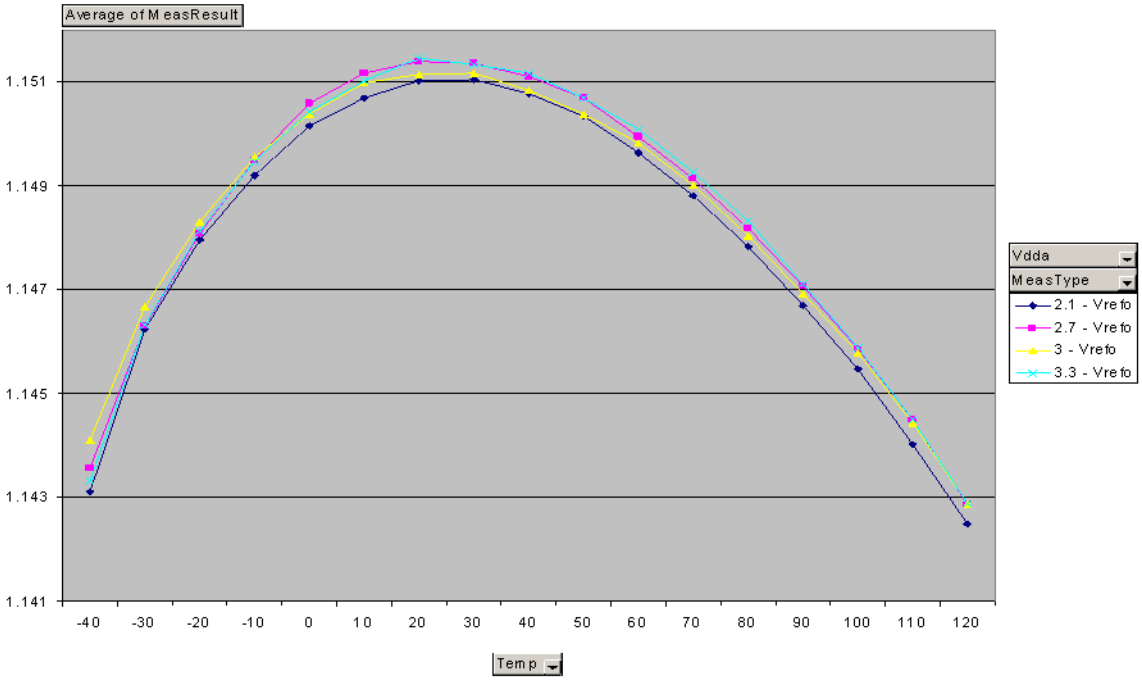


Figure 20. Typical VREF Output vs. V_{DD}

Table 28. TRIAMP Characteristics 1.8–3.6 V, –40°C~105°C (continued)

#	Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit	C
28	Input Voltage Noise Density	f= 1 kHz	—	160	—	nV/√Hz	T

1 All parameters are measured at 3.0 V, CL= 47 pF across temperature –40 to + 105 °C unless specified.
2 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

3.18 OPAMP Electrical Parameters

Table 29. OPAMP Characteristics 1.8–3.6 V

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
1	Operating Voltage	V_{DD}	1.8	—	3.6	V	C
2	Supply Current (I_{OUT}=0mA, CL=0 Low-Power mode)	I_{SUPPLY}	—	48	80	μA	T
3	Supply Current (I_{OUT}=0mA, CL=0 High-Speed mode)	I_{SUPPLY}	—	350	500	μA	T
4	Input Offset Voltage	V_{OS}	—	±2	±6	mV	T
5	Input Offset Voltage Temperature Coefficient	α_{VOS}	—	10	—	μV/C	T
6	Input Offset Current (–40°C to 105°C)	I_{OS}	—	±2.5	±250	nA	T
7	Input Offset Current (–40°C to 50°C)	I_{OS}	—	—	45	nA	T
8	Positive Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	0.8	3.5	nA	T
9	Positive Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	±2	nA	T
10	Negative Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	2.5	250	nA	T
11	Negative Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	45	nA	T
12	Input Common Mode Voltage Low	V_{CML}	0.1	—	—	V	T
13	Input Common Mode Voltage High	V_{CMH}	—	—	V_{DD}	V	T
14	Input Resistance	R_{IN}	—	500	—	MΩ	T
15	Input Capacitances	C_{IN}	—	—	10	pF	D
16	AC Input Impedance (f_{IN}=100kHz Negative Channel)	$\|X_{IN}\|$	—	52	—	kΩ	D
17	AC Input Impedance (f_{IN}=100kHz Positive Channel)	$\|X_{IN}\|$	—	132	—	kΩ	D
18	Input Common Mode Rejection Ratio	CMRR	55	65	—	dB	T
19	Power Supply Rejection Ratio	PSRR	60	65	—	dB	T
20	Slew Rate (ΔV_{IN}=100mV Low-Power mode)	SR	0.1	—	—	V/μs	T
21	Slew Rate (ΔV_{IN}=100mV High-Speed mode)	SR	1	—	—	V/μs	T
22	Unity Gain Bandwidth (Low-Power mode)	GBW	0.2	—	—	MHz	T
23	Unity Gain Bandwidth (High-Speed mode)	GBW	1	—	—	MHz	T
24	DC Open Loop Voltage Gain	A_V	80	90	—	dB	T
25	Load Capacitance Driving Capability	CL(max)	—	—	100	pF	T
26	Output Impedance AC Open Loop (@100 kHz Low-Power mode)	R_{OUT}	—	4k	—	Ω	D

Table 29. OPAMP Characteristics 1.8–3.6 V (continued)

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
27	Output Impedance AC Open Loop (@100 kHz High-Speed mode)	R_{OUT}	—	220	—	Ω	D
28	Output Voltage Range	V_{OUT}	0.15	—	V_{DD}–0.15	V	T
29	Output Drive Capability	I_{OUT}	±0.5	±1.0	—	mA	T
30	Gain Margin	GM	20	—	—	dB	D
31	Phase Margin	PM	45	55	—	deg	T
32	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	4	—	uS	T
33	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	1	—	uS	T
34	Input Voltage Noise Density	f=1 kHz	—	250	—	nV/√Hz	T

1 All parameters are measured at 3.3 V, CL =4 7 pF across temperature –40 to + 105°C unless specified.
2 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.