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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x16b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51mm128vmb

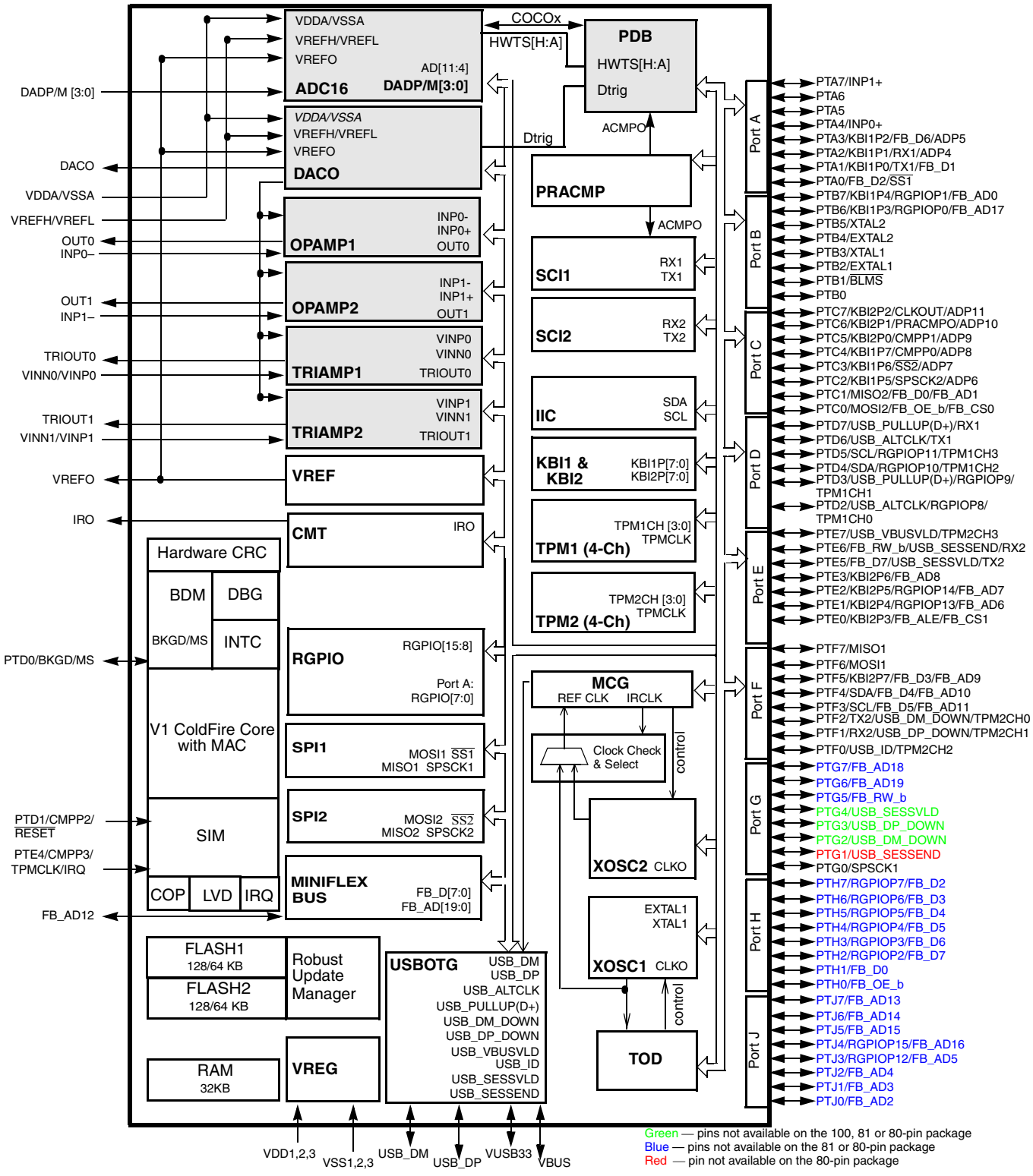


Figure 1. MCF51MM256 Series Block Diagram

2 Pinouts and Pin Assignments

2.1 104-Pin MAPBGA

The following figure shows the 104-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTF6	PTF7	USB_DP	USB_DM	VUSB33	PTF4	PTF3	FB_AD12	PTJ7	PTJ5	PTJ4	A
B	PTG0	PTA0	PTG3	VBUS	PTF5	PTJ6	PTH0	PTE5	PTF0	PTF1	PTF2	B
C	IRO	PTG4	PTA6	PTG2	PTG6	PTG5	PTG7	PTH1	PTE4	PTE6	PTE7	C
D	PTA5	PTA4	PTB1	VDD1		VDD2		VDD3	PTA1	PTE3	PTE2	D
E	VSSA	PTA7	PTB0						PTA2	PTJ3	PTE1	E
F	VREFL	INP1-	INP2-	PTG1				PTC7	PTJ2	PTJ0	PTJ1	F
G	TRIOUT1	OUT1	OUT2						PTD5	PTD7	PTE0	G
H	VINP1	VINN1	PTA3	VSS1		VSS2		VSS3	PTD4	PTD3	PTD2	H
J	DADP0	DADM0	PTH7	PTH6	PTH4	PTH3	PTH2	PTD6	PTC2	PTC0	PTC1	J
K	VINP2	VINN2	DADP1	PTH5	PTB6	PTB7	PTC3	PTD1	PTC4	PTC5	PTC6	K
L	TRIOUT2	DACO	DADM1	VREFO	VREFH	VDDA	PTB3	PTB2	PTD0	PTB5	PTB4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. 104-Pin MAPBGA

2.5 Pin Assignments

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
B2	1	B2	1	PTA0	FB_D2	$\overline{SS1}$	—	PTA0/FB_D2/$\overline{SS1}$
C1	2	A1	2	IRO	—	—	—	IRO
C6	3	—	—	PTG5	FB_$\overline{RW}$	—	—	PTG5/FB_$\overline{RW}$
C5	4	—	—	PTG6	FB_AD19	—	—	PTG6/FB_AD19
C7	5	—	—	PTG7	FB_AD18	—	—	PTG7/FB_AD18
B7	6	—	—	PTH0	$\overline{FB\_OE}$	—	—	PTH0/$\overline{FB\_OE}$
C8	7	—	—	PTH1	FB_D0	—	—	PTH1/FB_D0
D9	8	C4	3	PTA1	KBI1P0	TX1	FB_D1	PTA1/KBI1P0/TX1/FB_D1
E9	9	D5	4	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
H3	10	D6	5	PTA3	KBI1P2	FB_D6	ADP5	PTA3/KBI1P2/FB_D6/ADP5
D2	11	C1	6	PTA4	INP1+	—	—	PTA4/INP1+
D1	12	C2	7	PTA5	—	—	—	PTA5
C3	13	C3	8	PTA6	—	—	—	PTA6
E2	14	D2	9	PTA7	INP2+	—	—	PTA7/INP2+
E3	15	D3	10	PTB0	—	—	—	PTB0
D3	16	D4	11	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
E1	17	J1	12	VSSA	—	—	—	VSSA
F1	18	J2	13	VREFL	—	—	—	VREFL
F2	19	D1	14	INP1-	—	—	—	INP1-
G2	20	E1	15	OUT1	—	—	—	OUT1
G1	21	F2	16	DADP2	TRIOUT1	—	—	DADP2/TRIOUT1
H1	22	F1	17	VINP1	—	—	—	VINP1
H2	23	E2	18	DADM2	VINN1	—	—	DADM2/VINN1
F3	24	F3	19	INP2-	—	—	—	INP2-
G3	25	E3	20	OUT2	—	—	—	OUT2
L2	26	G2	21	DACO	—	—	—	DACO
L1	27	G3	22	DADP3	TRIOUT2	—	—	DADP3/TRIOUT2
K1	28	H4	23	VINP2	—	—	—	VINP2
K2	29	G4	24	DADM3	VINN2	—	—	DADM3/VINN2

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Min	Max	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T

Table 9. DC Characteristics (continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
20	V_{LVWH}	Low-voltage warning threshold — high range[9] V_{DD} falling						
			—	2.36	2.46	2.56	V	P
		V_{DD} rising						
			—	2.36	2.46	2.56	V	P
21	V_{LVWL}	Low-voltage warning threshold — low range[9] V_{DD} falling						
			—	2.11	2.16	2.22	V	P
		V_{DD} rising						
			—	2.16	2.21	2.27	V	P
22	V_{hys}	Low-voltage inhibit reset/recoverhysteresis[10]	—	—	50	—	mV	C
23	V_{BG}	Bandgap Voltage Reference[11]	—	1.110	1.17	1.230	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to V_{DD} or V_{SS} and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 Maximum is highest voltage that POR is guaranteed.

9 Run at 1 MHz bus frequency

10 Low voltage detection and warning limits measured at 1 MHz bus frequency.

11 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

Table 10. Supply Current Characteristics (continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	16.5	—	mA	–40 to 105	C
			20 MHz	3	10.3	—	mA	–40 to 105	T
			8 MHz	3	6.6	—	mA	–40 to 105	T
			1 MHz	3	1.7	—	mA	–40 to 105	T
6	$LPWI_{DD}$	Low-Power Wait mode supply current							
			16 KHz	3	28	62	µA	–40 to 105	T
7	$S2I_{DD}$	Stop2 mode supply current[4]							
			N/A	3	0.410	1.00	µA	–40 to 25	P
			N/A	3	3.7	10	µA	70	C
			N/A	3	10	20	µA	85	C
			N/A	3	21	31.5	µA	105	P
			N/A	2	0.410	0.640	µA	–40 to 25	C
			N/A	2	3.4	9	µA	70	C
			N/A	2	9.5	18	µA	85	C
			N/A	2	20	30	µA	105	C

Table 15. 16-Bit ADC Operating Conditions (continued)

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
5	V_{REFL}	Ref Voltage Low		V_{SSA}	V_{SSA}	V_{SSA}	V	D	
6	V_{ADIN}	Input Voltage		V_{REFL}	—	V_{REFH}	V	D	
7	C_{ADIN}	Input Capacitance	16-bit modes 8/10/12-bit modes	—	8 4	10 5	pF	T	
8	R_{ADIN}	Input Resistance		—	2	5	kΩ	T	
9	R_{AS}	Analog Source Resistance							External to MCU Assumes ADLSMP=0
		16-bit mode	f_{ADCK} > 8 MHz	—	—	0.5	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	1	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	2	kΩ	T	
		13/12-bit mode	f_{ADCK} > 8 MHz	—	—	1	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	2	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	5	kΩ	T	
		11/10-bit mode	f_{ADCK} > 8 MHz	—	—	2	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	10	kΩ	T	
		9/8-bit mode	f_{ADCK} > 8 MHz	—	—	5	kΩ	T	
			f_{ADCK} < 8 MHz	—	—	10	kΩ	T	
10	f_{ADCK}	ADC Conversion Clock Frequency							
		ADLPC=0, ADHSC=1		1.0	—	8.0	MHz	D	
		ADLPC=0, ADHSC=0		1.0	—	5.0	MHz	D	
		ADLPC=1, ADHSC=0		1.0	—	2.5	MHz	D	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq$ 8 MHz, –40 to 85 °C)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	215	—	μA	T	ADLSMP =0 ADCO=1
		ADLPC=0, ADHSC=0		—	470	—			
		ADLPC=0, ADHSC=1		—	610	—			
2	Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	—	μA	T	
3	ADC Asynchronous Clock Source	ADLPC=1, ADHSC=0	f_{ADACK}	—	2.4	—	MHz	C	$t_{ADACK} = 1/f_{ADACK}$
		ADLPC=0, ADHSC=0		—	5.2	—			
		ADLPC=0, ADHSC=1		—	6.2	—			
4	Sample Time	See Reference Manual for sample times							
5	Conversion Time	See Reference Manual for conversion times							
6	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+48/ –40 +56/ –28	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±3.0 ±3.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.5 ±1.5		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
7	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	+5/–3 +5/–3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

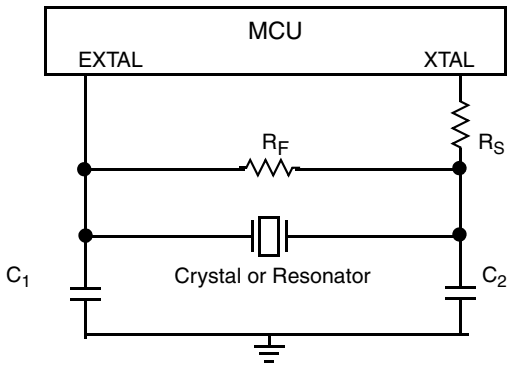
Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, $f_{ADACK} \leq 4$ MHz, ADHSC = 1)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+24/ –24 +32/–20	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.0 ±1.25		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
2	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
3	Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	
4	Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-8	LSB[2]	T	$V_{ADIN} = V_{SSA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

Table 19. XOSC (Temperature Range = –40 to 105°C Ambient) (continued)

#	Characteristic	Symbol	Min	Typ[1]	Max	Unit	C
6	Crystal start-up time [4] • Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	ms	D
	• Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—		D
	• High range, low gain (RANGE = 1, HGO = 0)[5]	$t_{CSTH-LP}$	—	5	—		D
	• High range, high gain (RANGE = 1, HGO = 1)[5]	$t_{CSTH-HGO}$	—	15	—		D

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.
2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.
4 This parameter is characterized and not tested on each device. Proper PC board layout porcedures must be followed to achieve specifications.
5 4 MHz crystal.



3.11 Mini-FlexBus Timing Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 25.1666 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

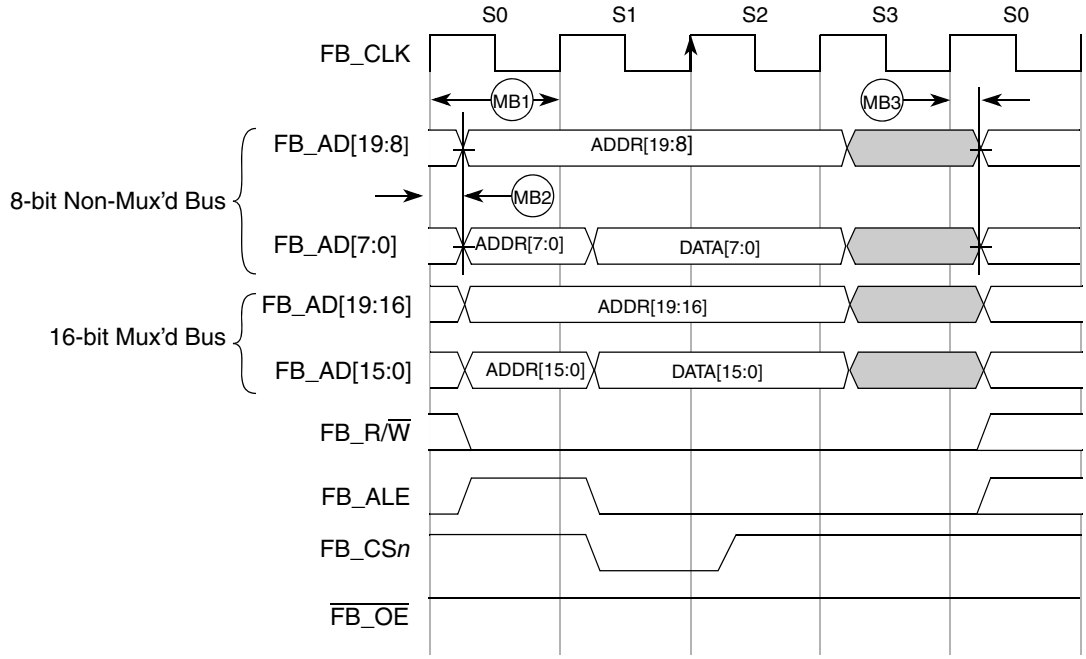


Figure 10. Mini-FlexBus Write Timing

Table 21. Control Timing (continued)

#	Symbol	Parameter	Min	Typical[1]	Max	C	Unit
9	t_{Rise}, t_{Fall}	Port rise and fall time (load = 50 pF)[4], Low Drive					ns
		Slew rate control disabled (PTxSE = 0)	—	11	—	D	
		Slew rate control enabled (PTxSE = 1)	—	35	—	D	
		Slew rate control disabled (PTxSE = 0)	—	40	—	D	
		Slew rate control enabled (PTxSE = 1)	—	75	—	D	

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

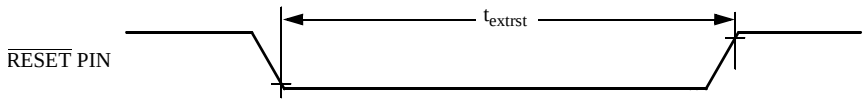


Figure 11. Reset Timing

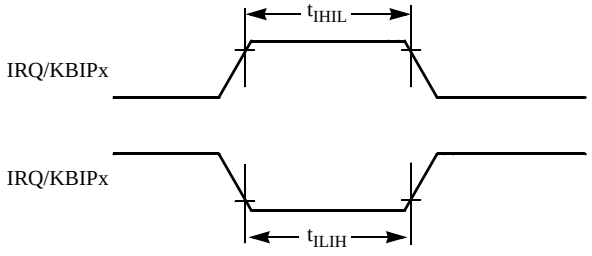


Figure 12. IRQ/KBIPx Timing

3.12.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 22. TPM Input Timing

#	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

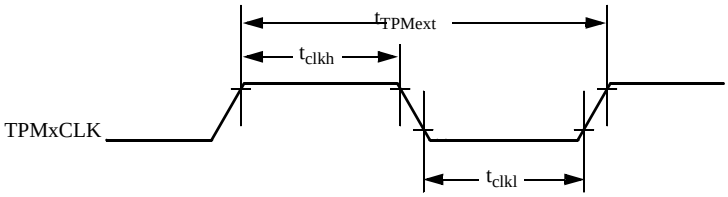


Figure 13. Timer External Clock

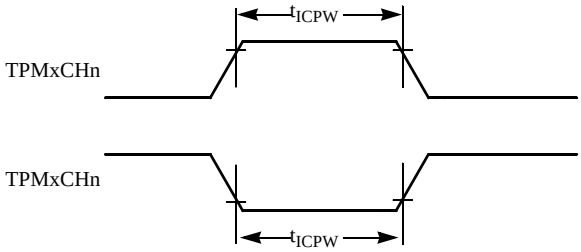
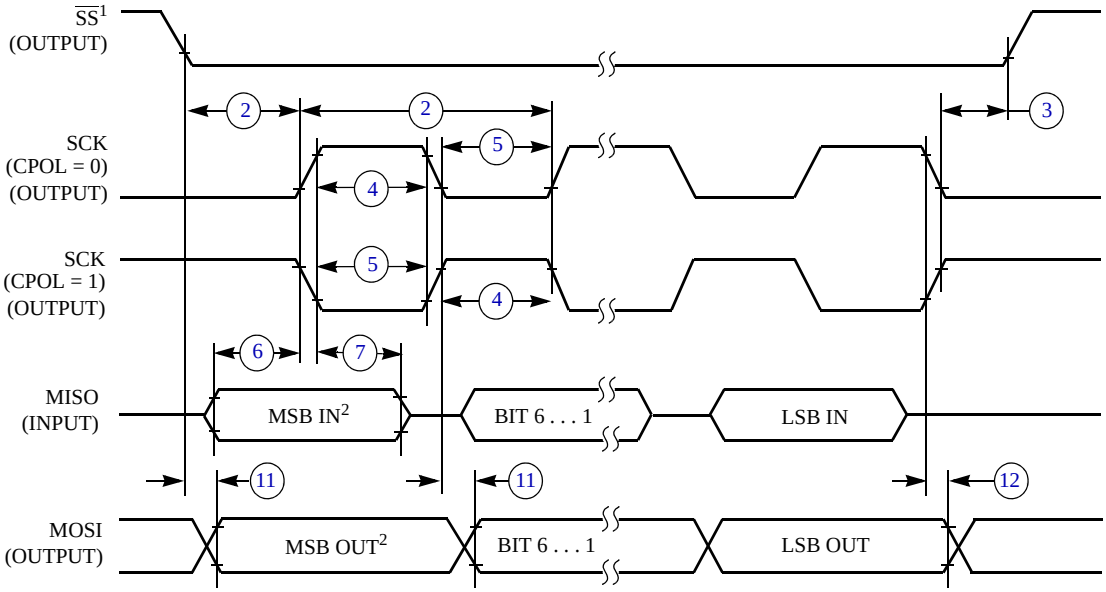
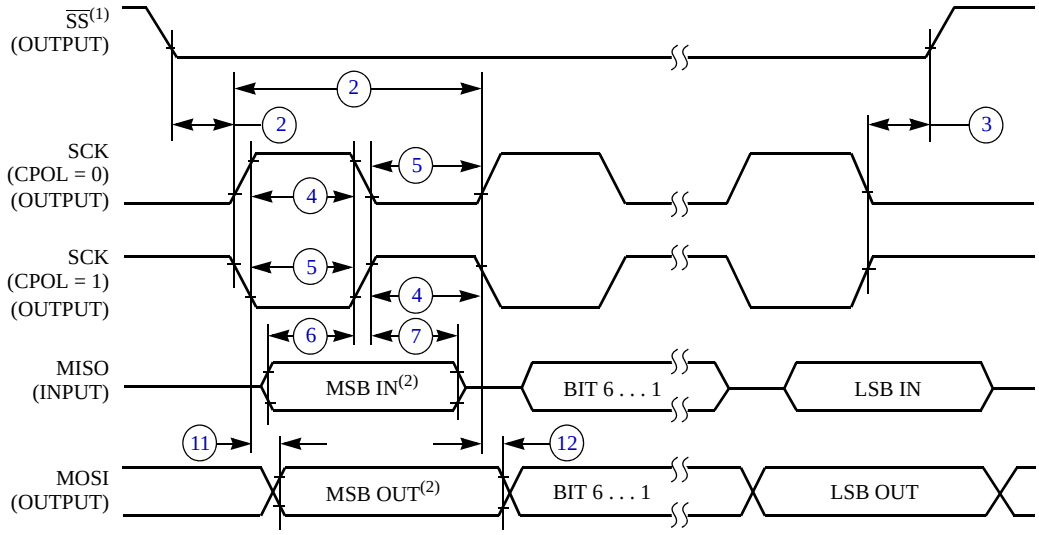


Figure 14. Timer Input Capture Pulse



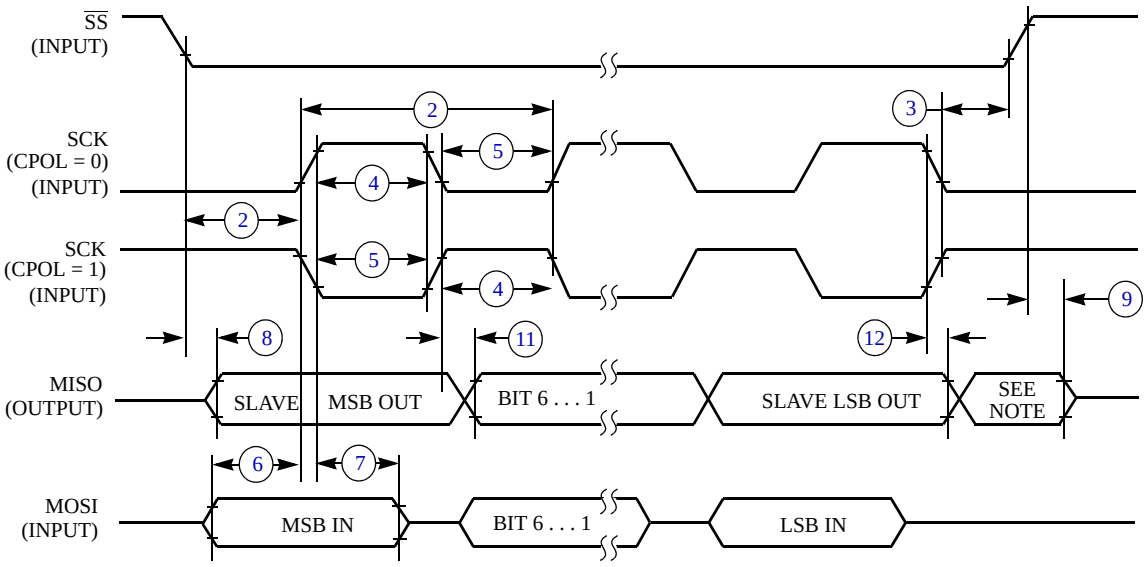
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

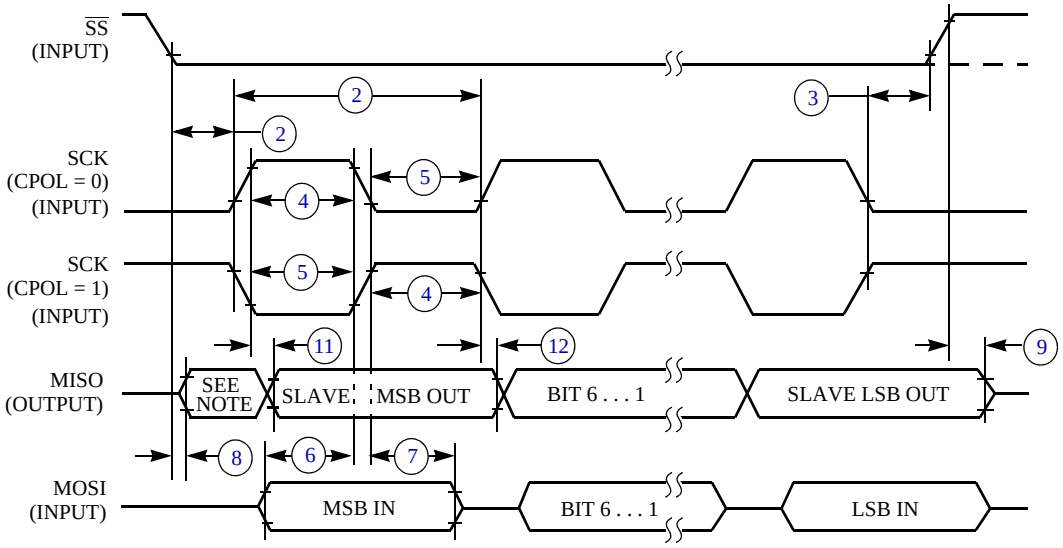
Figure 16. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined, but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

3.16 VREF Electrical Specifications

Table 26. VREF Electrical Specifications

#	Characteristic	Symbol	Min	Max	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Operating temperature range	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nF	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V at 25 °C	V_{out}	1.145	1.153	V	P
6	Temperature Drift (V_{min}—V_{max} across the full temperature range)	Tdrift	—	25	mV[1]	T
7	Aging Coefficient[2]	A_C	—	60	µV/year	C
8	Powered down Current (Off Mode, VREFEN=0, VRSTEN=0)	I	—	0.10	µA	C
9	Bandgap only (Mode_LV[1:0] = 00)	I	—	75	µA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	µA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation MODE_LV = 10	—	—	100	µV/mA	C
13	Line Regulation MODE = 1:0, Tight Regulation V_{DD} < 2.3 V, Delta V_{DDA} =100 mV, VREFH = 1.2 V driven externally with VREFO disabled. (Power Supply Rejection)	DC	70	—	dB	C

1 See typical chart that follows (Figure 20).

2 Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging µV/year. VREF0 data recorded per month.

Table 27. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C
1	Voltage Reference Output with Factory Trim (Temperature range from 0°C to 50 °C)	V_{out}	1.149	1.152	mV	T
2	Temperature Drive (V_{min} —V_{max} Temperature range from 0 °C to 50 °C)	T_{drift}	—	3	mV[1]	T

1 See typical chart that follows (Figure 20).

Table 28. TRIAMP Characteristics 1.8–3.6 V, –40°C~105°C (continued)

#	Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit	C
28	Input Voltage Noise Density	f= 1 kHz	—	160	—	nV/√Hz	T

1 All parameters are measured at 3.0 V, CL= 47 pF across temperature –40 to + 105 °C unless specified.
2 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

3.18 OPAMP Electrical Parameters

Table 29. OPAMP Characteristics 1.8–3.6 V

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
1	Operating Voltage	V_{DD}	1.8	—	3.6	V	C
2	Supply Current (I_{OUT}=0mA, CL=0 Low-Power mode)	I_{SUPPLY}	—	48	80	μA	T
3	Supply Current (I_{OUT}=0mA, CL=0 High-Speed mode)	I_{SUPPLY}	—	350	500	μA	T
4	Input Offset Voltage	V_{OS}	—	±2	±6	mV	T
5	Input Offset Voltage Temperature Coefficient	α_{VOS}	—	10	—	μV/C	T
6	Input Offset Current (–40°C to 105°C)	I_{OS}	—	±2.5	±250	nA	T
7	Input Offset Current (–40°C to 50°C)	I_{OS}	—	—	45	nA	T
8	Positive Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	0.8	3.5	nA	T
9	Positive Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	±2	nA	T
10	Negative Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	2.5	250	nA	T
11	Negative Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	45	nA	T
12	Input Common Mode Voltage Low	V_{CML}	0.1	—	—	V	T
13	Input Common Mode Voltage High	V_{CMH}	—	—	V_{DD}	V	T
14	Input Resistance	R_{IN}	—	500	—	MΩ	T
15	Input Capacitances	C_{IN}	—	—	10	pF	D
16	AC Input Impedance (f_{IN}=100kHz Negative Channel)	$\|X_{IN}\|$	—	52	—	kΩ	D
17	AC Input Impedance (f_{IN}=100kHz Positive Channel)	$\|X_{IN}\|$	—	132	—	kΩ	D
18	Input Common Mode Rejection Ratio	CMRR	55	65	—	dB	T
19	Power Supply Rejection Ratio	PSRR	60	65	—	dB	T
20	Slew Rate (ΔV_{IN}=100mV Low-Power mode)	SR	0.1	—	—	V/μs	T
21	Slew Rate (ΔV_{IN}=100mV High-Speed mode)	SR	1	—	—	V/μs	T
22	Unity Gain Bandwidth (Low-Power mode)	GBW	0.2	—	—	MHz	T
23	Unity Gain Bandwidth (High-Speed mode)	GBW	1	—	—	MHz	T
24	DC Open Loop Voltage Gain	A_V	80	90	—	dB	T
25	Load Capacitance Driving Capability	CL(max)	—	—	100	pF	T
26	Output Impedance AC Open Loop (@100 kHz Low-Power mode)	R_{OUT}	—	4k	—	Ω	D

Table 29. OPAMP Characteristics 1.8–3.6 V (continued)

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
27	Output Impedance AC Open Loop (@100 kHz High-Speed mode)	R_{OUT}	—	220	—	Ω	D
28	Output Voltage Range	V_{OUT}	0.15	—	V_{DD}–0.15	V	T
29	Output Drive Capability	I_{OUT}	±0.5	±1.0	—	mA	T
30	Gain Margin	GM	20	—	—	dB	D
31	Phase Margin	PM	45	55	—	deg	T
32	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	4	—	uS	T
33	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	1	—	uS	T
34	Input Voltage Noise Density	f=1 kHz	—	250	—	nV/√Hz	T

1 All parameters are measured at 3.3 V, CL =4 7 pF across temperature –40 to + 105°C unless specified.
2 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

5 Revision History

This section lists major changes between versions of the MCF51MM256 Data Sheet.

Table 32. Revision History

Revision	Date	Description
0	March/April 2009	Initial Draft
1	July 2009	• Revised to follow standard template. • Removed extraneous headings from the TOC. • Corrected units for Monotonocity to be blank in for the DAC specification. • Updated ADC characteristic tables to include 16-Bit SAR in headings.
2	July 2009	• Changed MCG (XOSC) Electricals Table - Row 2, Average Internal Reference Frequency typical value from 32.768 to 31.25.
3	April 2010	• Updated Thermal Characteristics table. Reinserted the 81 and 104 MapBGA devices. • Revised the ESD and Latch-Up Protection Characteristic description to read: Latch-up Current at T_A = 125°C. • Changed Table 9. DC Characteristics rows 2 and 4, to 1.8 V, ILoad = -600 mA conditions to 1.8 V, ILoad = 600μA respectively. • Corrected the 16-bit SAR ADC Operating Condition table Ref Voltage High Min value to be 1.13 instead of 1.15. • Updated the ADC electricals. • Inserted the Mini-FlexBus Timing Specifications. • Added a Temp Drift parameter to the VREF Electrical Specifications. • Removed the S08 Naming Convention diagram. • Updated the Orderable Part Number Summary to include the Freescale Part Number suffixes. • Completed the Package Description table values. • Changed the 80LQFP package drawing from 98ARL10530D to 98ASS23174W. • Updated electrical characteristic data.
4	October 2010	• Updated with the latest characteristic data. Added several figures. Added the ADC Typical Operation table.
5	July 2012	In “Supply current characteristics” table, • For S3I_{DD}, the maximum value for the first row at 1μA is changed to 1.3 μA and the typical value 0.65 μA is changed to 0.75μA. • For parameter 3, changed “LPS” to “LPR”, “FBILP” to "FBI" and “FBELP” to “FBE”. • For parameter 4, changed “LPS” to “LPR”, and “FBELP” to “BLPE” in both instances.

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