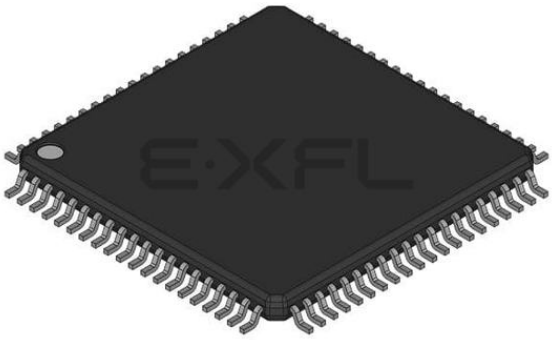


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Coldfire V1 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | CANbus, EBI/EMI, I²C, SCI, SPI, USB OTG |
| Peripherals | LVD, PWM, WDT |
| Number of I/O | 47 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 8x16b; D/A 1x12b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51mm256clk |

# 1 Features

The following table provides a cross-comparison of the features of the MCF51MM256/128 according to package.

**Table 1. MCF51MM256/128 Features by MCU and Package**

| Feature | MCF51MM256 | | | | MCF51MM128 | |
|---|---|---|---|---|---|---|
| FLASH Size (bytes) | 262144 | | | | 131072 | |
| RAM Size (bytes) | 32K | | | | 32K | |
| Pin Quantity | 104 | 100 | 81 | 80 | 81 | 80 |
| Programmable Analog Comparator (PRACMP) | yes | yes | yes | yes | yes | yes |
| Debug Module (DBG) | yes | yes | yes | yes | yes | yes |
| Multipurpose Clock Generator (MCG) | yes | yes | yes | yes | yes | yes |
| Inter-Integrated Communication (IIC) | yes | yes | yes | yes | yes | yes |
| Interrupt Request Pin (IRQ) | yes | yes | yes | yes | yes | yes |
| Keyboard Interrupt (KBI) | 16 | 16 | 16 | 16 | 16 | 16 |
| Digital General Purpose I/O[1] | 69 | 65 | 48 | 47 | 48 | 47 |
| Dedicated Analog Input Pins | 14 | 14 | 14 | 14 | 14 | 14 |
| Power and Ground Pins | 8 | 8 | 8 | 8 | 8 | 8 |
| Time Of Day (TOD) | yes | yes | yes | yes | yes | yes |
| Serial Communications (SCI1) | yes | yes | yes | yes | yes | yes |
| Serial Communications (SCI2) | yes | yes | yes | yes | yes | yes |
| Serial Peripheral Interface (SPI1(FIFO)) | yes | yes | yes | yes | yes | yes |
| Serial Peripheral Interface(SPI2) | yes | yes | yes | yes | yes | yes |
| Carrier Modulator Timer Pin (IRO) | yes | yes | yes | yes | yes | yes |
| TPM Input Clock Pin (TPMCLK) | yes | yes | yes | yes | yes | yes |
| TPM1 Channels | 4 | 4 | 4 | 4 | 4 | 4 |
| TPM2 Channels | 4 | 4 | 4 | 4 | 4 | 4 |
| XOSC1 | yes | yes | yes | yes | yes | yes |
| XOSC2 | yes | yes | yes | yes | yes | yes |
| USB On-the-Go | yes | yes | yes | yes | yes | yes |
| Mini-FlexBus | yes | yes | DATA[2] | DATA[2] | DATA[2] | DATA[2] |
| Rapid GPIO | 16 | 16 | 9 | 9 | 9 | 9 |
| **MEASUREMENT ENGINE** | | | | | | |
| Programmable Delay Block (PDB) | yes | yes | yes | yes | yes | yes |
| 16-Bit SAR ADC Differential Channels[3] | 4 | 4 | 4 | 4 | 4 | 4 |
| 16-Bit SAR ADC Single-Ended Channels | 8 | 8 | 8 | 8 | 8 | 8 |
| DAC Ouput Pin (DACO) | yes | yes | yes | yes | yes | yes |
| Voltage Reference Output Pin (VREFO) | yes | yes | yes | yes | yes | yes |
| General Purpose Operational Amplifier (OPAMP) | yes | yes | yes | yes | yes | yes |
| Trans-Impedance Amplifier (TRIAMP) | yes | yes | yes | yes | yes | yes |

1 Port I/O count does not include $\overline{\text{BLMS}}$, BKGD and IRQ. $\overline{\text{BLMS}}$ and BKGD are Output only, IRQ is input only.

2 The 80/81 pin packages contain the Mini-FlexBus data pins to support an 8-bit data bus interface to external peripherals.

3 Each differential channel is comprised of 2 pin inputs.

**Table 2. MCF51MM256/128 Functional Units (continued)**

| Unit | Function |
|---|---|
| SCI1, SCI2 (Serial Communications Interfaces) | Serial communications UARTs capable of supporting RS-232 and LIN protocols. |
| SIM (system integration unit) | |
| SPI1 (FIFO), SPI2 (Serial Peripheral Interfaces) | SPI1 and SPI2 provide standard master/slave capability. SPI contains a FIFO buffer in order to increase the throughput for this peripheral. |
| TPM1, TPM2 (Timer/PWM Module) | Timer/PWM module can be used for a variety of generic timer operations as well as pulse-width modulation. |
| VREG (Voltage Regulator) | Controls power management across the device. |
| XOSC1 and XOSC2 (Crystal Oscillators) | These devices incorporate redundant crystal oscillators. One is intended primarily for use by the TOD, and the other by the CPU and other peripherals. |

## 2.2 100-Pin LQFP

The following figure shows the 100-pin LQFP pinout configuration.

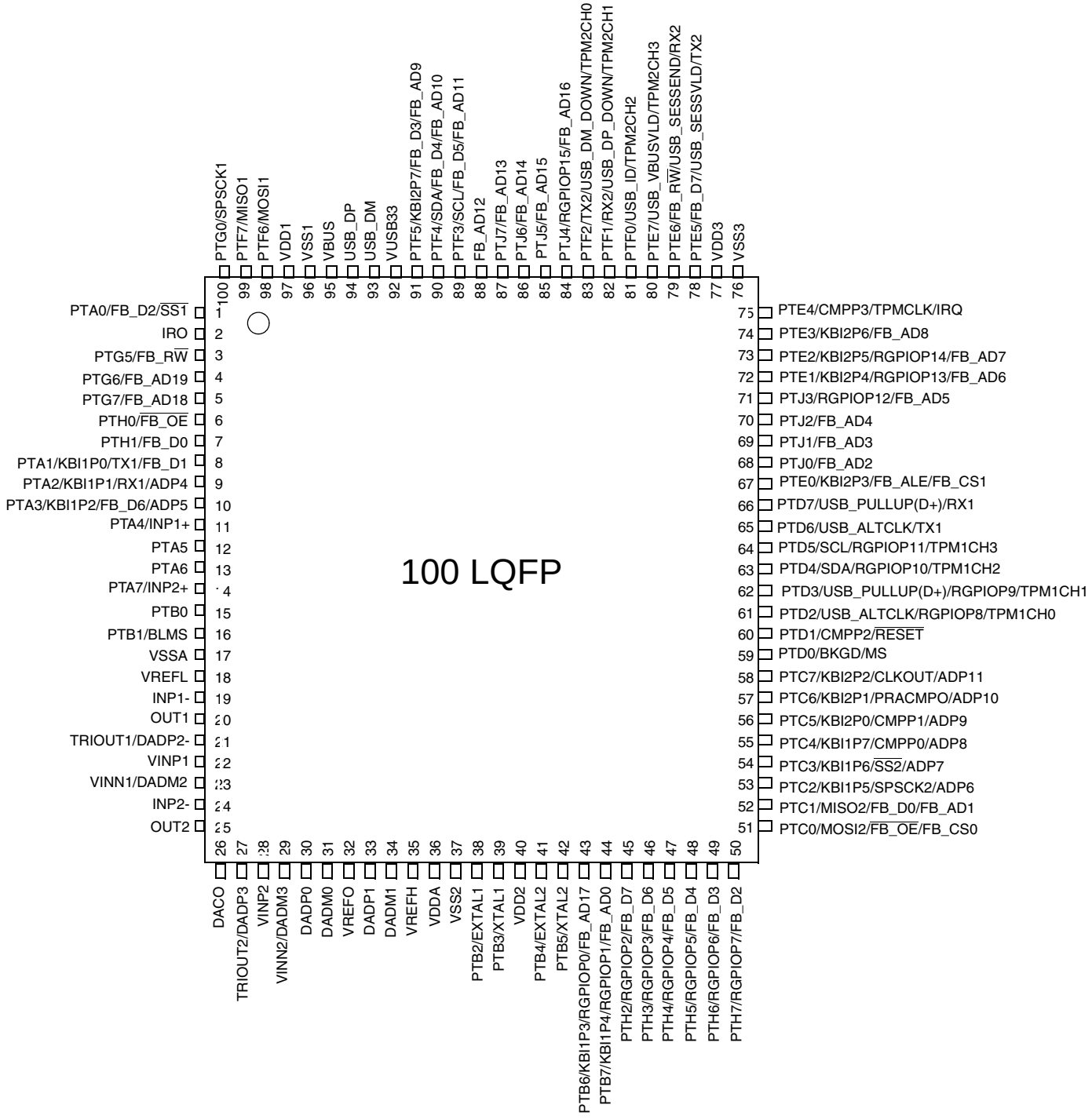



**Figure 3. 100-Pin LQFP**

**Table 3. Package Pin Assignments (continued)**

| Package | | | | Default Function | Alternate 1 | Alternate 2 | Alternate 3 | Composite Pin Name |
|---|---|---|---|---|---|---|---|---|
| 104 MAPBGA | 100 LQFP | 81 MAPBGA | 80 LQFP | | | | | |
| J1 | 30 | G1 | 25 | DADP0 | — | — | — | DADP0 |
| J2 | 31 | H1 | 26 | DADM0 | — | — | — | DADM0 |
| L4 | 32 | G5 | 27 | VREFO | — | — | — | VREFO |
| K3 | 33 | H3 | 28 | DADP1 | — | — | — | DADP1 |
| L3 | 34 | H2 | 29 | DADM1 | — | — | — | DADM1 |
| L5 | 35 | J3 | 30 | VREFH | — | — | — | VREFH |
| L6 | 36 | J4 | 31 | VDDA | — | — | — | VDDA |
| H6 | 37 | F4 | 32 | VSS2 | — | — | — | VSS2 |
| L8 | 38 | J5 | 33 | PTB2 | EXTAL1 | — | — | PTB2/EXTAL1 |
| L7 | 39 | J6 | 34 | PTB3 | XTAL1 | — | — | PTB3/XTAL1 |
| D6 | 40 | E4 | 35 | VDD2 | — | — | — | VDD2 |
| L11 | 41 | J8 | 36 | PTB4 | EXTAL2 | — | — | PTB4/EXTAL2 |
| L10 | 42 | J9 | 37 | PTB5 | XTAL2 | — | — | PTB5/XTAL2 |
| K5 | 43 | G6 | 38 | PTB6 | KBI1P3 | RGPIOP0 | FB_AD17 | PTB6/KBI1P3/RGPIOP0/FB_AD17 |
| K6 | 44 | F7 | 39 | PTB7 | KBI1P4 | RGPIOP1 | FB_AD0 | PTB7/KBI1P4/RGPIOP1/FB_AD0 |
| J7 | 45 | — | — | PTH2 | RGPIOP2 | FB_D7 | — | PTH2/RGPIOP2/FB_D7 |
| J6 | 46 | — | — | PTH3 | RGPIOP3 | FB_D6 | — | PTH3/RGPIOP3/FB_D6 |
| J5 | 47 | — | — | PTH4 | RGPIOP4 | FB_D5 | — | PTH4/RGPIOP4/FB_D5 |
| K4 | 48 | — | — | PTH5 | RGPIOP5 | FB_D4 | — | PTH5/RGPIOP5/FB_D4 |
| J4 | 49 | — | — | PTH6 | RGPIOP6 | FB_D3 | — | PTH6/RGPIOP6/FB_D3 |
| J3 | 50 | — | — | PTH7 | RGPIOP7 | FB_D2 | — | PTH7/RGPIOP7/FB_D2 |
| J10 | 51 | G7 | 40 | PTC0 | MOSI2 | $\overline{\text{FB\_OE}}$ | FB_CS0 | PTC0/MOSI2/$\overline{\text{FB\_OE}}$/FB_CS0 |
| J11 | 52 | G8 | 41 | PTC1 | MISO2 | FB_D0 | FB_AD1 | PTC1/MISO2/FB_D0/FB_AD1 |
| J9 | 53 | G9 | 42 | PTC2 | KBI1P5 | SPSCK2 | ADP6 | PTC2/KBI1P5/SPSCK2/ADP6 |
| K7 | 54 | H5 | 43 | PTC3 | KBI1P6 | $\overline{\text{SS2}}$ | ADP7 | PTC3/KBI1P6/$\overline{\text{SS2}}$/ADP7 |
| K9 | 55 | H6 | 44 | PTC4 | KBI1P7 | CMPP0 | ADP8 | PTC4/KBI1P7/CMPP0/ADP8 |
| K10 | 56 | H8 | 45 | PTC5 | KBI2P0 | CMPP1 | ADP9 | PTC5/KBI2P0/CMPP1/ADP9 |
| K11 | 57 | H9 | 46 | PTC6 | KBI2P1 | PRACMPO | ADP10 | PTC6/KBI2P1/PRACMPO/ADP10 |
| F8 | 58 | F8 | 47 | PTC7 | KBI2P2 | CLKOUT | ADP11 | PTC7/KBI2P2/CLKOUT/ADP11 |
| L9 | 59 | H7 | 48 | PTD0 | BKGD | MS | — | PTD0/BKGD/MS |
| K8 | 60 | J7 | 49 | PTD1 | CMPP2 | $\overline{\text{RESET}}$ | — | PTD1/CMPP2/$\overline{\text{RESET}}$ |

**Table 3. Package Pin Assignments (continued)**

| Package | | | | Default Function | Alternate 1 | Alternate 2 | Alternate 3 | Composite Pin Name |
|---|---|---|---|---|---|---|---|---|
| 104 MAPBGA | 100 LQFP | 81 MAPBGA | 80 LQFP | | | | | |
| A8 | 88 | — | — | FB_AD12 | — | — | — | FB_AD12 |
| A7 | 89 | A8 | 69 | PTF3 | SCL | FB_D5 | FB_AD11 | PTF3/SCL/FB_D5/FB_AD11 |
| A6 | 90 | A7 | 70 | PTF4 | SDA | FB_D4 | FB_AD10 | PTF4/SDA/FB_D4/FB_AD10 |
| B5 | 91 | B5 | 71 | PTF5 | KBI2P7 | FB_D3 | FB_AD9 | PTF5/KBI2P7/FB_D3/FB_AD9 |
| A5 | 92 | A6 | 72 | VUSB33 | — | — | — | VUSB33 |
| A4 | 93 | B4 | 73 | USB_DM | — | — | — | USB_DM |
| A3 | 94 | A4 | 74 | USB_DP | — | — | — | USB_DP |
| B4 | 95 | A5 | 75 | VBUS | — | — | — | VBUS |
| H4 | 96 | F6 | 76 | VSS1 | — | — | — | VSS1 |
| D4 | 97 | E6 | 77 | VDD1 | — | — | — | VDD1 |
| A1 | 98 | A3 | 78 | PTF6 | MOSI1 | — | — | PTF6/MOSI1 |
| A2 | 99 | B1 | 79 | PTF7 | MISO1 | — | — | PTF7/MISO1 |
| B1 | 100 | A2 | 80 | PTG0 | SPSCK1 | — | — | PTG0/SPSCK1 |
| F4 | — | A1 | — | PTG1 | USB_ SESSEND | — | — | PTG1/USB_SESSEND |
| C4 | — | — | — | PTG2 | USB_DM_ DOWN | — | — | PTG2/USB_DM_DOWN |
| B3 | — | — | — | PTG3 | USB_DP_ DOWN | — | — | PTG3/USB_DP_DOWN |
| C2 | — | — | — | PTG4 | USB_SESSVLD | — | — | PTG4/USB_SESSVLD |

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving Equation 1 and Equation 2 iteratively for any value of $T_A$.

## 3.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 7. ESD and Latch-up Test Conditions**

| Model | Description | Symbol | Value | Unit |
|---|---|---|---|---|
| Human Body | Series Resistance | R1 | 1500 | Ω |
| | Storage Capacitance | C | 100 | pF |
| | Number of Pulse per pin | — | 3 | — |
| Machine | Series Resistance | R1 | 0 | Ω |
| | Storage Capacitance | C | 200 | pF |
| | Number of Pulse per pin | — | 3 | — |
| Latch-up | Minimum input voltage limit | — | –2.5 | V |
| | Maximum input voltage limit | — | 7.5 | V |

**Table 8. ESD and Latch-Up Protection Characteristics**

| # | Rating | Symbol | Min | Max | Unit | C |
|---|---|---|---|---|---|---|
| 1 | Human Body Model (HBM) | $V_{HBM}$ | ±2000 | — | V | T |
| 2 | Machine Model (MM) | $V_{MM}$ | ±200 | — | V | T |

**Table 9. DC Characteristics (continued)**

| Num | Symbol | Characteristic | Condition | Min | Typ[1] | Max | Unit | C |
|---|---|---|---|---|---|---|---|---|
| 7 | $V_{IL}$ | Input low voltage — all digital inputs | | | | | | |
| | | | $V_{DD}$ > 2.7 V | — | — | 0.35 x $V_{DD}$ | V | P |
| | | | $V_{DD}$ >1.8 V | — | — | 0.30 x $V_{DD}$ | V | C |
| 8 | $V_{hys}$ | Input hysteresis — all digital inputs | — | 0.06 x $V_{DD}$ | — | — | mV | C |
| 9 | $\|I_{In}\|$ | Input leakage current — all input only pins (Per pin) | $V_{In}$ = $V_{DD}$ or $V_{SS}$ | — | — | 0.5 | μA | P |
| 10 | $\|I_{OZ}\|$ | Hi-Z (off-state) leakage current[3] — all digital input/output (per pin) | $V_{In}$ = $V_{DD}$ or $V_{SS}$ | — | 0.003 | 0.5 | μA | P |
| 11 | $R_{PU}$ | Pull-up resistors — all digital inputs, when enabled | — | 17.5 | — | 52.5 | kΩ | P |
| 12 | $R_{PD}$ | Internal pull-down resistors[4] | — | 17.5 | — | 52.5 | kΩ | P |
| 13 | $I_{IC}$ | DC injection current [5, 6, 7] — Single pin limit | | | | | | |
| | | | $V_{SS}$ > $V_{IN}$ > $V_{DD}$ | –0.2 | — | 0.2 | mA | D |
| | | Total MCU limit, includes sum of all stressed pins | | | | | | |
| | | | $V_{SS}$ > $V_{IN}$ > $V_{DD}$ | –5 | — | 5 | mA | D |
| 14 | $C_{In}$ | Input Capacitance, all pins | — | — | — | 8 | pF | C |
| 15 | $V_{RAM}$ | RAM retention voltage | — | — | 0.6 | 1.0 | V | C |
| 16 | $V_{POR}$ | POR re-arm voltage[8] | — | 0.9 | 1.4 | 1.79 | V | C |
| 17 | $t_{POR}$ | POR re-arm time | — | 10 | — | — | μs | D |
| 18 | $V_{LVDH}$[9] | Low-voltage detection threshold — high range — $V_{DD}$ falling | | | | | | |
| | | | — | 2.11 | 2.16 | 2.22 | V | P |
| | | $V_{DD}$ rising | | | | | | |
| | | | — | 2.16 | 2.21 | 2.27 | V | P |
| 19 | $V_{LVDL}$ | Low-voltage detection threshold — low range[9] — $V_{DD}$ falling | | | | | | |
| | | | — | 1.80 | 1.82 | 1.91 | V | P |
| | | $V_{DD}$ rising | | | | | | |
| | | | — | 1.86 | 1.90 | 1.99 | V | P |

**Table 9. DC Characteristics (continued)**

| Num | Symbol | Characteristic | Condition | Min | Typ[1] | Max | Unit | C |
|---|---|---|---|---|---|---|---|---|
| 20 | $V_{LVWH}$ | Low-voltage warning threshold — high range[9] $V_{DD}$ falling | | | | | | |
| | | | — | 2.36 | 2.46 | 2.56 | V | P |
| | | $V_{DD}$ rising | | | | | | |
| | | | — | 2.36 | 2.46 | 2.56 | V | P |
| 21 | $V_{LVWL}$ | Low-voltage warning threshold — low range[9] $V_{DD}$ falling | | | | | | |
| | | | — | 2.11 | 2.16 | 2.22 | V | P |
| | | $V_{DD}$ rising | | | | | | |
| | | | — | 2.16 | 2.21 | 2.27 | V | P |
| 22 | $V_{hys}$ | Low-voltage inhibit reset/recoverhysteresis[10] | — | — | 50 | — | mV | C |
| 23 | $V_{BG}$ | Bandgap Voltage Reference[11] | — | 1.110 | 1.17 | 1.230 | V | P |

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above $V_{LVDL}$.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to $V_{DD}$ or $V_{SS}$ and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to $V_{SS}$ and $V_{DD}$ except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 Maximum is highest voltage that POR is guaranteed.

9 Run at 1 MHz bus frequency

10 Low voltage detection and warning limits measured at 1 MHz bus frequency.

11 Factory trimmed at $V_{DD}$ = 3.0 V, Temp = 25°C

## 3.6 Supply Current Characteristics

**Table 10. Supply Current Characteristics**

| # | Symbol | Parameter | Bus Freq | $V_{DD}$ (V) | Typ[1] | Max | Unit | Temp (°C) | C |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $RI_{DD}$ | Run supply current FEI mode; all modules ON[2] | | | | | | | |
| | | | 25.165 MHz | 3 | 44 | 48 | mA | –40 to 25 | P |
| | | | 25.165 MHz | 3 | 44 | 48 | mA | 105 | P |
| | | | 20 MHz | 3 | 32.3 | — | mA | –40 to 105 | T |
| | | | 8 MHz | 3 | 16.4 | — | mA | –40 to 105 | T |
| | | | 1 MHz | 3 | 2.9 | — | mA | –40 to 105 | T |
| 2 | $RI_{DD}$ | Run supply current FEI mode; all modules OFF[3] | | | | | | | |
| | | | 25.165 MHz | 3 | 29 | 29.6 | mA | –40 to 105 | C |
| | | | 20 MHz | 3 | 25.4 | — | mA | –40 to 105 | T |
| | | | 8 MHz | 3 | 12.7 | — | mA | –40 to 105 | T |
| | | | 1 MHz | 3 | 2.4 | — | mA | –40 to 105 | T |
| 3 | $RI_{DD}$ | Run supply current LPR=0; all modules OFF[3] | | | | | | | |
| | | | 16 kHz FBI | 3 | 232 | 280 | µA | –40 to 105 | T |
| | | | 16 kHz FBE | 3 | 231 | 296 | µA | –40 to 105 | T |
| 4 | $RI_{DD}$ | Run supply current LPR=1, all modules OFF[3] | | | | | | | |
| | | | 16 kHz BLPE | 3 | 74 | 75 | µA | 0 to 70 | T |
| | | | 16 kHz BLPE | 3 | 74 | 120 | µA | –40 to 105 | T |

**Table 10. Supply Current Characteristics (continued)**

| # | Symbol | Parameter | Bus Freq | $V_{DD}$ (V) | Typ[1] | Max | Unit | Temp (°C) | C |
|---|---|---|---|---|---|---|---|---|---|
| 5 | $WI_{DD}$ | Wait mode supply current FEI mode, all modules OFF[3] | | | | | | | |
| | | | 25.165 MHz | 3 | 16.5 | — | mA | –40 to 105 | C |
| | | | 20 MHz | 3 | 10.3 | — | mA | –40 to 105 | T |
| | | | 8 MHz | 3 | 6.6 | — | mA | –40 to 105 | T |
| | | | 1 MHz | 3 | 1.7 | — | mA | –40 to 105 | T |
| 6 | $LPWI_{DD}$ | Low-Power Wait mode supply current | | | | | | | |
| | | | 16 KHz | 3 | 28 | 62 | µA | –40 to 105 | T |
| 7 | $S2I_{DD}$ | Stop2 mode supply current[4] | | | | | | | |
| | | | N/A | 3 | 0.410 | 1.00 | µA | –40 to 25 | P |
| | | | N/A | 3 | 3.7 | 10 | µA | 70 | C |
| | | | N/A | 3 | 10 | 20 | µA | 85 | C |
| | | | N/A | 3 | 21 | 31.5 | µA | 105 | P |
| | | | N/A | 2 | 0.410 | 0.640 | µA | –40 to 25 | C |
| | | | N/A | 2 | 3.4 | 9 | µA | 70 | C |
| | | | N/A | 2 | 9.5 | 18 | µA | 85 | C |
| | | | N/A | 2 | 20 | 30 | µA | 105 | C |

**Table 10. Supply Current Characteristics (continued)**

| # | Symbol | Parameter | Bus Freq | $V_{DD}$ (V) | Typ[1] | Max | Unit | Temp (°C) | C |
|---|---|---|---|---|---|---|---|---|---|
| 8 | $S3I_{DD}$ | Stop3 mode supply current[4] No clocks active | n/a | 3 | 0.750 | 1.3 | μA | –40 to 25 | P |
| | | | | | 8.5 | 18 | | 70 | C |
| | | | | | 20 | 28 | | 85 | C |
| | | | | | 53 | 63 | | 105 | P |
| | | | | 2 | 0.400 | 0.900 | | –40 to 25 | C |
| | | | | | 8.2 | 16 | | 70 | C |
| | | | | | 18 | 26 | | 85 | C |
| | | | | | 47 | 59 | | 105 | C |

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 ON = System Clock Gating Control registers turn on system clock to the corresponding modules.

3 OFF = System Clock Gating Control registers turn off system Clock to the corresponding modules.

4 All digital pins must be configured to a known state to prevent floating pins from adding current. Smaller packages may have some pins that are not bonded out; however, software must still be configured to the largest pin package available so that all pins are in a known state. Otherwise, floating pins that are not bonded in the smaller packages may result in a higher current draw. NOTE: I/O pins are configured to output low; input-only pins are configured to pullup-enabled. IRO pin connects to ground. FB_AD12 pin is pullup-enabled. TRIAMPx, OPAMPx, DACO, and VREFO pins are at reset state and unconnected.

**Table 11. Typical Stop Mode Adders**

| # | Parameter | Condition | Temperature (°C) | | | | | Units | C |
|---|---|---|---|---|---|---|---|---|---|
| | | | -40 | 25 | 70 | 85 | 105 | | |
| 1 | LPO | — | 50 | 75 | 100 | 150 | 250 | nA | D |
| 2 | EREFSTEN | RANGE = HGO = 0 | 600 | 650 | 750 | 850 | 1000 | nA | D |
| 3 | IREFSTEN[1] | — | — | 73 | 80 | 93 | 125 | μA | T |
| 4 | TOD | Does not include clock source current | 50 | 75 | 100 | 150 | 250 | nA | D |
| 5 | LVD[1] | LVDSE = 1 | 116 | 117 | 126 | 132 | 172 | μA | T |
| 6 | PRACMP[1] | Not using the bandgap (BGBE = 0) | 17 | 18 | 24 | 35 | 74 | μA | T |
| 7 | ADC[1] | ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0) | 190 | 195 | 210 | 220 | 260 | μA | T |
| 8 | DAC[1] | High-Power mode; no load on DACO | 339 | 345 | 346 | 346 | 360 | μA | T |
| | | Low-Power mode | 41 | 43 | 43 | 44 | 50 | μA | T |
| 9 | OPAMP[1] | High-Power mode | 276 | 350 | 370 | 376 | 390 | μA | T |
| | | Low-Power mode | 42 | 49 | 57 | 58 | 68 | μA | T |
| 10 | TRIAMP[1] | High-Power mode | 420 | 432 | 433 | 438 | 478 | μA | T |
| | | Low-Power mode | 52 | 52 | 52 | 55 | 60 | μA | T |

1 Not available in stop2 mode.

**Table 15. 16-Bit ADC Operating Conditions (continued)**

| # | Symb | Characteristic | Conditions | Min | Typ[1] | Max | Unit | C | Comment |
|---|---|---|---|---|---|---|---|---|---|
| 5 | $V_{REFL}$ | Ref Voltage Low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | D | |
| 6 | $V_{ADIN}$ | Input Voltage | | $V_{REFL}$ | — | $V_{REFH}$ | V | D | |
| 7 | $C_{ADIN}$ | Input Capacitance | 16-bit modes<br>8/10/12-bit modes | — | 8<br>4 | 10<br>5 | pF | T | |
| 8 | $R_{ADIN}$ | Input Resistance | | — | 2 | 5 | kΩ | T | |
| 9 | $R_{AS}$ | Analog Source Resistance | | | | | | | External to MCU Assumes ADLSMP=0 |
| | | 16-bit mode | $f_{ADCK}$ > 8 MHz | — | — | 0.5 | kΩ | T | |
| | | | 4 MHz < $f_{ADCK}$ < 8 MHz | — | — | 1 | kΩ | T | |
| | | | $f_{ADCK}$ < 4 MHz | — | — | 2 | kΩ | T | |
| | | 13/12-bit mode | $f_{ADCK}$ > 8 MHz | — | — | 1 | kΩ | T | |
| | | | 4 MHz < $f_{ADCK}$ < 8 MHz | — | — | 2 | kΩ | T | |
| | | | $f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | T | |
| | | 11/10-bit mode | $f_{ADCK}$ > 8 MHz | — | — | 2 | kΩ | T | |
| | | | 4 MHz < $f_{ADCK}$ < 8 MHz | — | — | 5 | kΩ | T | |
| | | | $f_{ADCK}$ < 4 MHz | — | — | 10 | kΩ | T | |
| | | 9/8-bit mode | $f_{ADCK}$ > 8 MHz | — | — | 5 | kΩ | T | |
| | | | $f_{ADCK}$ < 8 MHz | — | — | 10 | kΩ | T | |
| 10 | $f_{ADCK}$ | ADC Conversion Clock Frequency | | | | | | | |
| | | ADLPC=0, ADHSC=1 | | 1.0 | — | 8.0 | MHz | D | |
| | | ADLPC=0, ADHSC=0 | | 1.0 | — | 5.0 | MHz | D | |
| | | ADLPC=1, ADHSC=0 | | 1.0 | — | 2.5 | MHz | D | |

1 Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

**Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq$ 8 MHz, –40 to 85 °C)**

| # | Characteristic | Conditions[1] | Symb | Min | Typ[2] | Max | Unit | C | Comment |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Supply Current | ADLPC=1, ADHSC=0 | $I_{DDAD}$ | — | 215 | — | μA | T | ADLSMP =0 ADCO=1 |
| | | ADLPC=0, ADHSC=0 | | — | 470 | — | | | |
| | | ADLPC=0, ADHSC=1 | | — | 610 | — | | | |
| 2 | Supply Current | Stop, Reset, Module Off | $I_{DDAD}$ | — | 0.01 | — | μA | T | |
| 3 | ADC Asynchronous Clock Source | ADLPC=1, ADHSC=0 | $f_{ADACK}$ | — | 2.4 | — | MHz | C | $t_{ADACK} = 1/f_{ADACK}$ |
| | | ADLPC=0, ADHSC=0 | | — | 5.2 | — | | | |
| | | ADLPC=0, ADHSC=1 | | — | 6.2 | — | | | |
| 4 | Sample Time | See Reference Manual for sample times | | | | | | | |
| 5 | Conversion Time | See Reference Manual for conversion times | | | | | | | |
| 6 | Total Unadjusted Error | 16-bit differential mode<br>16-bit single-ended mode | TUE | —<br>— | ±16<br>±20 | +48/ –40<br>+56/ –28 | LSB[3] | T | 32x Hardware Averaging (AVGE = %1 AVGS = %11) |
| | | 13-bit differential mode<br>12-bit single-ended mode | | —<br>— | ±1.5<br>±1.75 | ±3.0<br>±3.5 | | T | |
| | | 11-bit differential mode<br>10-bit single-ended mode | | —<br>— | ±0.7<br>±0.8 | ±1.5<br>±1.5 | | T | |
| | | 9-bit differential mode<br>8-bit single-ended mode | | —<br>— | ±0.5<br>±0.5 | ±1.0<br>±1.0 | | T | |
| 7 | Differential Non-Linearity | 16-bit differential mode<br>16-bit single-ended mode | DNL | —<br>— | ±2.5<br>±2.5 | +5/–3<br>+5/–3 | LSB[2] | T | |
| | | 13-bit differential mode<br>12-bit single-ended mode | | —<br>— | ±0.7<br>±0.7 | ±1<br>±1 | | T | |
| | | 11-bit differential mode<br>10-bit single-ended mode | | —<br>— | ±0.5<br>±0.5 | ±0.75<br>±0.75 | | T | |
| | | 9-bit differential mode<br>8-bit single-ended mode | | —<br>— | ±0.2<br>±0.2 | ±0.5<br>±0.5 | | T | |

**Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq$ 8 MHz, –40 to 85 °C) (continued)**

| # | Characteristic | Conditions[1] | Symb | Min | Typ[2] | Max | Unit | C | Comment |
|---|---|---|---|---|---|---|---|---|---|
| 14 | Total Harmonic Distortion | 16-bit differential mode Avg=32 | THD | — | –91.5 | –74.3 | dB | C | $F_{in} = F_{sample}/100$ |
| | | 16-bit single-ended mode Avg=32 | | — | –85.5 | — | | D | |
| 15 | Spurious Free Dynamic Range | 16-bit differential mode Avg=32 | SFDR | 75.0 | 92.2 | — | dB | C | $F_{in} = F_{sample}/100$ |
| | | 16-bit single-ended mode Avg=32 | | — | 86.2 | — | | D | |
| 16 | Input Leakage Error | all modes | $E_{IL}$ | $I_{In} * R_{AS}$ | | | mV | D | $I_{In}$ = leakage current (refer to DC characteristics) |
| 17 | Temp Sensor Slope | –40°C – 25°C | m | — | 1.646 | — | mV/×C | C | |
| | | 25°C – 125°C | | — | 1.769 | — | | | |
| 18 | Temp Sensor Voltage | 25°C | $V_{TEMP25}$ | — | 718.2 | — | mV | C | |

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}$

2 Typical values assume $V_{DDA}$ = 3.0V, Temp = 25°C, $f_{ADCK}$=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{BUS}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via $V_{DD}$ and $V_{SS}$ and variation in crystal oscillator frequency increase the $C_{Jitter}$ percentage for a given interval.

5 625 ns represents 5 time quanta for CAN applications, under worst-case conditions of 8 MHz CAN bus clock, 1 Mbps CAN Bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

6 Below $D_{lock}$ minimum, the MCG is guaranteed to enter lock. Above $D_{lock}$ maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

7 Below $D_{unl}$ minimum, the MCG will not exit lock if already in lock. Above $D_{unl}$ maximum, the MCG is guaranteed to exit lock.

**Table 19. XOSC (Temperature Range = –40 to 105°C Ambient)**

| # | Characteristic | | Symbol | Min | Typ[1] | Max | Unit | C |
|---|---|---|---|---|---|---|---|---|
| 1 | Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) | • Low range (RANGE = 0) | $f_{lo}$ | 32 | — | 38.4 | kHz | D |
| | | • High range (RANGE = 1),<br>• FEE or FBE mode [2] | $f_{hi-fll}$ | 1 | — | 5 | MHz | D |
| | | • High range (RANGE = 1),<br>• PEE or PBE mode [3] | $f_{hi-pll}$ | 1 | — | 16 | MHz | D |
| | | • High range (RANGE = 1),<br>• High gain (HGO = 1),<br>• BLPE mode | $f_{hi-hgo}$ | 1 | — | 16 | MHz | D |
| | | • High range (RANGE = 1),<br>• Low power (HGO = 0),<br>• BLPE mode | $f_{hi-lp}$ | 1 | — | 8 | MHz | D |
| 2 | Load capacitors | | $C_1$<br>$C_2$ | See crystal or resonator manufacturer's recommendation. | | | | D |
| 3 | Feedback resistor | • Low range<br>(32 kHz to 38.4 kHz) | $R_F$ | — | 10 | — | MΩ | D |
| | | • High range<br>(1 MHz to 16 MHz) | — | — | 1 | — | | D |
| 4 | Series resistor — Low range | • Low Gain (HGO = 0) | $R_S$ | — | 0 | — | kΩ | D |
| | | • High Gain (HGO = 1) | | — | 100 | — | | D |
| 5 | Series resistor — High range | • Low Gain (HGO = 0) | $R_S$ | — | 0 | — | kΩ | D |
| | | • High Gain (HGO = 1) | | | | | | D |
| | | ≥ 8 MHz | | — | 0 | 0 | | D |
| | | 4 MHz | | — | 0 | 10 | | D |
| | | 1 MHz | | — | 0 | 20 | | D |

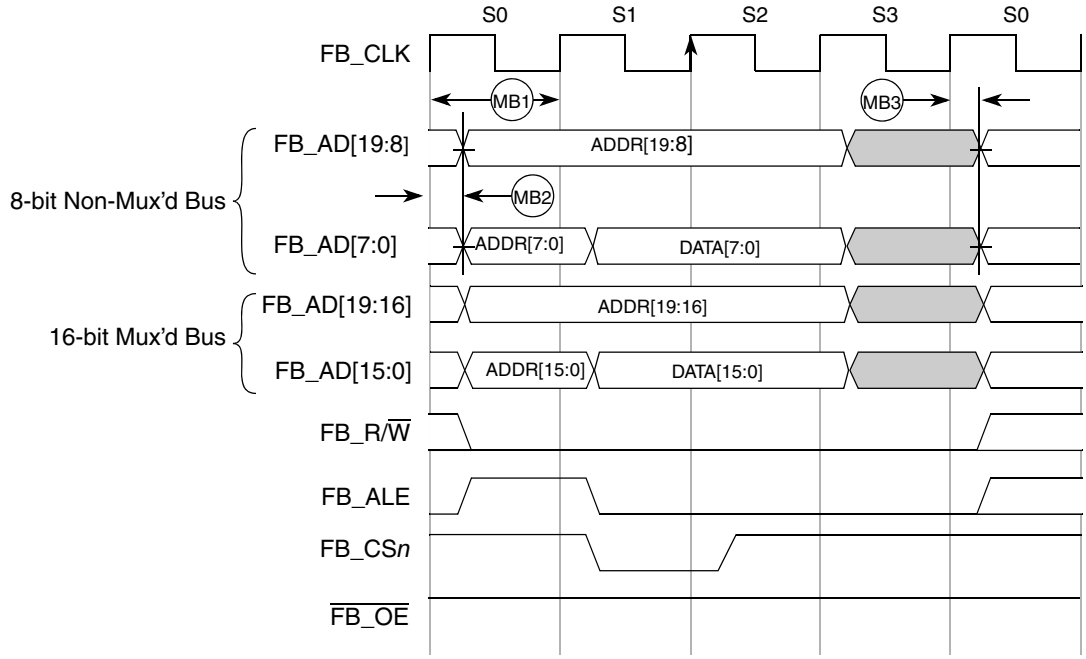



**Figure 10. Mini-FlexBus Write Timing**

## 3.12.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

**Table 22. TPM Input Timing**

| # | C | Function | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | — | External clock frequency | $f_{TPMext}$ | dc | $f_{Bus}/4$ | MHz |
| 2 | — | External clock period | $t_{TPMext}$ | 4 | — | $t_{cyc}$ |
| 3 | D | External clock high time | $t_{clkh}$ | 1.5 | — | $t_{cyc}$ |
| 4 | D | External clock low time | $t_{clkl}$ | 1.5 | — | $t_{cyc}$ |
| 5 | D | Input capture pulse width | $t_{ICPW}$ | 1.5 | — | $t_{cyc}$ |

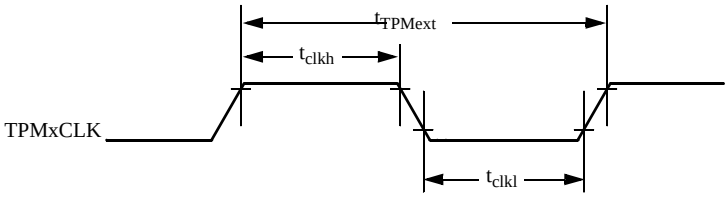



**Figure 13. Timer External Clock**

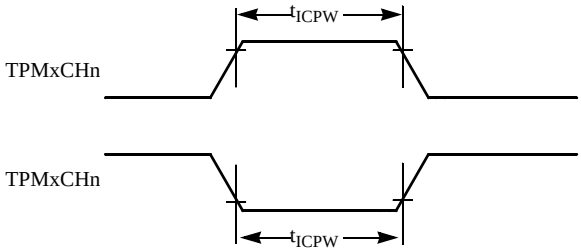
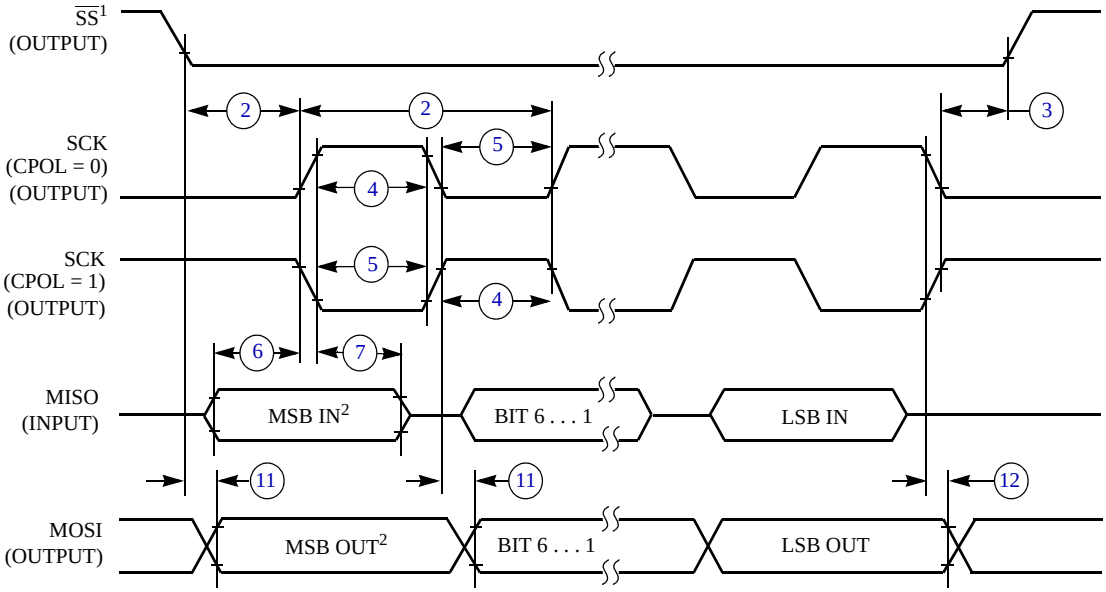
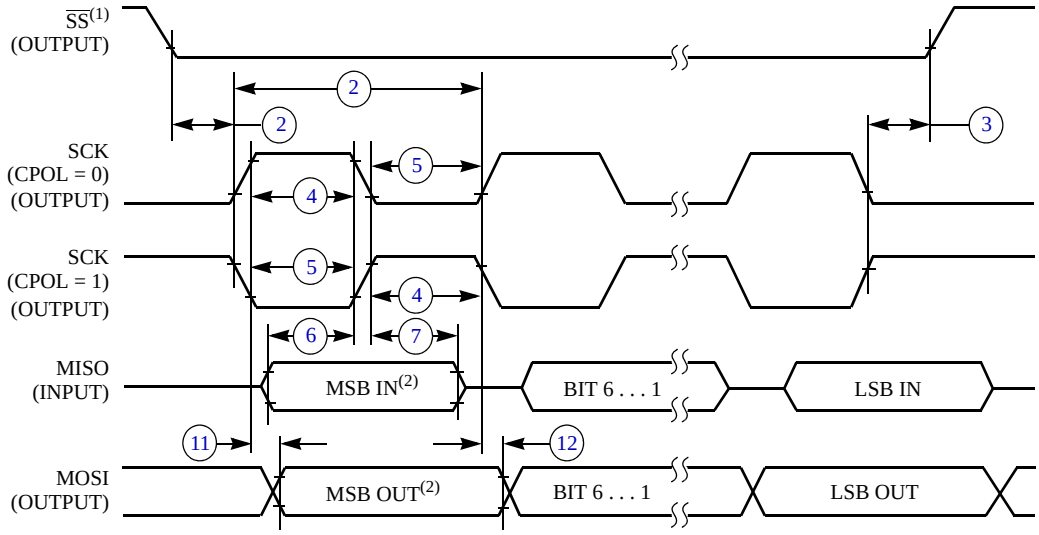



**Figure 14. Timer Input Capture Pulse**




NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 15. SPI Master Timing (CPHA = 0)**




NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 16. SPI Master Timing (CPHA = 1)**

## 3.16 VREF Electrical Specifications

**Table 26. VREF Electrical Specifications**

| # | Characteristic | Symbol | Min | Max | Unit | C |
|---|---|---|---|---|---|---|
| 1 | Supply voltage | $V_{DDA}$ | 1.80 | 3.6 | V | C |
| 2 | Operating temperature range | $T_A$ | –40 | 105 | °C | C |
| 3 | Output Load Capacitance | $C_L$ | — | 100 | nF | D |
| 4 | Maximum Load | — | — | 10 | mA | — |
| 5 | Voltage Reference Output with Factory Trim. $V_{DD}$ = 3 V at 25 °C | $V_{out}$ | 1.145 | 1.153 | V | P |
| 6 | Temperature Drift ($V_{min}$—$V_{max}$ across the full temperature range) | Tdrift | — | 25 | mV[1] | T |
| 7 | Aging Coefficient[2] | $A_C$ | — | 60 | µV/year | C |
| 8 | Powered down Current (Off Mode, VREFEN=0, VRSTEN=0) | I | — | 0.10 | µA | C |
| 9 | Bandgap only (Mode_LV[1:0] = 00) | I | — | 75 | µA | T |
| 10 | Low-Power buffer (MODE_LV[1:0] = 01) | I | — | 125 | µA | T |
| 11 | Tight-Regulation buffer (MODE_LV[1:0] = 10) | I | — | 1.1 | mA | T |
| 12 | Load Regulation MODE_LV = 10 | — | — | 100 | µV/mA | C |
| 13 | Line Regulation MODE = 1:0, Tight Regulation $V_{DD}$ < 2.3 V, Delta $V_{DDA}$ =100 mV, VREFH = 1.2 V driven externally with VREFO disabled. (Power Supply Rejection) | DC | 70 | — | dB | C |

1 See typical chart that follows (Figure 20).

2 Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging µV/year. VREF0 data recorded per month.

**Table 27. VREF Limited Range Operating Behaviors**

| # | Characteristic | Symbol | Min | Max | Unit | C |
|---|---|---|---|---|---|---|
| 1 | Voltage Reference Output with Factory Trim (Temperature range from 0°C to 50 °C) | $V_{out}$ | 1.149 | 1.152 | mV | T |
| 2 | Temperature Drive ($V_{min}$ —$V_{max}$ Temperature range from 0 °C to 50 °C) | $T_{drift}$ | — | 3 | mV[1] | T |

1 See typical chart that follows (Figure 20).

**How to Reach Us:**

**Home Page:**
www.freescale.com

**Web Support:**
http://www.freescale.com/support

**USA/Europe or Locations Not Listed:**
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

**Europe, Middle East, and Africa:**
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MCF51MM256
Rev. 5
07/2012