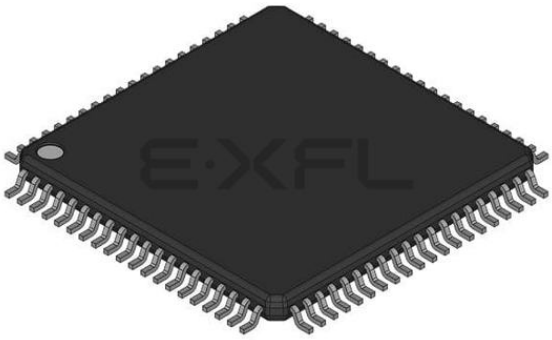


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	47
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x16b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51mm256vlk

1 Features

The following table provides a cross-comparison of the features of the MCF51MM256/128 according to package.

Table 1. MCF51MM256/128 Features by MCU and Package

Feature	MCF51MM256				MCF51MM128	
FLASH Size (bytes)	262144				131072	
RAM Size (bytes)	32K				32K	
Pin Quantity	104	100	81	80	81	80
Programmable Analog Comparator (PRACMP)	yes	yes	yes	yes	yes	yes
Debug Module (DBG)	yes	yes	yes	yes	yes	yes
Multipurpose Clock Generator (MCG)	yes	yes	yes	yes	yes	yes
Inter-Integrated Communication (IIC)	yes	yes	yes	yes	yes	yes
Interrupt Request Pin (IRQ)	yes	yes	yes	yes	yes	yes
Keyboard Interrupt (KBI)	16	16	16	16	16	16
Digital General Purpose I/O[1]	69	65	48	47	48	47
Dedicated Analog Input Pins	14	14	14	14	14	14
Power and Ground Pins	8	8	8	8	8	8
Time Of Day (TOD)	yes	yes	yes	yes	yes	yes
Serial Communications (SCI1)	yes	yes	yes	yes	yes	yes
Serial Communications (SCI2)	yes	yes	yes	yes	yes	yes
Serial Peripheral Interface (SPI1(FIFO))	yes	yes	yes	yes	yes	yes
Serial Peripheral Interface(SPI2)	yes	yes	yes	yes	yes	yes
Carrier Modulator Timer Pin (IRO)	yes	yes	yes	yes	yes	yes
TPM Input Clock Pin (TPMCLK)	yes	yes	yes	yes	yes	yes
TPM1 Channels	4	4	4	4	4	4
TPM2 Channels	4	4	4	4	4	4
XOSC1	yes	yes	yes	yes	yes	yes
XOSC2	yes	yes	yes	yes	yes	yes
USB On-the-Go	yes	yes	yes	yes	yes	yes
Mini-FlexBus	yes	yes	DATA[2]	DATA[2]	DATA[2]	DATA[2]
Rapid GPIO	16	16	9	9	9	9
MEASUREMENT ENGINE						
Programmable Delay Block (PDB)	yes	yes	yes	yes	yes	yes
16-Bit SAR ADC Differential Channels[3]	4	4	4	4	4	4
16-Bit SAR ADC Single-Ended Channels	8	8	8	8	8	8
DAC Ouput Pin (DACO)	yes	yes	yes	yes	yes	yes
Voltage Reference Output Pin (VREFO)	yes	yes	yes	yes	yes	yes
General Purpose Operational Amplifier (OPAMP)	yes	yes	yes	yes	yes	yes
Trans-Impedance Amplifier (TRIAMP)	yes	yes	yes	yes	yes	yes

1 Port I/O count does not include $\overline{\text{BLMS}}$, BKGD and IRQ. $\overline{\text{BLMS}}$ and BKGD are Output only, IRQ is input only.

2 The 80/81 pin packages contain the Mini-FlexBus data pins to support an 8-bit data bus interface to external peripherals.

3 Each differential channel is comprised of 2 pin inputs.

The following table describes the functional units of the MCF51MM256/128.

Table 2. MCF51MM256/128 Functional Units

Unit	Function
Measurement Engine	DAC (digital to analog converter) — Used to output voltage levels.
	16-BIT SAR ADC (analog-to-digital converter) — Measures analog voltages at up to 16 bits of resolution. The ADC has up to four differential and 8 single-ended inputs.
	OPAMP — General purpose op amp used for signal filtering or amplification.
	TRIAMP —- Transimpedance amplifier optimized for converting small currents into voltages.
	Measurement Engine PDB — The measurement engine PDB is used to precisely trigger the DAC and the ADC modules to complete sensor biasing and measuring.
Mini-FlexBus	Provides expansion capability for off-chip memory and peripherals.
USB On-the-Go	Supports the USB On-the-Go dual-role controller.
CMT (Carrier Modulator Timer)	Infrared output used for the Remote Controller operation.
MCG (Multipurpose Clock Generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources.
BDM (Background Debug Module)	Provides single pin debugging interface (part of the V1 ColdFire core).
CF1 CORE (V1 ColdFire Core)	Executes programs and interrupt handlers.
PRACMP	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (Computer Operating Properly)	Software Watchdog.
IRQ (Interrupt Request)	Single-pin high-priority interrupt (part of the V1 ColdFire core).
CRC (Cyclic Redundancy Check)	High-speed CRC calculation.
DBG (Debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire. core)
FLASH (Flash Memory)	Provides storage for program code, constants, and variables.
IIC (Inter-integrated Circuits)	Supports standard IIC communications protocol and SMBus.
INTC (Interrupt Controller)	Controls and prioritizes all device interrupts.
KBI1 & KBI2	Keyboard Interfaces 1 and 2.
LVD (Low-voltage Detect)	Provides an interrupt to the ColdFire V1 CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event.
VREF (Voltage Reference)	The Voltage Reference output is available for both on- and off-chip use.
RAM (Random-Access Memory)	Provides stack and variable storage.
RGPIO (Rapid General-purpose Input/output)	Allows for I/O port access at CPU clock speeds. RGPIO is used to implement GPIO functionality.

2 Pinouts and Pin Assignments

2.1 104-Pin MAPBGA

The following figure shows the 104-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTF6	PTF7	USB_DP	USB_DM	VUSB33	PTF4	PTF3	FB_AD12	PTJ7	PTJ5	PTJ4	A
B	PTG0	PTA0	PTG3	VBUS	PTF5	PTJ6	PTH0	PTE5	PTF0	PTF1	PTF2	B
C	IRO	PTG4	PTA6	PTG2	PTG6	PTG5	PTG7	PTH1	PTE4	PTE6	PTE7	C
D	PTA5	PTA4	PTB1	VDD1		VDD2		VDD3	PTA1	PTE3	PTE2	D
E	VSSA	PTA7	PTB0						PTA2	PTJ3	PTE1	E
F	VREFL	INP1-	INP2-	PTG1				PTC7	PTJ2	PTJ0	PTJ1	F
G	TRIOUT1	OUT1	OUT2						PTD5	PTD7	PTE0	G
H	VINP1	VINN1	PTA3	VSS1		VSS2		VSS3	PTD4	PTD3	PTD2	H
J	DADP0	DADM0	PTH7	PTH6	PTH4	PTH3	PTH2	PTD6	PTC2	PTC0	PTC1	J
K	VINP2	VINN2	DADP1	PTH5	PTB6	PTB7	PTC3	PTD1	PTC4	PTC5	PTC6	K
L	TRIOUT2	DACO	DADM1	VREFO	VREFH	VDDA	PTB3	PTB2	PTD0	PTB5	PTB4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. 104-Pin MAPBGA

2.2 100-Pin LQFP

The following figure shows the 100-pin LQFP pinout configuration.

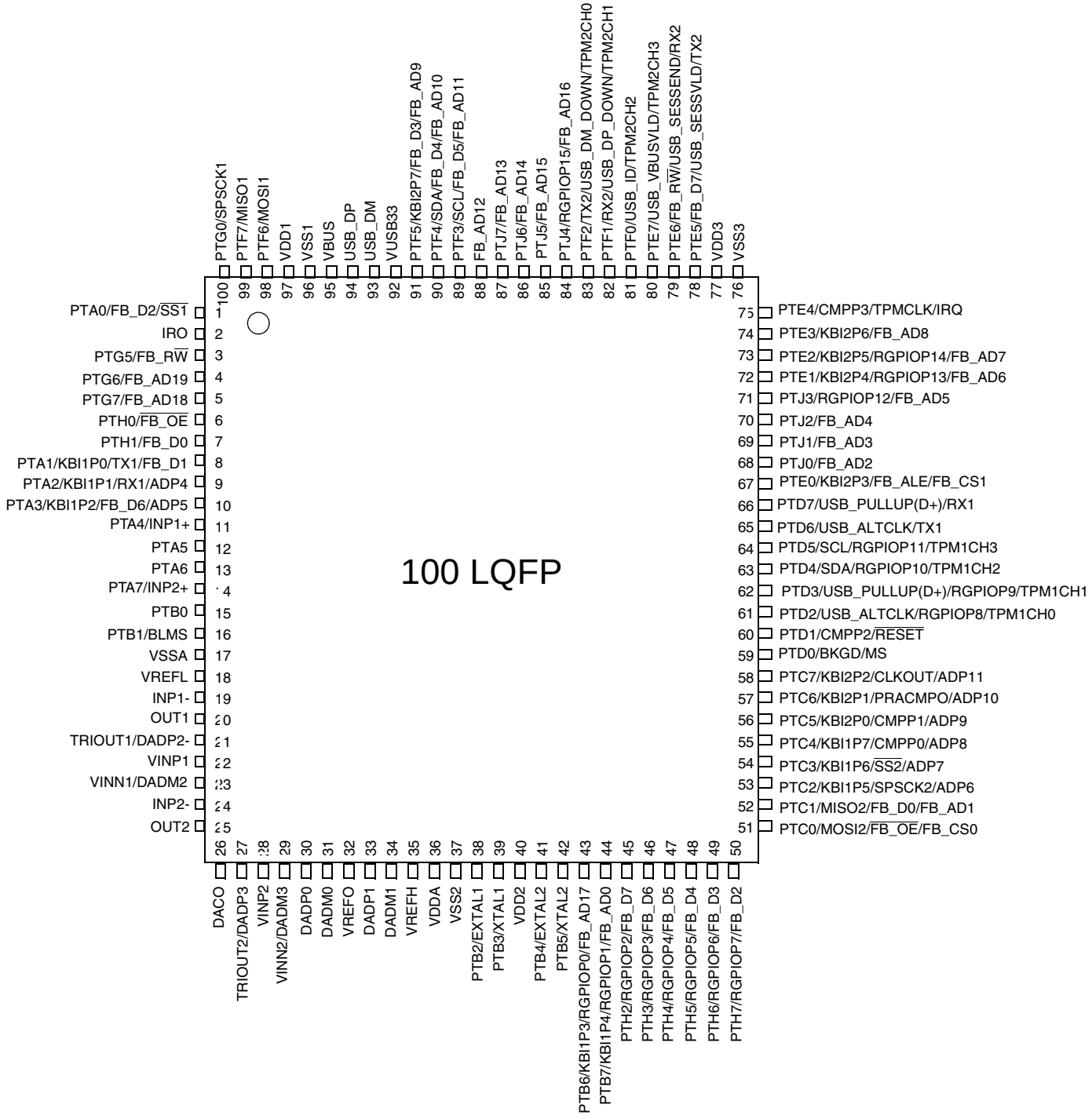


Figure 3. 100-Pin LQFP

2.5 Pin Assignments

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
B2	1	B2	1	PTA0	FB_D2	$\overline{SS1}$	—	PTA0/FB_D2/$\overline{SS1}$
C1	2	A1	2	IRO	—	—	—	IRO
C6	3	—	—	PTG5	FB_$\overline{RW}$	—	—	PTG5/FB_$\overline{RW}$
C5	4	—	—	PTG6	FB_AD19	—	—	PTG6/FB_AD19
C7	5	—	—	PTG7	FB_AD18	—	—	PTG7/FB_AD18
B7	6	—	—	PTH0	$\overline{FB\_OE}$	—	—	PTH0/$\overline{FB\_OE}$
C8	7	—	—	PTH1	FB_D0	—	—	PTH1/FB_D0
D9	8	C4	3	PTA1	KBI1P0	TX1	FB_D1	PTA1/KBI1P0/TX1/FB_D1
E9	9	D5	4	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
H3	10	D6	5	PTA3	KBI1P2	FB_D6	ADP5	PTA3/KBI1P2/FB_D6/ADP5
D2	11	C1	6	PTA4	INP1+	—	—	PTA4/INP1+
D1	12	C2	7	PTA5	—	—	—	PTA5
C3	13	C3	8	PTA6	—	—	—	PTA6
E2	14	D2	9	PTA7	INP2+	—	—	PTA7/INP2+
E3	15	D3	10	PTB0	—	—	—	PTB0
D3	16	D4	11	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
E1	17	J1	12	VSSA	—	—	—	VSSA
F1	18	J2	13	VREFL	—	—	—	VREFL
F2	19	D1	14	INP1-	—	—	—	INP1-
G2	20	E1	15	OUT1	—	—	—	OUT1
G1	21	F2	16	DADP2	TRIOUT1	—	—	DADP2/TRIOUT1
H1	22	F1	17	VINP1	—	—	—	VINP1
H2	23	E2	18	DADM2	VINN1	—	—	DADM2/VINN1
F3	24	F3	19	INP2-	—	—	—	INP2-
G3	25	E3	20	OUT2	—	—	—	OUT2
L2	26	G2	21	DACO	—	—	—	DACO
L1	27	G3	22	DADP3	TRIOUT2	—	—	DADP3/TRIOUT2
K1	28	H4	23	VINP2	—	—	—	VINP2
K2	29	G4	24	DADM3	VINN2	—	—	DADM3/VINN2

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
H11	61	E7	50	PTD2	USB_ALTCLK	RGPIOP8	TPM1CH0	PTD2/USB_ALTCLK/RGPIOP8/TPM1CH0
H10	62	E8	51	PTD3	USB_PULLUP (D+)	RGPIOP9	TPM1CH1	PTD3/USB_PULLUP(D+)/RGPIOP9/TPM1CH1
H9	63	F9	52	PTD4	SDA	RGPIOP10	TPM1CH2	PTD4/SDA/RGPIOP10/TPM1CH2
G9	64	D7	53	PTD5	SCL	RGPIOP11	TPM1CH3	PTD5/SCL/RGPIOP11/TPM1CH3
J8	65	E9	54	PTD6	USB_ALTCLK	TX1	—	PTD6/USB_ALTCLK/TX1
G10	66	D8	55	PTD7	USB_PULLUP (D+)	RX1	—	PTD7/USB_PULLUP(D+) /RX1
G11	67	D9	56	PTE0	KBI2P3	FB_ALE	FB_CS1	PTE0/KBI2P3/FB_ALE/FB_CS1
F10	68	—	—	PTJ0	FB_AD2	—	—	PTJ0/FB_AD2
F11	69	—	—	PTJ1	FB_AD3	—	—	PTJ1/FB_AD3
F9	70	—	—	PTJ2	FB_AD4	—	—	PTJ2/FB_AD4
E10	71	—	—	PTJ3	RGPIOP12	FB_AD5	—	PTJ3/RGPIOP12/FB_AD5
E11	72	C9	57	PTE1	KBI2P4	RGPIOP13	FB_AD6	PTE1/KBI2P4/RGPIOP13/FB_AD6
D11	73	C8	58	PTE2	KBI2P5	RGPIOP14	FB_AD7	PTE2/KBI2P5/RGPIOP14/FB_AD7
D10	74	B9	59	PTE3	KBI2P6	FB_AD8	—	PTE3/KBI2P6/FB_AD8
C9	75	A9	60	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/IRQ
H8	76	F5	61	VSS3	—	—	—	VSS3
D8	77	E5	62	VDD3	—	—	—	VDD3
B8	78	C7	63	PTE5	FB_D7	USB_ SESSVLD	TX2	PTE5/FB_D7/USB_SESSVLD/TX2
C10	79	C6	64	PTE6	FB_R$\overline{W}$	USB_ SESSEND	RX2	PTE6/FB_R$\overline{W}$/USB_SESSEND/RX2
C11	80	B6	65	PTE7	USB_ VBUSVLD	TPM2CH3	—	PTE7/USB_VBUSVLD/TPM2CH3
B9	81	B8	66	PTF0	USB_ID	TPM2CH2	—	PTF0/USB_ID/TPM2CH2
B10	82	B7	67	PTF1	RX2	USB_DP_D OWN	TPM2CH1	PTF1/RX2/USB_DP_DOWN/TPM2CH1
B11	83	C5	68	PTF2	TX2	USB_DM_ DOWN	TPM2CH0	PTF2/TX2/USB_DM_DOWN/TPM2CH0
A11	84	—	—	PTJ4	RGPIOP15	FB_AD16	—	PTJ4/RGPIOP15/FB_AD16
A10	85	—	—	PTJ5	FB_AD15	—	—	PTJ5/FB_AD15
B6	86	—	—	PTJ6	FB_AD14	—	—	PTJ6/FB_AD14
A9	87	—	—	PTJ7	FB_AD13	—	—	PTJ7/FB_AD13

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Min	Max	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T

Table 8. ESD and Latch-Up Protection Characteristics (continued)

3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at T_A = 125°C	I_{LAT}	±100	—	mA	T

Table 9. DC Characteristics (continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
20	V_{LVWH}	Low-voltage warning threshold — high range[9] V_{DD} falling						
			—	2.36	2.46	2.56	V	P
		V_{DD} rising						
			—	2.36	2.46	2.56	V	P
21	V_{LVWL}	Low-voltage warning threshold — low range[9] V_{DD} falling						
			—	2.11	2.16	2.22	V	P
		V_{DD} rising						
			—	2.16	2.21	2.27	V	P
22	V_{hys}	Low-voltage inhibit reset/recoverhysteresis[10]	—	—	50	—	mV	C
23	V_{BG}	Bandgap Voltage Reference[11]	—	1.110	1.17	1.230	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to V_{DD} or V_{SS} and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 Maximum is highest voltage that POR is guaranteed.

9 Run at 1 MHz bus frequency

10 Low voltage detection and warning limits measured at 1 MHz bus frequency.

11 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

Table 10. Supply Current Characteristics (continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	16.5	—	mA	–40 to 105	C
			20 MHz	3	10.3	—	mA	–40 to 105	T
			8 MHz	3	6.6	—	mA	–40 to 105	T
			1 MHz	3	1.7	—	mA	–40 to 105	T
6	$LPWI_{DD}$	Low-Power Wait mode supply current							
			16 KHz	3	28	62	µA	–40 to 105	T
7	$S2I_{DD}$	Stop2 mode supply current[4]							
			N/A	3	0.410	1.00	µA	–40 to 25	P
			N/A	3	3.7	10	µA	70	C
			N/A	3	10	20	µA	85	C
			N/A	3	21	31.5	µA	105	P
			N/A	2	0.410	0.640	µA	–40 to 25	C
			N/A	2	3.4	9	µA	70	C
			N/A	2	9.5	18	µA	85	C
			N/A	2	20	30	µA	105	C

Table 14. DAC 12-Bit Operating Behaviors (continued)

#	Characteristic	Symbol	Min	Typ	Max	Unit	C	Notes
2	Supply current low-power mode	I_{DDA_DACLP}	—	50	100	µA	T	
3	Supply current high-power mode	I_{DDA_DACHP}	—	345	500	µA	T	
4	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$Ts_{FS}LP$	—	—	200	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
5	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$Ts_{FS}HP$	—	—	30	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
6	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$Ts_{C-C}LP$	—	—	5	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
7	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode (3 V at Room Temperature)	$Ts_{C-C}HP$	—	1	—	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
8	DAC output voltage range low (high-power mode, no load, DAC set to 0) (3 V at Room Temperature)	$V_{dacoutl}$	—	—	100	mV	T	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	V_{DACR} -100	—	—	mV	T	
10	Integral non-linearity error	INL	—	—	± 8	LSB	T	
11	Differential non-linearity error VDACR is > 2.4 V	DNL	—	—	± 1	LSB	T	
12	Offset error	E_O	—	±0.4	± 3	%FSR	T	Calculated by a best fit curve from V_{SS} + 100mV to V_{REFH} –100mV
13	Gain error, $V_{REFH} = V_{ext} = V_{DD}$	E_G	—	±0.1	± 0.5	%FSR	T	Calculated by a best fit curve from V_{SS} + 100mV to V_{REFH} –100mV

Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq 8$ MHz, –40 to 85 °C) (continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
8	Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	INL	— —	±6.0 ±10.0	±16.0 ±20.0	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±2.5 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	
9	Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{ZS}	— —	±4.0 ±4.0	+32/ –24 +24/ –16	LSB[2]	T	$V_{ADIN} = V_{SSA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.5 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
10	Full-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{FS}	— —	+10/0 +14/0	+42/–2 +46/–2	LSB[2]	T	$V_{ADIN} = V_{DDA}$
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±3.5 ±3.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.5 ±1.5		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
11	Quantization Error	16-bit modes	E_Q	—	–1 to 0	—	LSB[2]	D	
		≤13-bit modes		—	—	±0.5			
12	Effective Number of Bits	16-bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	ENOB	 12.8 12.7 12.6 12.5 11.9	 14.2 13.8 13.6 13.3 12.5	 — — — — —	Bits	C	$F_{in} = F_{sample}/100$
13	Signal to Noise plus Distortion	See ENOB	SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB		

Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, $f_{ADACK} \leq 4$ MHz, ADHSC = 1)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+24/ –24 +32/–20	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.0 ±1.25		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
2	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
3	Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	
4	Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-8	LSB[2]	T	$V_{ADIN} = V_{SSA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

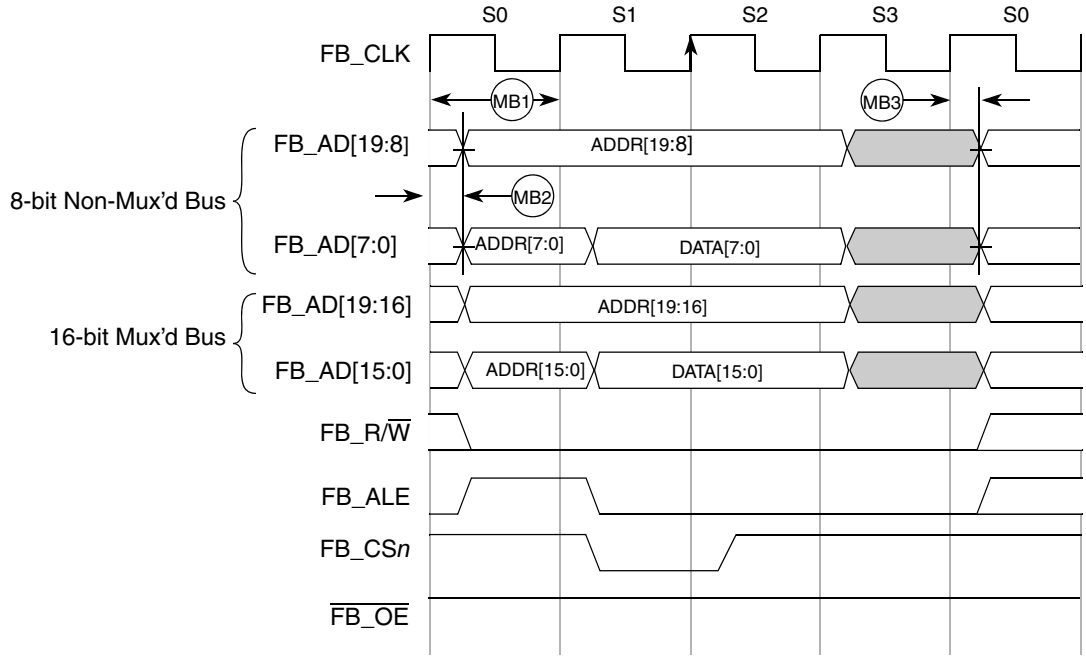
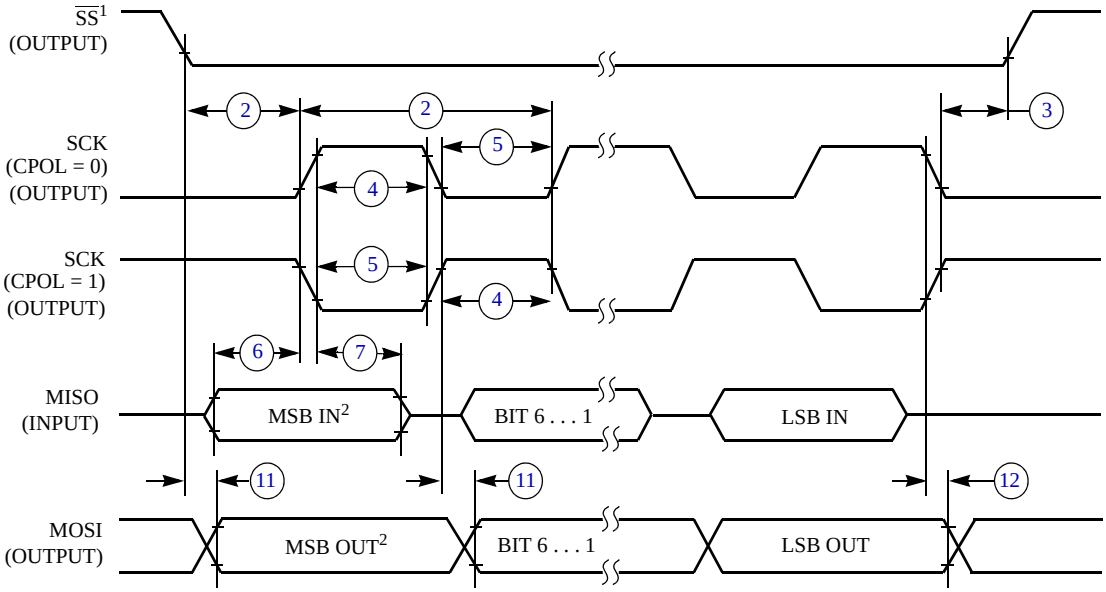
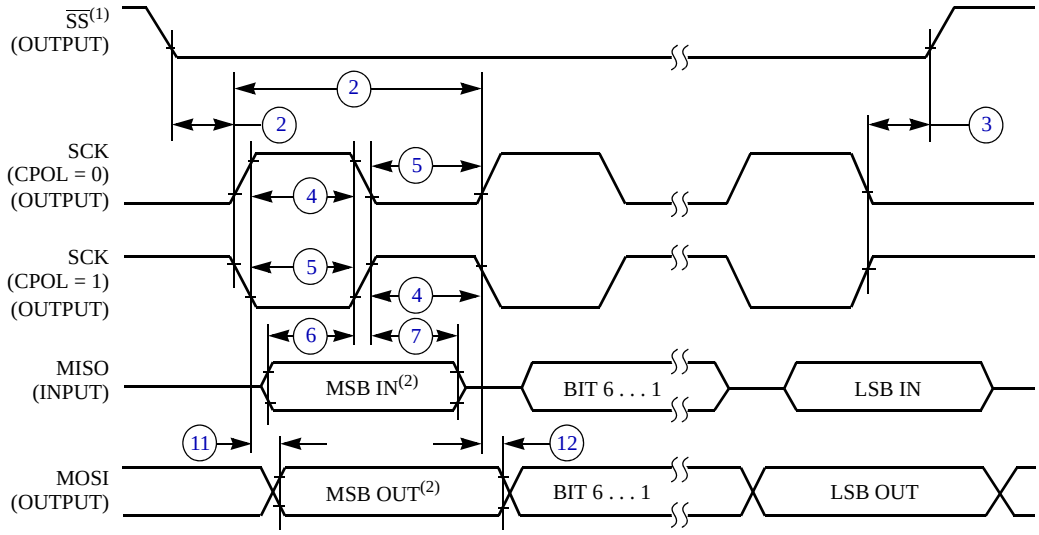


Figure 10. Mini-FlexBus Write Timing



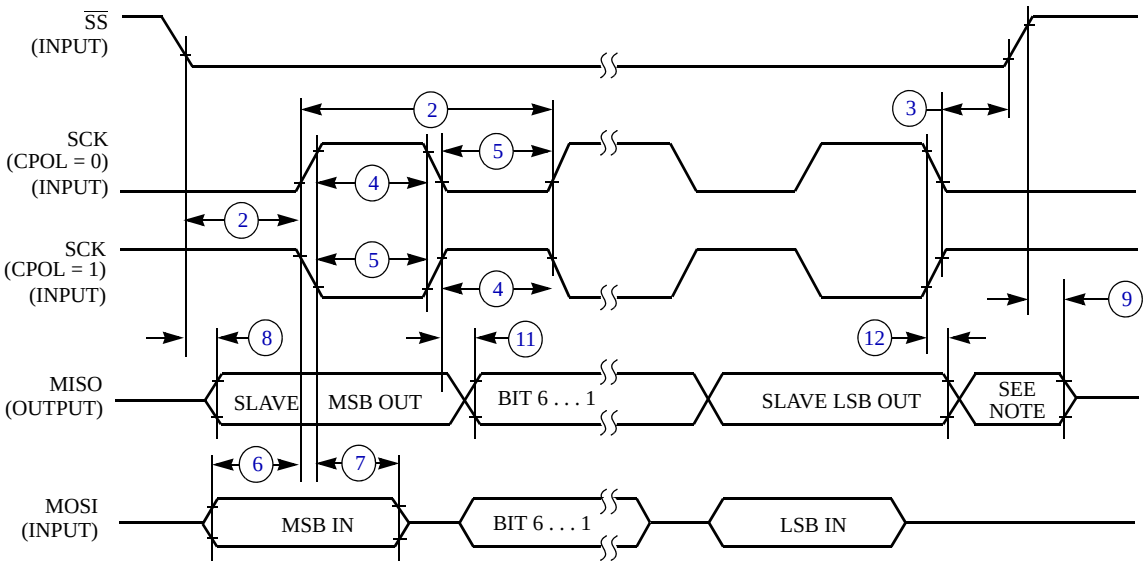
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

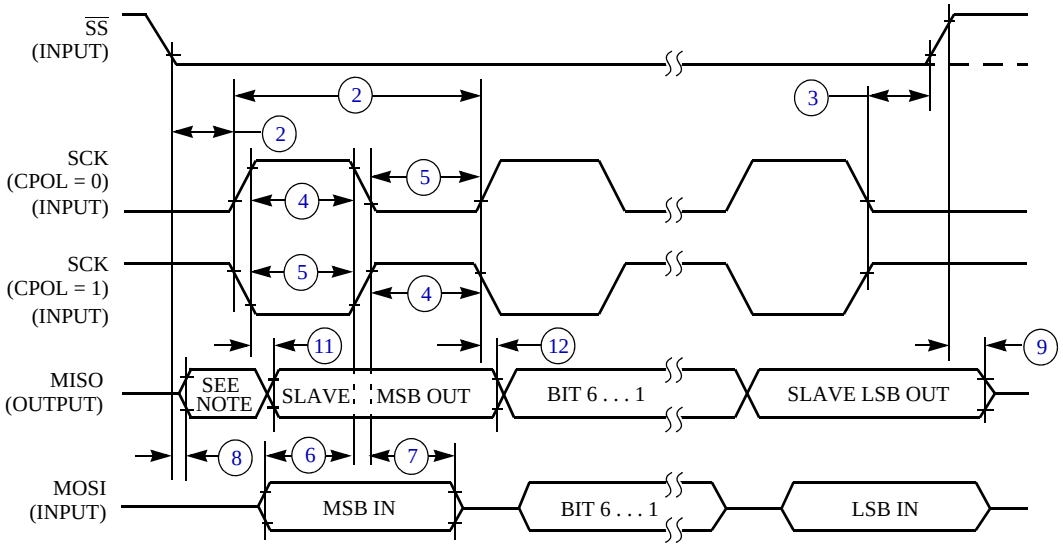
Figure 16. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined, but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51MM256RM).

Table 24. Flash Characteristics

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage for program/erase –40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 25. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

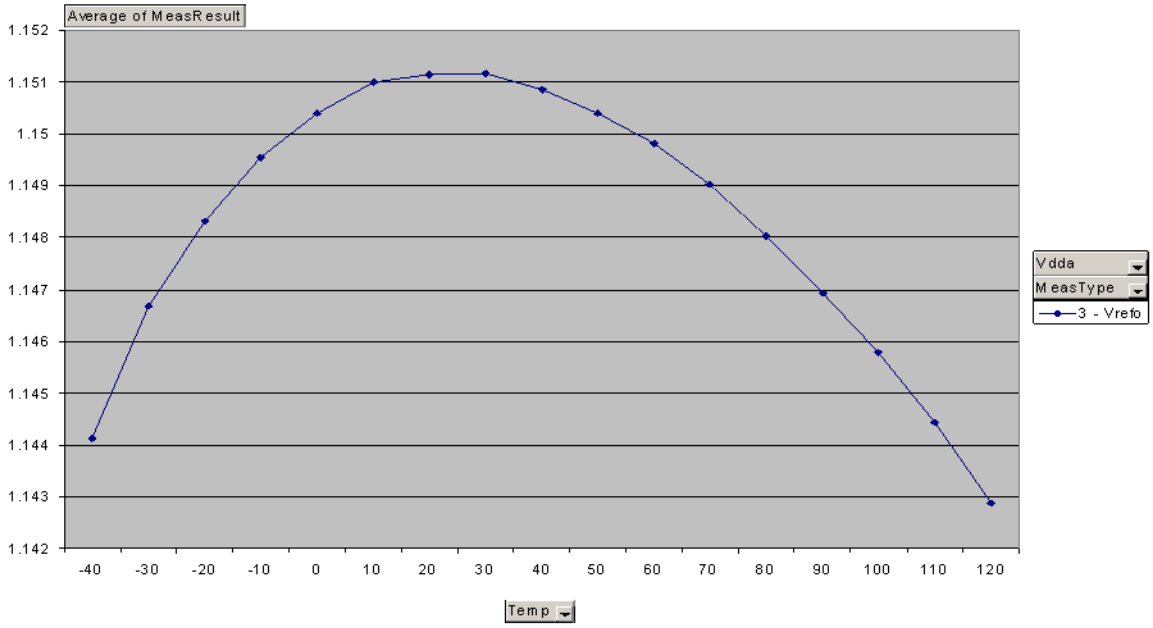


Figure 19. Typical VREF Output vs. Temperature

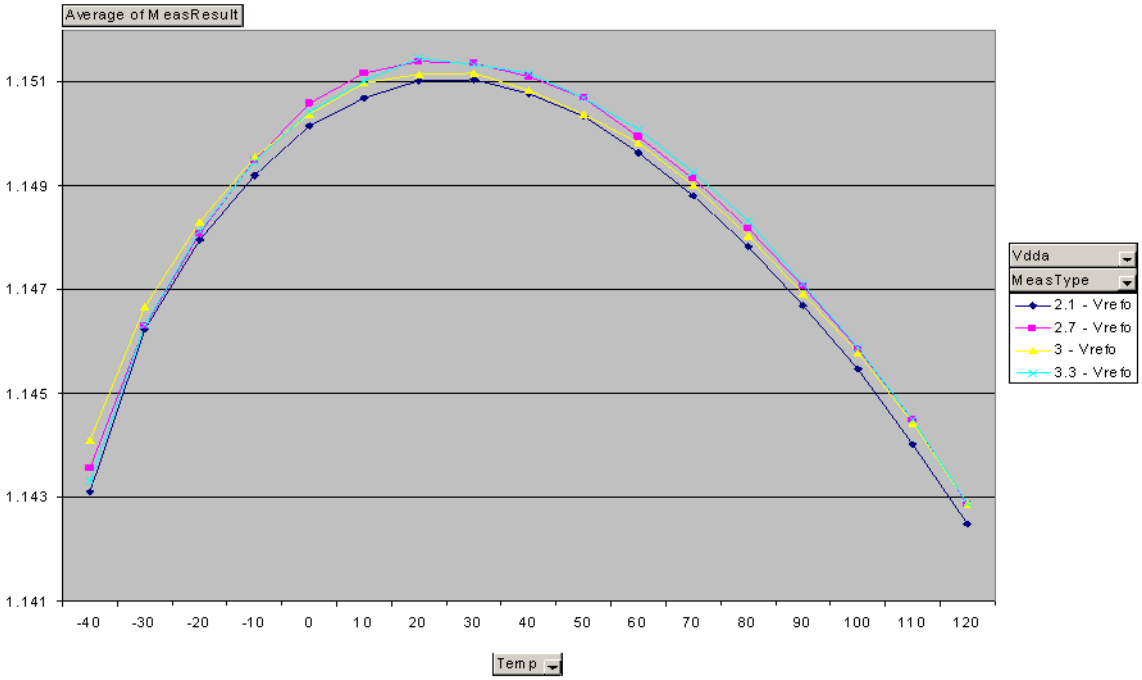


Figure 20. Typical VREF Output vs. V_{DD}

5 Revision History

This section lists major changes between versions of the MCF51MM256 Data Sheet.

Table 32. Revision History

Revision	Date	Description
0	March/April 2009	Initial Draft
1	July 2009	• Revised to follow standard template. • Removed extraneous headings from the TOC. • Corrected units for Monotonocity to be blank in for the DAC specification. • Updated ADC characteristic tables to include 16-Bit SAR in headings.
2	July 2009	• Changed MCG (XOSC) Electricals Table - Row 2, Average Internal Reference Frequency typical value from 32.768 to 31.25.
3	April 2010	• Updated Thermal Characteristics table. Reinserted the 81 and 104 MapBGA devices. • Revised the ESD and Latch-Up Protection Characteristic description to read: Latch-up Current at T_A = 125°C. • Changed Table 9. DC Characteristics rows 2 and 4, to 1.8 V, ILoad = -600 mA conditions to 1.8 V, ILoad = 600μA respectively. • Corrected the 16-bit SAR ADC Operating Condition table Ref Voltage High Min value to be 1.13 instead of 1.15. • Updated the ADC electricals. • Inserted the Mini-FlexBus Timing Specifications. • Added a Temp Drift parameter to the VREF Electrical Specifications. • Removed the S08 Naming Convention diagram. • Updated the Orderable Part Number Summary to include the Freescale Part Number suffixes. • Completed the Package Description table values. • Changed the 80LQFP package drawing from 98ARL10530D to 98ASS23174W. • Updated electrical characteristic data.
4	October 2010	• Updated with the latest characteristic data. Added several figures. Added the ADC Typical Operation table.
5	July 2012	In “Supply current characteristics” table, • For S3I_{DD}, the maximum value for the first row at 1μA is changed to 1.3 μA and the typical value 0.65 μA is changed to 0.75μA. • For parameter 3, changed “LPS” to “LPR”, “FBILP” to "FBI" and “FBELP” to “FBE”. • For parameter 4, changed “LPS” to “LPR”, and “FBELP” to “BLPE” in both instances.