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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	65
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x16b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51mm256vll

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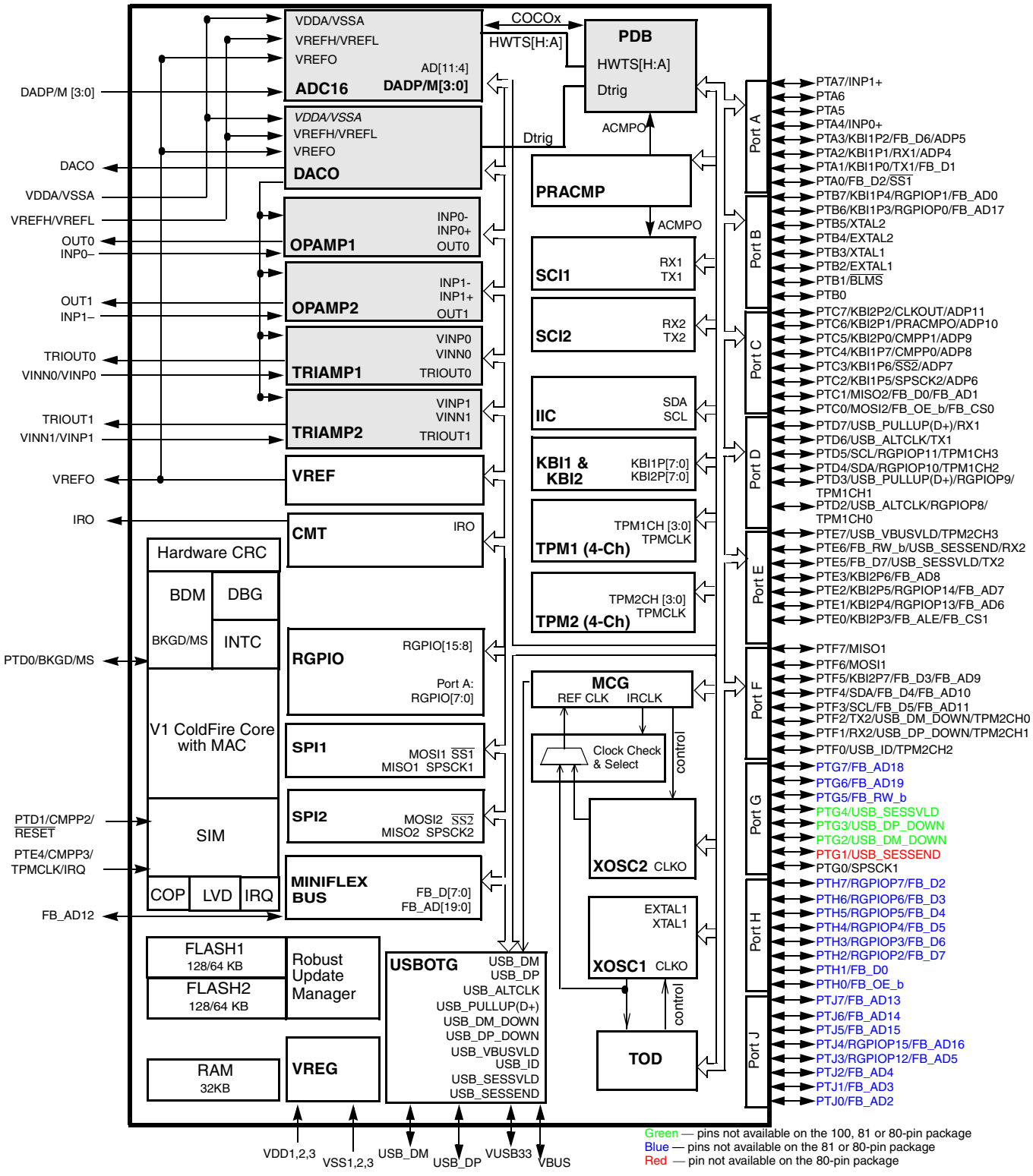

Figure 1. MCF51MM256 Series Block Diagram

2 Pinouts and Pin Assignments

2.1 104-Pin MAPBGA

The following figure shows the 104-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTF6	PTF7	USB_DP	USB_DM	VUSB33	PTF4	PTF3	FB_AD12	PTJ7	PTJ5	PTJ4	A
B	PTG0	PTA0	PTG3	VBUS	PTF5	PTJ6	PTH0	PTE5	PTF0	PTF1	PTF2	B
C	IRO	PTG4	PTA6	PTG2	PTG6	PTG5	PTG7	PTH1	PTE4	PTE6	PTE7	C
D	PTA5	PTA4	PTB1	VDD1		VDD2		VDD3	PTA1	PTE3	PTE2	D
E	VSSA	PTA7	PTB0						PTA2	PTJ3	PTE1	E
F	VREFL	INP1-	INP2-	PTG1				PTC7	PTJ2	PTJ0	PTJ1	F
G	TRIOUT1	OUT1	OUT2						PTD5	PTD7	PTE0	G
H	VINP1	VINN1	PTA3	VSS1		VSS2		VSS3	PTD4	PTD3	PTD2	H
J	DADP0	DADM0	PTH7	PTH6	PTH4	PTH3	PTH2	PTD6	PTC2	PTC0	PTC1	J
K	VINP2	VINN2	DADP1	PTH5	PTB6	PTB7	PTC3	PTD1	PTC4	PTC5	PTC6	K
L	TRIOUT2	DACO	DADM1	VREFO	VREFH	VDDA	PTB3	PTB2	PTD0	PTB5	PTB4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. 104-Pin MAPBGA

2.2 100-Pin LQFP

The following figure shows the 100-pin LQFP pinout configuration.

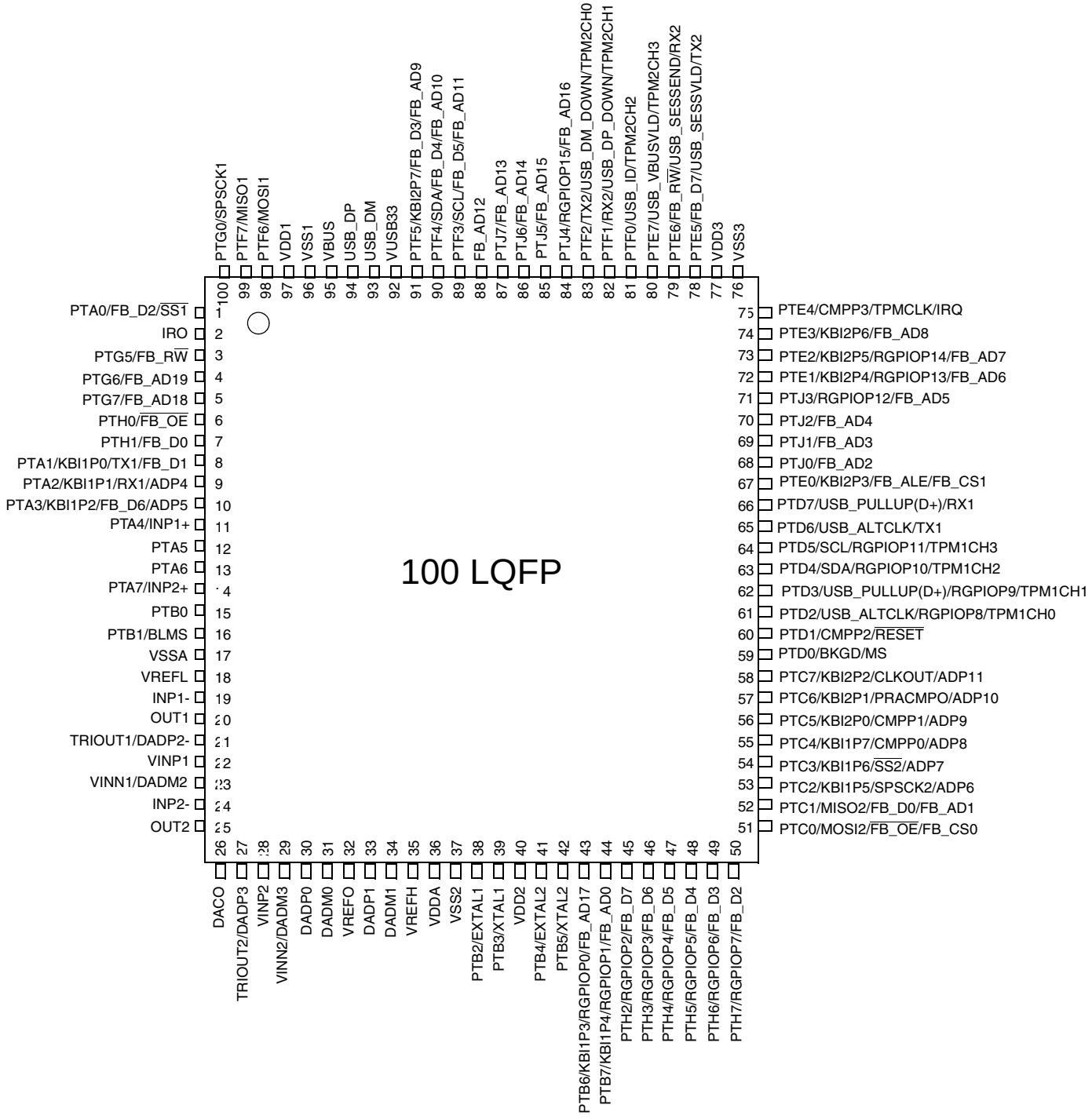

Figure 3. 100-Pin LQFP

2.3 81-Pin MAPBGA

The following figure shows the 81-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	
A	IRO	PTG0	PTF6	USB_DP	VBUS	VUSB33	PTF4	PTF3	PTE4	**A**
B	PTF7	PTA0	PTG1	USB_DM	PTF5	PTE7	PTF1	PTF0	PTE3	**B**
C	PTA4	PTA5	PTA6	PTA1	PTF2	PTE6	PTE5	PTE2	PTE1	**C**
D	INP1-	PTA7	PTB0	PTB1	PTA2	PTA3	PTD5	PTD7	PTE0	**D**
E	OUT1	VINN1	OUT2	VDD2	VDD3	VDD1	PTD2	PTD3	PTD6	**E**
F	VINP1	TRIOUT1	INP2-	VSS2	VSS3	VSS1	PTB7	PTC7	PTD4	**F**
G	DADP0	DACO	TRIOUT2	VINN2	VREFO	PTB6	PTC0	PTC1	PTC2	**G**
H	DADM0	DADM1	DADP1	VINP2	PTC3	PTC4	PTD0	PTC5	PTC6	**H**
J	VSSA	VREFL	VREFH	VDDA	PTB2	PTB3	PTD1	PTB4	PTB5	**J**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	

Figure 4. 81-Pin MAPBGA

2.5 Pin Assignments

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
B2	1	B2	1	PTA0	FB_D2	$\overline{SS1}$	—	PTA0/FB_D2/$\overline{SS1}$
C1	2	A1	2	IRO	—	—	—	IRO
C6	3	—	—	PTG5	FB_$\overline{RW}$	—	—	PTG5/FB_$\overline{RW}$
C5	4	—	—	PTG6	FB_AD19	—	—	PTG6/FB_AD19
C7	5	—	—	PTG7	FB_AD18	—	—	PTG7/FB_AD18
B7	6	—	—	PTH0	$\overline{FB\_OE}$	—	—	PTH0/$\overline{FB\_OE}$
C8	7	—	—	PTH1	FB_D0	—	—	PTH1/FB_D0
D9	8	C4	3	PTA1	KBI1P0	TX1	FB_D1	PTA1/KBI1P0/TX1/FB_D1
E9	9	D5	4	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
H3	10	D6	5	PTA3	KBI1P2	FB_D6	ADP5	PTA3/KBI1P2/FB_D6/ADP5
D2	11	C1	6	PTA4	INP1+	—	—	PTA4/INP1+
D1	12	C2	7	PTA5	—	—	—	PTA5
C3	13	C3	8	PTA6	—	—	—	PTA6
E2	14	D2	9	PTA7	INP2+	—	—	PTA7/INP2+
E3	15	D3	10	PTB0	—	—	—	PTB0
D3	16	D4	11	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
E1	17	J1	12	VSSA	—	—	—	VSSA
F1	18	J2	13	VREFL	—	—	—	VREFL
F2	19	D1	14	INP1-	—	—	—	INP1-
G2	20	E1	15	OUT1	—	—	—	OUT1
G1	21	F2	16	DADP2	TRIOUT1	—	—	DADP2/TRIOUT1
H1	22	F1	17	VINP1	—	—	—	VINP1
H2	23	E2	18	DADM2	VINN1	—	—	DADM2/VINN1
F3	24	F3	19	INP2-	—	—	—	INP2-
G3	25	E3	20	OUT2	—	—	—	OUT2
L2	26	G2	21	DACO	—	—	—	DACO
L1	27	G3	22	DADP3	TRIOUT2	—	—	DADP3/TRIOUT2
K1	28	H4	23	VINP2	—	—	—	VINP2
K2	29	G4	24	DADM3	VINN2	—	—	DADM3/VINN2

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
J1	30	G1	25	DADP0	—	—	—	DADP0
J2	31	H1	26	DADM0	—	—	—	DADM0
L4	32	G5	27	VREFO	—	—	—	VREFO
K3	33	H3	28	DADP1	—	—	—	DADP1
L3	34	H2	29	DADM1	—	—	—	DADM1
L5	35	J3	30	VREFH	—	—	—	VREFH
L6	36	J4	31	VDDA	—	—	—	VDDA
H6	37	F4	32	VSS2	—	—	—	VSS2
L8	38	J5	33	PTB2	EXTAL1	—	—	PTB2/EXTAL1
L7	39	J6	34	PTB3	XTAL1	—	—	PTB3/XTAL1
D6	40	E4	35	VDD2	—	—	—	VDD2
L11	41	J8	36	PTB4	EXTAL2	—	—	PTB4/EXTAL2
L10	42	J9	37	PTB5	XTAL2	—	—	PTB5/XTAL2
K5	43	G6	38	PTB6	KBI1P3	RGPIOP0	FB_AD17	PTB6/KBI1P3/RGPIOP0/FB_AD17
K6	44	F7	39	PTB7	KBI1P4	RGPIOP1	FB_AD0	PTB7/KBI1P4/RGPIOP1/FB_AD0
J7	45	—	—	PTH2	RGPIOP2	FB_D7	—	PTH2/RGPIOP2/FB_D7
J6	46	—	—	PTH3	RGPIOP3	FB_D6	—	PTH3/RGPIOP3/FB_D6
J5	47	—	—	PTH4	RGPIOP4	FB_D5	—	PTH4/RGPIOP4/FB_D5
K4	48	—	—	PTH5	RGPIOP5	FB_D4	—	PTH5/RGPIOP5/FB_D4
J4	49	—	—	PTH6	RGPIOP6	FB_D3	—	PTH6/RGPIOP6/FB_D3
J3	50	—	—	PTH7	RGPIOP7	FB_D2	—	PTH7/RGPIOP7/FB_D2
J10	51	G7	40	PTC0	MOSI2	$\overline{\text{FB\_OE}}$	FB_CS0	PTC0/MOSI2/$\overline{\text{FB\_OE}}$/FB_CS0
J11	52	G8	41	PTC1	MISO2	FB_D0	FB_AD1	PTC1/MISO2/FB_D0/FB_AD1
J9	53	G9	42	PTC2	KBI1P5	SPSCK2	ADP6	PTC2/KBI1P5/SPSCK2/ADP6
K7	54	H5	43	PTC3	KBI1P6	$\overline{\text{SS2}}$	ADP7	PTC3/KBI1P6/$\overline{\text{SS2}}$/ADP7
K9	55	H6	44	PTC4	KBI1P7	CMPP0	ADP8	PTC4/KBI1P7/CMPP0/ADP8
K10	56	H8	45	PTC5	KBI2P0	CMPP1	ADP9	PTC5/KBI2P0/CMPP1/ADP9
K11	57	H9	46	PTC6	KBI2P1	PRACMPO	ADP10	PTC6/KBI2P1/PRACMPO/ADP10
F8	58	F8	47	PTC7	KBI2P2	CLKOUT	ADP11	PTC7/KBI2P2/CLKOUT/ADP11
L9	59	H7	48	PTD0	BKGD	MS	—	PTD0/BKGD/MS
K8	60	J7	49	PTD1	CMPP2	$\overline{\text{RESET}}$	—	PTD1/CMPP2/$\overline{\text{RESET}}$

Table 9. DC Characteristics (continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
20	V_{LVWH}	Low-voltage warning threshold — high range[9] V_{DD} falling						
			—	2.36	2.46	2.56	V	P
		V_{DD} rising						
			—	2.36	2.46	2.56	V	P
21	V_{LVWL}	Low-voltage warning threshold — low range[9] V_{DD} falling						
			—	2.11	2.16	2.22	V	P
		V_{DD} rising						
			—	2.16	2.21	2.27	V	P
22	V_{hys}	Low-voltage inhibit reset/recoverhysteresis[10]	—	—	50	—	mV	C
23	V_{BG}	Bandgap Voltage Reference[11]	—	1.110	1.17	1.230	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to V_{DD} or V_{SS} and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 Maximum is highest voltage that POR is guaranteed.

9 Run at 1 MHz bus frequency

10 Low voltage detection and warning limits measured at 1 MHz bus frequency.

11 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

3.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
1	RI_{DD}	Run supply current FEI mode; all modules ON[2]							
			25.165 MHz	3	44	48	mA	–40 to 25	P
			25.165 MHz	3	44	48	mA	105	P
			20 MHz	3	32.3	—	mA	–40 to 105	T
			8 MHz	3	16.4	—	mA	–40 to 105	T
			1 MHz	3	2.9	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode; all modules OFF[3]							
			25.165 MHz	3	29	29.6	mA	–40 to 105	C
			20 MHz	3	25.4	—	mA	–40 to 105	T
			8 MHz	3	12.7	—	mA	–40 to 105	T
			1 MHz	3	2.4	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPR=0; all modules OFF[3]							
			16 kHz FBI	3	232	280	µA	–40 to 105	T
			16 kHz FBE	3	231	296	µA	–40 to 105	T
4	RI_{DD}	Run supply current LPR=1, all modules OFF[3]							
			16 kHz BLPE	3	74	75	µA	0 to 70	T
			16 kHz BLPE	3	74	120	µA	–40 to 105	T

Table 10. Supply Current Characteristics (continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	16.5	—	mA	–40 to 105	C
			20 MHz	3	10.3	—	mA	–40 to 105	T
			8 MHz	3	6.6	—	mA	–40 to 105	T
			1 MHz	3	1.7	—	mA	–40 to 105	T
6	$LPWI_{DD}$	Low-Power Wait mode supply current							
			16 KHz	3	28	62	µA	–40 to 105	T
7	$S2I_{DD}$	Stop2 mode supply current[4]							
			N/A	3	0.410	1.00	µA	–40 to 25	P
			N/A	3	3.7	10	µA	70	C
			N/A	3	10	20	µA	85	C
			N/A	3	21	31.5	µA	105	P
			N/A	2	0.410	0.640	µA	–40 to 25	C
			N/A	2	3.4	9	µA	70	C
			N/A	2	9.5	18	µA	85	C
			N/A	2	20	30	µA	105	C

3.7 PRACMP Electricals

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V_{PWR}	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	80	μA	D
3	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	μA	D
4	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA	D
5	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V	D
6	Analog input offset voltage	VAIO	—	5	40	mV	D
7	Analog comparator hysteresis	V_H	3.0	—	20.0	mV	D
8	Analog input leakage current	I_{ALKG}	—	—	1	nA	D
9	Analog comparator initialization delay	tAINIT	—	—	1.0	μs	D
10	Programmable reference generator inputs	V_{In2} (V_{DD25})	1.8	—	2.75	V	D
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	μs	D
12	Programmable reference generator step size	Vstep	0.75	1	1.25	LSB	D
13	Programmable reference generator voltage range	Vprgout	V_{In}/32	—	V_{in}	V	P

3.8 12-Bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	V_{DDA}	1.8	3.6	V	P	
2	Reference voltage	V_{DACR}	1.15	3.6	V	C	
3	Temperature	T_A	–40	105	°C	C	
4	Output load capacitance	C_L	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	I_L	—	1	mA	C	

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Min	Typ	Max	Unit	C	Notes
1	Resolution	N	12	—	12	bit	T	

Table 15. 16-Bit ADC Operating Conditions (continued)

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
5	V_{REFL}	Ref Voltage Low		V_{SSA}	V_{SSA}	V_{SSA}	V	D	
6	V_{ADIN}	Input Voltage		V_{REFL}	—	V_{REFH}	V	D	
7	C_{ADIN}	Input Capacitance	16-bit modes 8/10/12-bit modes	—	8 4	10 5	pF	T	
8	R_{ADIN}	Input Resistance		—	2	5	kΩ	T	
9	R_{AS}	Analog Source Resistance							External to MCU Assumes ADLSMP=0
		16-bit mode	f_{ADCK} > 8 MHz	—	—	0.5	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	1	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	2	kΩ	T	
		13/12-bit mode	f_{ADCK} > 8 MHz	—	—	1	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	2	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	5	kΩ	T	
		11/10-bit mode	f_{ADCK} > 8 MHz	—	—	2	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	10	kΩ	T	
		9/8-bit mode	f_{ADCK} > 8 MHz	—	—	5	kΩ	T	
			f_{ADCK} < 8 MHz	—	—	10	kΩ	T	
10	f_{ADCK}	ADC Conversion Clock Frequency							
		ADLPC=0, ADHSC=1		1.0	—	8.0	MHz	D	
		ADLPC=0, ADHSC=0		1.0	—	5.0	MHz	D	
		ADLPC=1, ADHSC=0		1.0	—	2.5	MHz	D	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

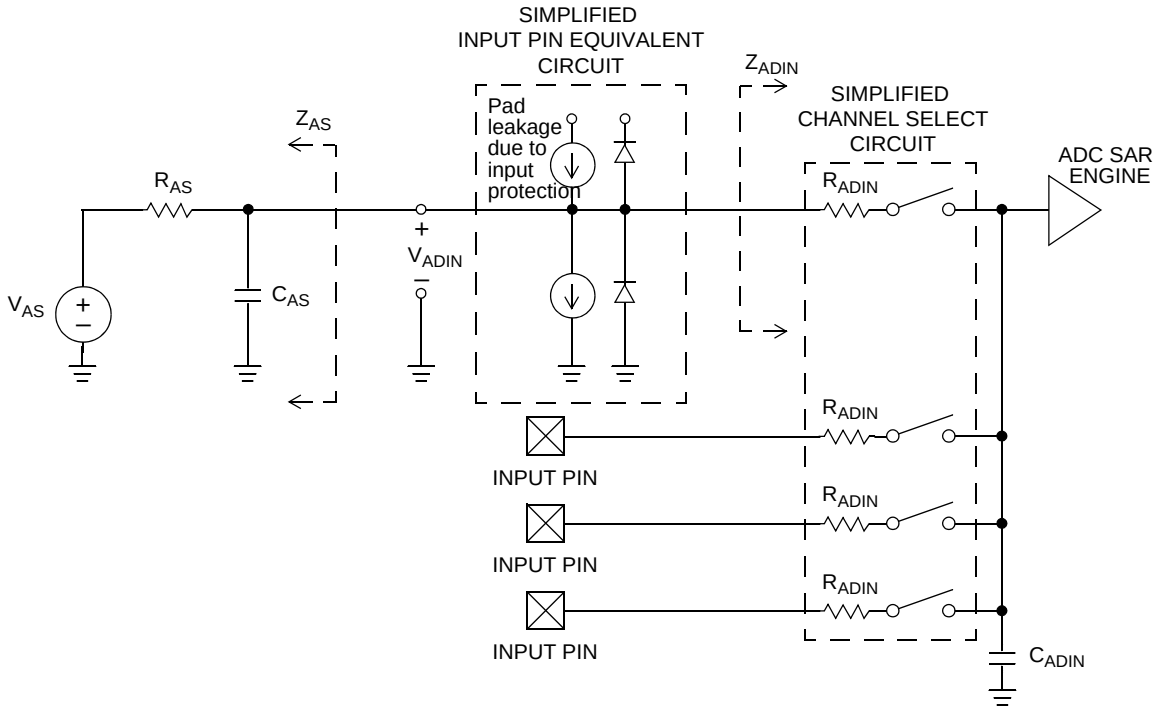

Figure 8. ADC Input Impedance Equivalency Diagram

Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq$ 8 MHz, –40 to 85 °C) (continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
14	Total Harmonic Distortion	16-bit differential mode Avg=32	THD	—	–91.5	–74.3	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	–85.5	—		D	
15	Spurious Free Dynamic Range	16-bit differential mode Avg=32	SFDR	75.0	92.2	—	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	86.2	—		D	
16	Input Leakage Error	all modes	E_{IL}	$I_{In} * R_{AS}$			mV	D	I_{In} = leakage current (refer to DC characteristics)
17	Temp Sensor Slope	–40°C – 25°C	m	—	1.646	—	mV/×C	C	
		25°C – 125°C		—	1.769	—			
18	Temp Sensor Voltage	25°C	V_{TEMP25}	—	718.2	—	mV	C	

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}$

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, $f_{ADACK} \leq 4$ MHz, ADHSC = 1)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+24/ –24 +32/–20	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.0 ±1.25		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
2	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
3	Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	
4	Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-8	LSB[2]	T	$V_{ADIN} = V_{SSA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, $f_{ADACK} \leq 4$ MHz, ADHSC = 1) (continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
5	Full-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	T	$V_{ADIN} = V_{DDA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
6	Quantization Error	16-bit modes	E_Q	—	–1 to 0	—	LSB[2]	D	
		≤13-bit modes		—	—	±0.5			
7	Effective Number of Bits	16-bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	ENOB	 14.3 13.8 13.4 13.1 12.4	 14.5 14.0 13.7 13.4 12.6	 — — — — —	Bits	C	$F_{in} = F_{sample}/100$
8	Signal to Noise plus Distortion	See ENOB	SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB		
9	Total Harmonic Distortion	16-bit differential mode Avg=32	THD	—	–95.8	–90.4	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
10	Spurious Free Dynamic Range	16-bit differential mode Avg=32	SFDR	91.0	96.5	—	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
11	Input Leakage Error	all modes	E_{IL}	$I_{In} * R_{AS}$			mV	D	I_{In} = leakage current (refer to DC characteristics)

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}$

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 625 ns represents 5 time quanta for CAN applications, under worst-case conditions of 8 MHz CAN bus clock, 1 Mbps CAN Bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

6 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

7 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

Table 19. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit	C
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz	D
		• High range (RANGE = 1), • FEE or FBE mode [2]	f_{hi-fll}	1	—	5	MHz	D
		• High range (RANGE = 1), • PEE or PBE mode [3]	f_{hi-pll}	1	—	16	MHz	D
		• High range (RANGE = 1), • High gain (HGO = 1), • BLPE mode	f_{hi-hgo}	1	—	16	MHz	D
		• High range (RANGE = 1), • Low power (HGO = 0), • BLPE mode	f_{hi-lp}	1	—	8	MHz	D
2	Load capacitors		C_1 C_2	See crystal or resonator manufacturer's recommendation.				D
3	Feedback resistor	• Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ	D
		• High range (1 MHz to 16 MHz)	—	—	1	—		D
4	Series resistor — Low range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)		—	100	—		D
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)						D
		≥ 8 MHz		—	0	0		D
		4 MHz		—	0	10		D
		1 MHz		—	0	20		D

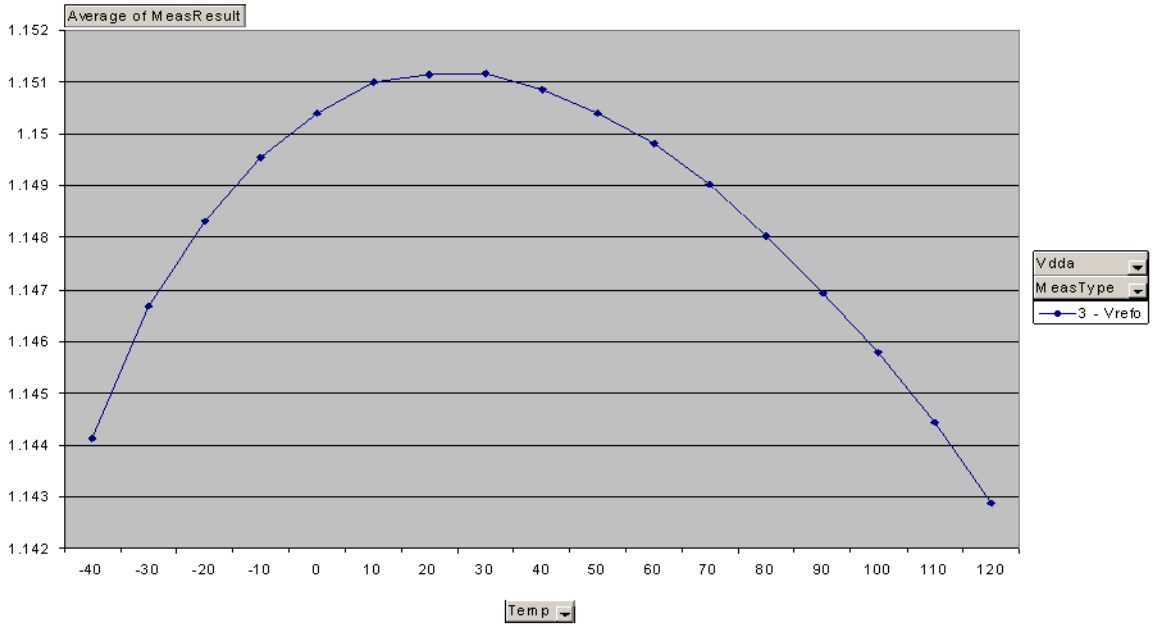

Figure 19. Typical VREF Output vs. Temperature

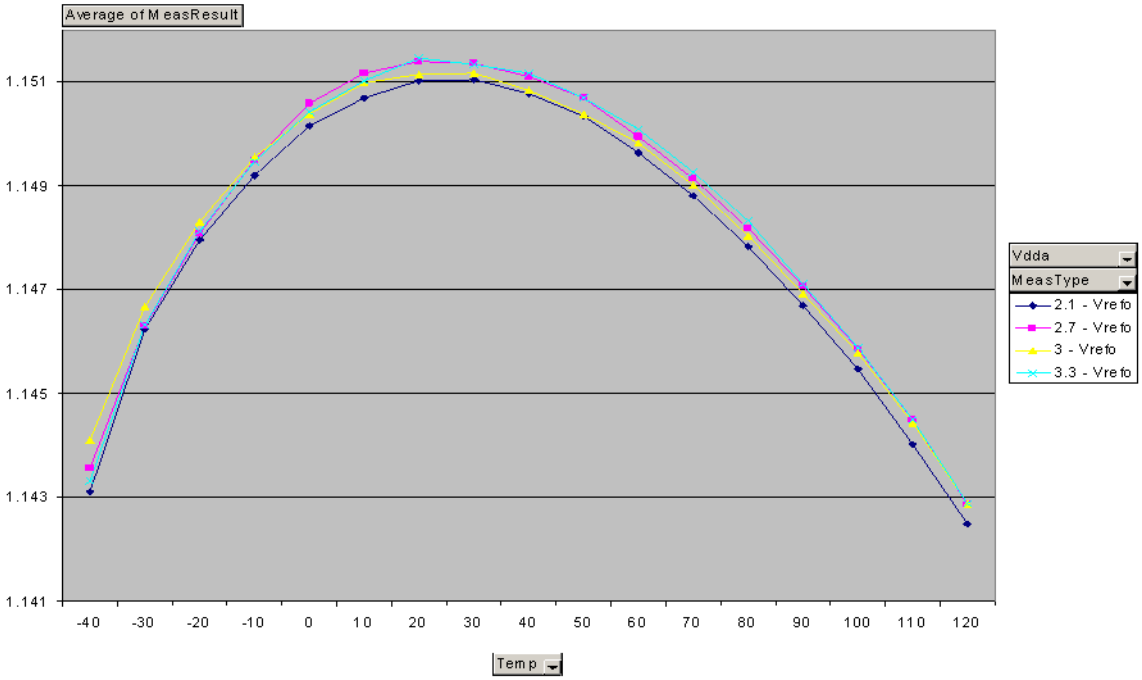

Figure 20. Typical VREF Output vs. V_{DD}

Table 29. OPAMP Characteristics 1.8–3.6 V (continued)

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
27	Output Impedance AC Open Loop (@100 kHz High-Speed mode)	R_{OUT}	—	220	—	Ω	D
28	Output Voltage Range	V_{OUT}	0.15	—	V_{DD}–0.15	V	T
29	Output Drive Capability	I_{OUT}	±0.5	±1.0	—	mA	T
30	Gain Margin	GM	20	—	—	dB	D
31	Phase Margin	PM	45	55	—	deg	T
32	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	4	—	uS	T
33	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	1	—	uS	T
34	Input Voltage Noise Density	f=1 kHz	—	250	—	nV/√Hz	T

1 All parameters are measured at 3.3 V, CL =4 7 pF across temperature –40 to + 105°C unless specified.
2 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

4 Ordering Information

This section contains ordering information for the device numbering system. See Table 1 for feature summary by package information.

4.1 Part Numbers

Table 30. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51MM256VML	MCF51MM256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 105 °C
MCF51MM256VLL	MCF51MM256 ColdFire Microcontroller	256K/32K	100 LQFP	–40 to 105 °C
MCF51MM256VMB	MCF51MM256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 105 °C
MCF51MM256VLK	MCF51MM256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 105 °C
MCF51MM128VMB	MCF51MM128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 105 °C
MCF51MM128VLK	MCF51MM128 ColdFire Microcontroller	128K/32K	80 LQFP	–40 to 105 °C

4.2 Package Information

Table 31. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
100	Low Quad Flat Package	LQFP	LL	983-03	98ASS23308W
80	Low Quad Flat Package	LQFP	LK	1418	98ASS23174W
104	MAP BGA Package	MAPBGA	ML	1285-02	98ARH98267A
81	MAP BGA Package	MAPBGA	MB	1662-01	98ASA10670D

4.3 Mechanical Drawings

Table 31 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51MM256/128 Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 31, or
- Open a browser to the Freescale website (http://www.freescale.com), and enter the appropriate document number (from Table 31) in the “Enter Keyword” search box at the top of the page.

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