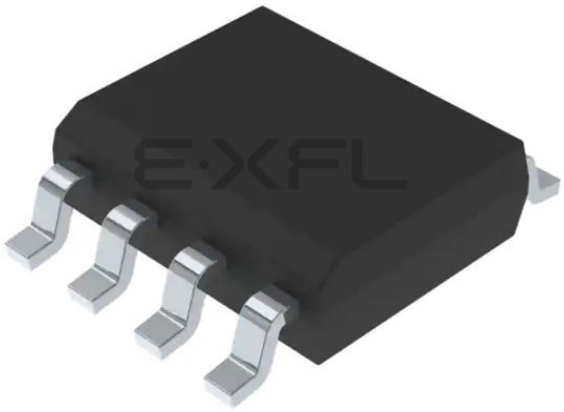

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fliteus2m3

Contents

Table 3. Hardware register map (continued)(1)

Address	Block	Register label	Register name	Reset status	Remarks
0049h 004Ah	AWU	AWUPR AWUCSR	AWU Prescaler register AWU Control/Status register	FFh 00h	R/W R/W
004Bh 004Ch 004Dh 004Eh 004Fh 0050h	DM(4)	DMCR DMSR DMBK1H DMBK1L DMBK2H DMBK2L	DM Control register DM Status register DM Breakpoint register 1 High DM Breakpoint register 1 Low DM Breakpoint register 2 High DM Breakpoint register 2 Low	00h 00h 00h 00h 00h 00h	R/W R/W R/W R/W R/W R/W
0051h to 007Fh	Reserved area (47 bytes)				

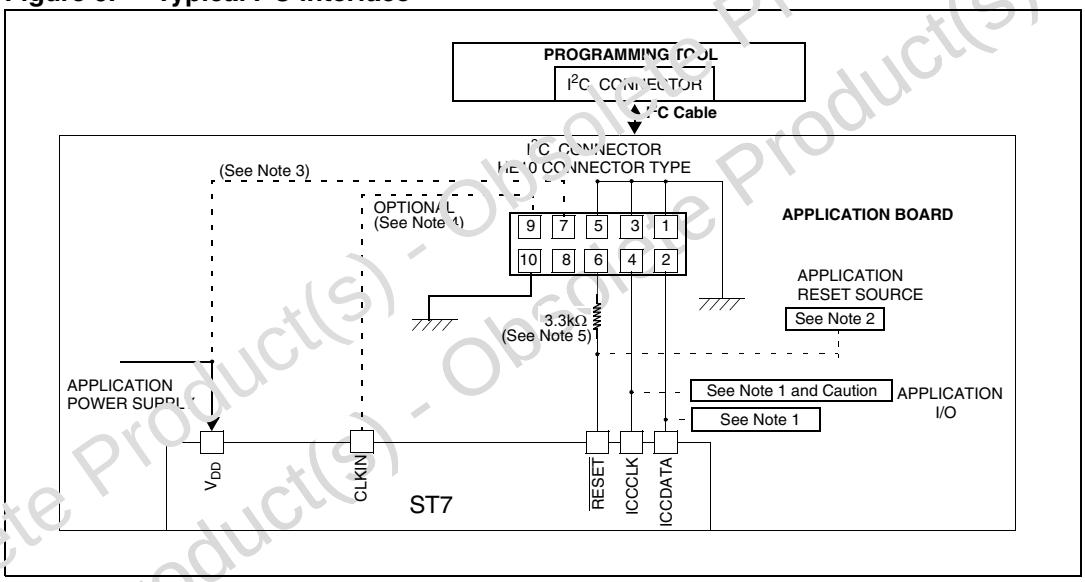
1. Legend: x=undefined, R/W=read/write
2. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.
3. The bits associated with unavailable pins must always keep their reset value.
4. For a description of the DM registers, see the ST7 I^2C Protocol Reference Manual.

Pin 9 has to be connected to the CLKIN pin of the ST7 when I^2C mode is selected with option bytes disabled (35-pulse I^2C entry mode). When option bytes are enabled (38-pulse I^2C entry mode), the internal RC clock (internal RC or AWU RC) is forced. If internal RC is selected in the option byte, the internal RC is provided. If AWU RC or external clock is selected, the AWU RC oscillator is provided.

A serial resistor must be connected to I^2C connector pin 6 in order to prevent contention on PA3/$\overline{\text{RESET}}$ pin. Contention may occur if a tool forces a state on $\overline{\text{RESET}}$ pin while PA3 pin forces the opposite state in output mode. The resistor value is defined to limit the current below 2 mA at 5 V. If PA3 is used as output push-pull, then the application must be switched off to allow the tool to take control of the $\overline{\text{RESET}}$ pin (PA3). To allow the programming tool to drive the $\overline{\text{RESET}}$ pin below V_{IL}, special care must also be taken when a pull-up is placed on PA3 for application reasons.

Caution: During normal operation, ICCCLK pin must be pulled- up, internally or externally (external pull-up of 10 kΩ mandatory in noisy environment). This is to avoid entering I^2C mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up.

Figure 6. Typical I^2C interface



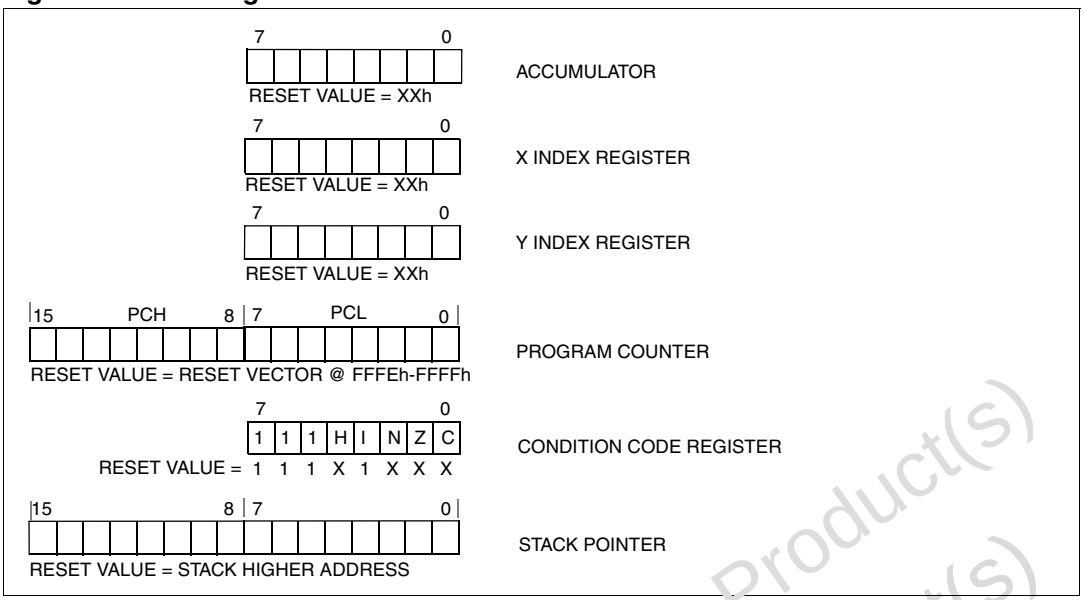
4.5 Memory protection

There are two different types of memory protection: readout protection and Write/Erase Protection which can be applied individually.

4.5.1 Readout protection

Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller. Program memory is protected.

Figure 7. CPU registers



1. X = Undefined value

5.3.4 Condition Code register (CC)

The 8-bit Condition Code register contains the interrupt mask and four flags representative of the result of the instruction just executed. This register can also be handled by the PUSH and POP instructions.

These bits can be individually tested and/or controlled by specific instructions.

Reset value: 111x1xxx

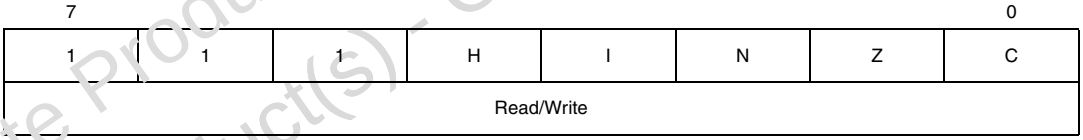
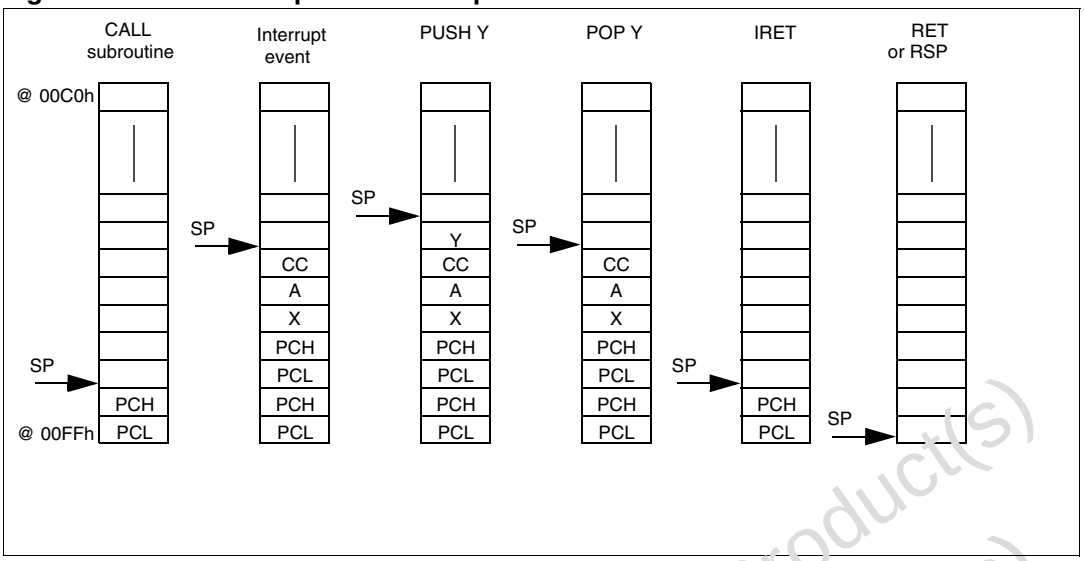


Figure 8. Stack manipulation example



1. Stack higher address = 00FFh.
2. Stack lower address = 00C0h.

Figure 15. Low voltage detector vs reset

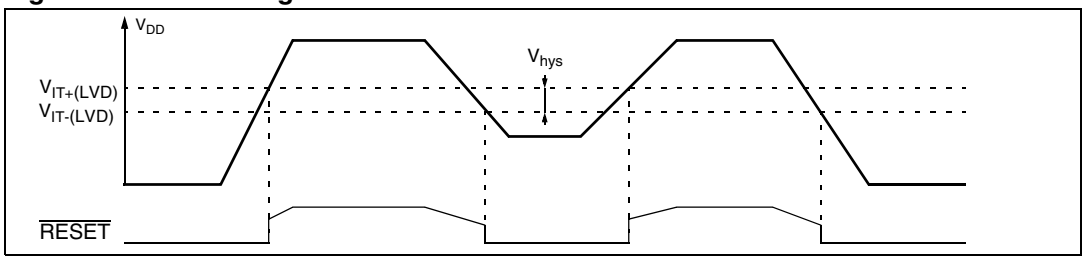


Figure 16. Reset and supply management block diagram

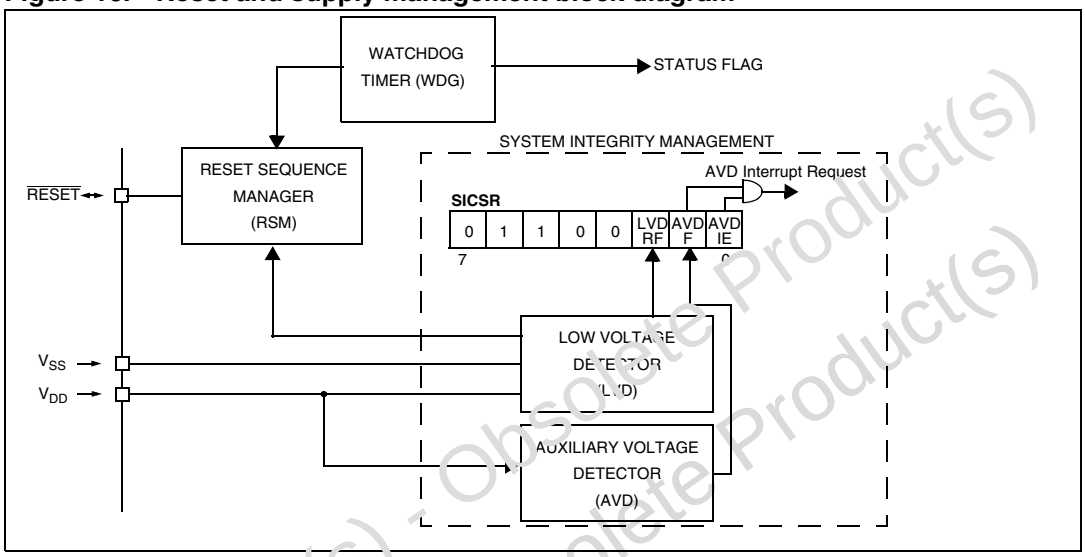
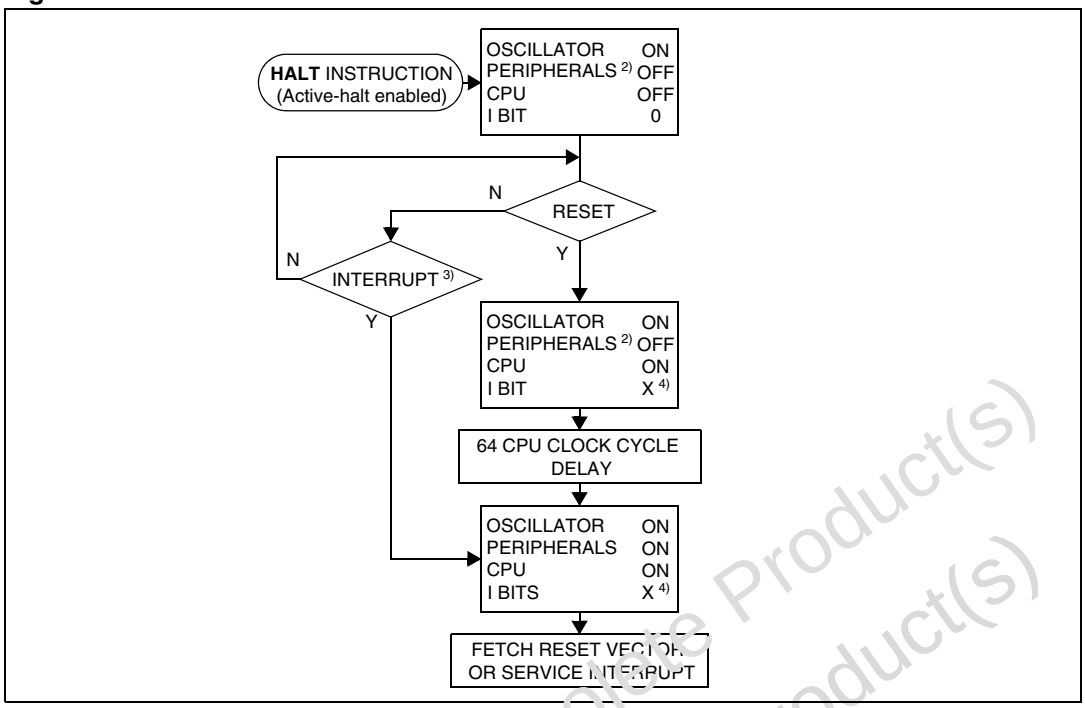


Figure 22. Active-halt mode flowchart



1. This delay occurs only if the MCU exits Active-halt mode by means of a reset.
2. Peripherals clocked with an external clock source can still be active.
3. Only the Lite Timer RTC and AT Timer interrupts can exit the MCU from Active-halt mode.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I bit of the CC register is set during the interrupt routine and cleared when the CC register is popped.

8.4.2 Halt mode

The Halt mode is the lowest power consumption mode of the MCU. It is entered by executing the 'HALT' instruction when Active-halt mode is disabled.

The MCU can exit Halt mode on reception of either a specific interrupt (see *Table 9: Interrupt mapping*) or a reset. When exiting Halt mode by means of a reset or an interrupt, the main oscillator is immediately turned on and the 64 CPU cycle delay is used to stabilize it. After the start up delay, the CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see *Figure 24*).

When entering Halt mode, the I bit in the CC register is forced to 0 to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes immediately.

In Halt mode, the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. All peripherals are not clocked except the ones which get their clock supply from another clock generator (such as an external or auxiliary oscillator).

The compatibility of watchdog operation with Halt mode is configured by the "WDGHALT" option bit of the option byte. The HALT instruction when executed while the watchdog system is enabled, can generate a watchdog reset (see *Section 14.1: Option bytes* for more details).

9.2.3 Alternate functions

When an on-chip peripheral is configured to use a pin, the alternate function is automatically selected. This alternate function takes priority over the standard I/O programming under the following conditions:

- When the signal is coming from an on-chip peripheral, the I/O pin is automatically configured in output mode (push-pull or open drain according to the peripheral).
- When the signal is going to an on-chip peripheral, the I/O pin must be configured in floating input mode. In this case, the pin state is also digitally readable by addressing the DR register.

Note: 1 Input pull-up configuration can cause unexpected value at the input of the alternate peripheral input.

2 When an on-chip peripheral use a pin as input and output, this pin has to be configured in input floating mode.

Figure 28. I/O port general block diagram

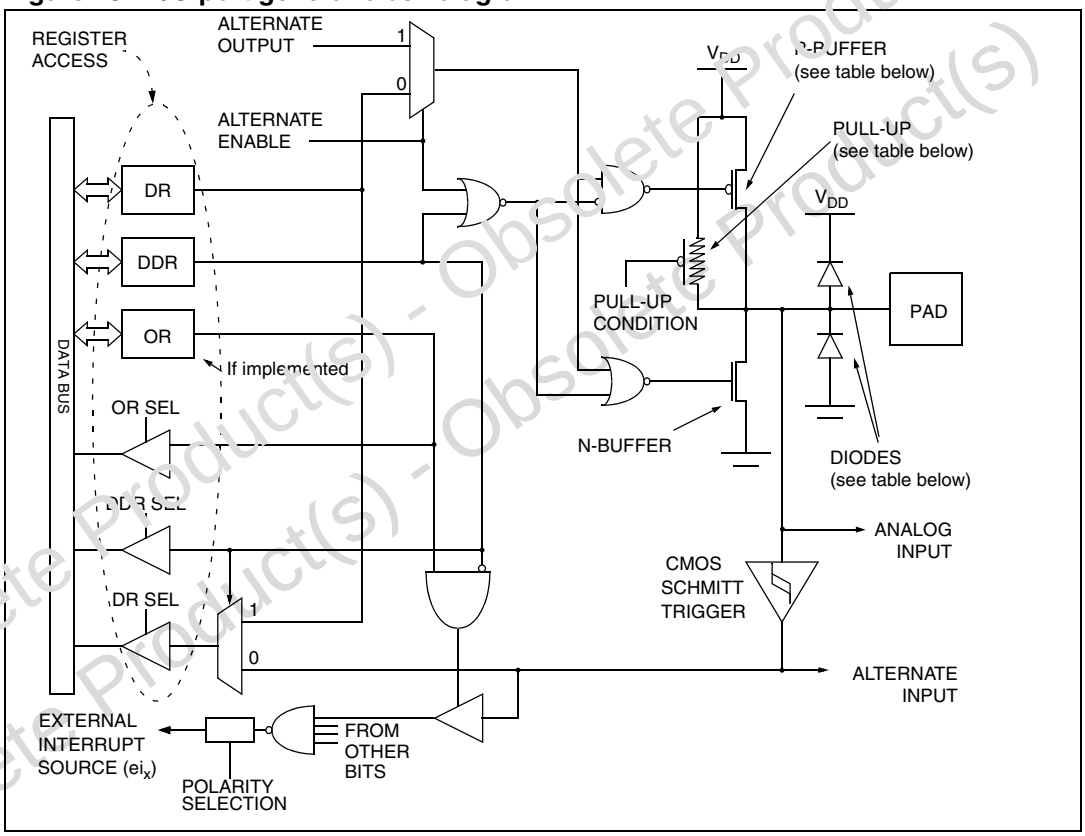
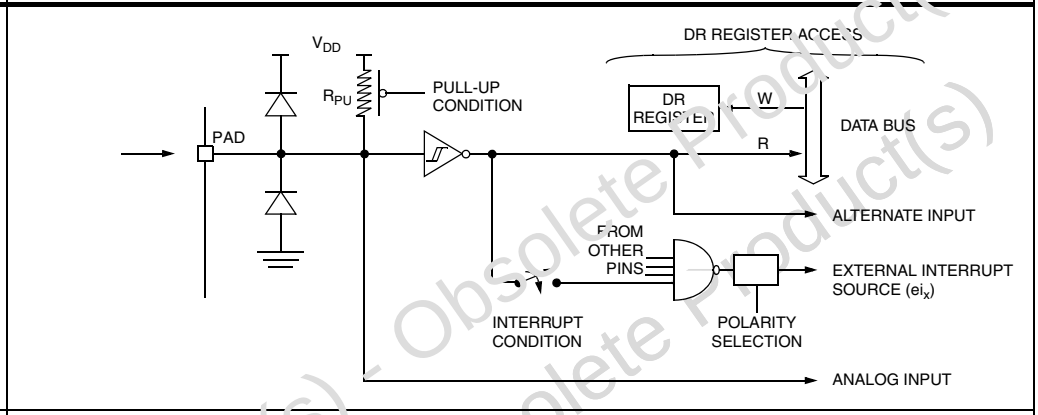
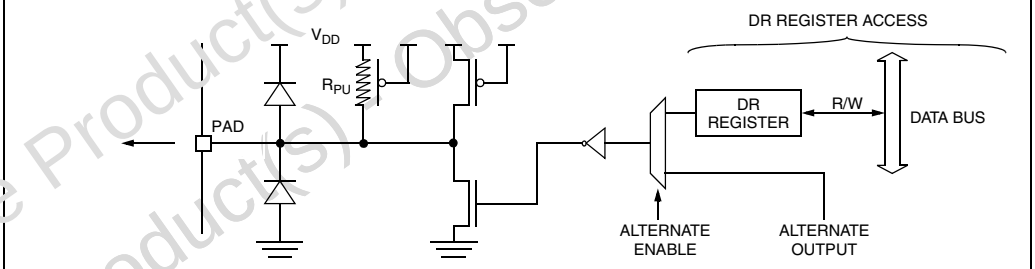
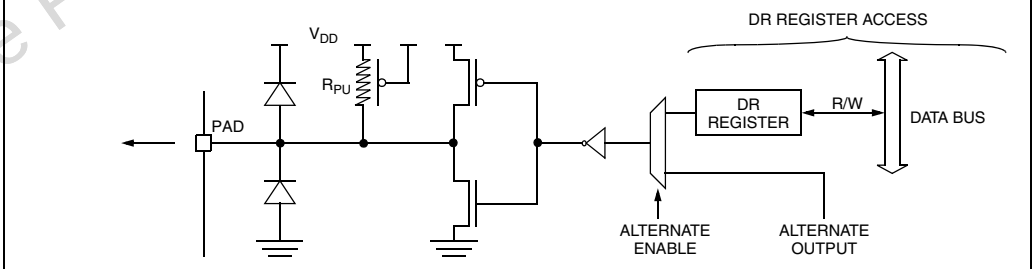


Table 18. I/O port mode options(1)

Configuration mode		Pull-up	P-buffer	Diodes	
				to V_{DD}	to V_{SS}
Input	Floating with/without Interrupt	Off	Off	On	On
	Pull-up with/without Interrupt	On			
Output	Push-pull	Off	On		
	Open Drain (logic level)		Off		

1. NI stands for not implemented; Off for implemented not activated; On for implemented and activated.

Table 19. I/O port configurations

	Hardware configuration
INPUT (1)	
OPEN-DRAIN OUTPUT (2)	
PUSH-PULL OUTPUT (2)	

1. When the I/O port is in input configuration and the associated alternate function is enabled as an output, reading the DR register will read the alternate function output status.
2. When the I/O port is in output configuration and the associated alternate function is enabled as an input, the alternate function reads the pin status given by the DR register content.

Table 36. ST7 addressing mode overview (continued)(1)

Mode			Syntax	Destination/ source	Pointer address	Pointer size	Length (bytes)
Long	Indirect	Indexed	ld A,([$10.w],X)	0000..FFFF	00..FF	word	+ 2
Relative	Direct		jrne loop	PC-128/PC+127[1)]			+ 1
Relative	Indirect		jrne [$10]	PC-128/PC+127[1)]	00..FF	byte	+ 2
Bit	Direct		bset $10,#7	00..FF			+ 1
Bit	Indirect		bset [$10],#7	00..FF	00..FF	byte	+ 2
Bit	Direct	Relative	btjt $10,#7,skip	00..FF			+ 2
Bit	Indirect	Relative	btjt [$10],#7,skip	00..FF	00..FF	byte	+ 3

1. At the time the instruction is executed, the Program Counter (PC) points to the instruction following JRxx.

11.1.1 Inherent mode

All Inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Table 37. Instructions supporting inherent addressing mode

Inherent instruction	Function
NOP	No operation
TRAP	S/W Interrupt
WFI	Wait For Interrupt (low power mode)
HALT	Halt Oscillator (lowest power mode)
RET	Subroutine return
IRET	Interrupt subroutine return
SIM	Set interrupt mask
RIM	Reset interrupt mask
SCF	Set carry flag
RCF	Reset carry flag
RSP	Reset stack pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 complement
MUL	Byte multiplication
SLL, SRL, SRA, RLC, RRC	Shift and rotate operations
SWAP	Swap nibbles

11.1.5 Indirect modes (short, long)

The required data byte to do the operation is found by its memory address, located in memory (pointer).

The pointer address follows the opcode. The indirect addressing mode consists of two submodes:

Indirect mode (short)

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - FF addressing space, and requires 1 byte after the opcode.

Indirect mode (long)

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

11.1.6 Indirect indexed modes (short, long)

This is a combination of indirect and short indexed addressing modes. The operand is referenced by its memory address, which is defined by the unsigned addition of an index register value (X or Y) with a pointer value located in memory. The pointer address follows the opcode.

The indirect indexed addressing mode consists of two submodes:

Indirect indexed mode (short)

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - 1FE addressing space, and requires 1 byte after the opcode.

Indirect indexed mode (long)

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

Table 30. Instructions supporting direct, indexed, indirect and indirect indexed addressing modes

Instructions	Function
Long and short instructions	
LD	Load
CP	Compare
AND, OR, XOR	Logical operations
ADC, ADD, SUB, SBC	Arithmetic addition/subtraction operations
BCP	Bit compare
Short instructions only	
CLR	Clear
INC, DEC	Increment/decrement
TNZ	Test negative or zero

Table 42. Illegal opcode detection (continued)

Mnemo	Description	Function/example	Dst	Src	H	I	N	Z	C
BRES	Bit Reset	bres Byte, #3	M	-	-	-	-	-	-
BSET	Bit Set	bset Byte, #3	M	-	-	-	-	-	-
BTJF	Jump if bit is false (0)	btjf Byte, #3, Jmp1	M	-	-	-	-	-	C
BTJT	Jump if bit is true (1)	btjt Byte, #3, Jmp1	M	-	-	-	-	-	C
CALL	Call subroutine		-	-	-	-	-	-	-
CALLR	Call subroutine relative		-	-	-	-	-	-	-
CLR	Clear		reg, M	-	-	-	0	1	-
CP	Arithmetic compare	tst(Reg - M)	reg	M	-	-	N	Z	C
CPL	One Complement	A = FFH-A	reg, M	-	-	-	N	Z	1
DEC	Decrement	dec Y	reg, M	-	-	-	N	Z	-
HALT	Halt		-	-	-	0	-	-	-
IRET	Interrupt routine return	Pop CC, A, X, PC	-	-	H	I	N	Z	C
INC	Increment	inc X	reg, M	-	-	-	N	Z	-
JP	Absolute jump	jp [TBL.w]	-	-	-	-	-	-	-
JRA	Jump relative always		-	-	-	-	-	-	-
JRT	Jump relative		-	-	-	-	-	-	-
JRF	Never jump	jrf *	-	-	-	-	-	-	-
JRIH	Jump if ext. interrupt = 1		-	-	-	-	-	-	-
JRIL	Jump if ext. interrupt = 0		-	-	-	-	-	-	-
JRH	Jump if H = 1	H = 1 ?	-	-	-	-	-	-	-
JRNH	Jump if H = 0	H = 0 ?	-	-	-	-	-	-	-
JRM	Jump if I = 1	I = 1 ?	-	-	-	-	-	-	-
JRNM	Jump if I = 0	I = 0 ?	-	-	-	-	-	-	-
JRMI	Jump if N = 1 (minus)	N = 1 ?	-	-	-	-	-	-	-
JRPL	Jump if N = 0 (plus)	N = 0 ?	-	-	-	-	-	-	-
JREQ	Jump if Z = 1 (equal)	Z = 1 ?	-	-	-	-	-	-	-
JRNE	Jump if Z = 0 (not equal)	Z = 0 ?	-	-	-	-	-	-	-
JRC	Jump if C = 1	C = 1 ?	-	-	-	-	-	-	-
JRNC	Jump if C = 0	C = 0 ?	-	-	-	-	-	-	-
JRULT	Jump if C = 1	Unsigned <	-	-	-	-	-	-	-
JRUGE	Jump if C = 0	Jmp if unsigned ≥	-	-	-	-	-	-	-
JRUGT	Jump if (C + Z = 0)	Unsigned >	-	-	-	-	-	-	-
JRULE	Jump if (C + Z = 1)	Unsigned ≤	-	-	-	-	-	-	-
LD	Load	dst ≤ src	reg, M	M, reg	-	-	N	Z	-
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A	0	-	-	-	0

12 Electrical characteristics

12.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

12.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25 °C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean+3Σ).

12.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25 °C, V_{DD}=5 V (for the 4.5 V≤V_{DD}≤5.5 V voltage range), V_{DD}=3.75 V (for the 3 V≤V_{DD}≤4.5 V voltage range) and V_{DD}=2.7 V (for the 2.4 V≤V_{DD}≤3 V voltage range). They are given only as design guidelines and are not tested.

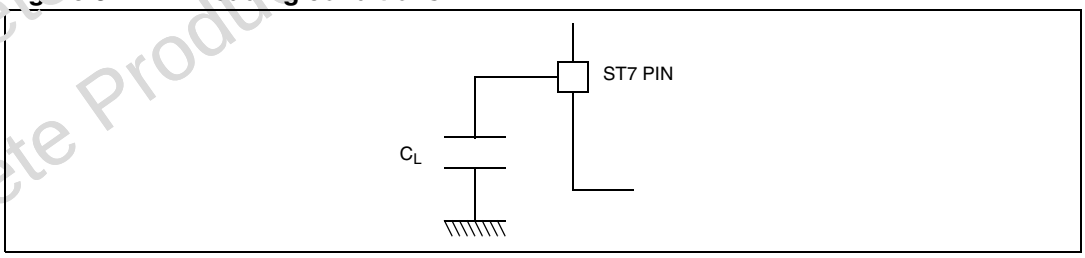
12.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

12.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 37*.

Figure 37. Pin loading conditions



12.3.3 Auxiliary voltage detector (AVD) thresholds

T_A = –40 to 125°C, unless otherwise specified.

Table 48. Operating characteristics with AVD(1)

Symbol	Parameter	Conditions	Min (2)	Typ (2)	Max (2)	Unit
$V_{IT+(AVD)}$	1 => 0 AVDF flag toggle threshold (V_{DD} rise)	High threshold Med. threshold Low threshold	4.0 3.4 2.6	4.4 3.7 2.9	4.8 4.1 3.2	V
$V_{IT-(AVD)}$	0 => 1 AVDF flag toggle threshold (V_{DD} fall)	High threshold Med. threshold Low threshold	3.9 3.3 2.5	4.3 3.6 2.8	4.7 4.0 3.1	
V_{hys}	AVD voltage threshold hysteresis	$V_{IT+(AVD)}$-$V_{IT-(AVD)}$		150		mV

1. Refer to *Section : Monitoring the VDD main supply*.
2. Not tested in production, guaranteed by characterization.

Table 49. Voltage drop between AVD flag set and LVD reset generation

Parameter	Min (1)	Typ (1)	Max (1)	Unit
AVD med. threshold - AVD low. threshold	800	850	950	mV
AVD high. threshold - AVD low threshold	1400	1450	1550	
AVD high. threshold - AVD med. threshold	600	650	750	
AVD low threshold - LVD low threshold	100	200	250	
AVD med. threshold - LVD low threshold	950	1050	1150	
AVD med. threshold - LVD med. threshold	250	300	400	
AVD high. threshold - LVD low threshold	1600	1700	1800	
AVD high. threshold - LVD med. threshold	900	1000	1050	

1. Not tested in production, guaranteed by characterization.

12.3.4 Internal RC oscillator

To improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100 nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

Internal RC oscillator calibrated at 5.0 V

The ST7 internal clock can be supplied by an internal RC oscillator (selectable by option byte).

Figure 40. Typical accuracy with RCCR=RCCR0 vs V_{DD}= 2.4-6.0 V and temperature

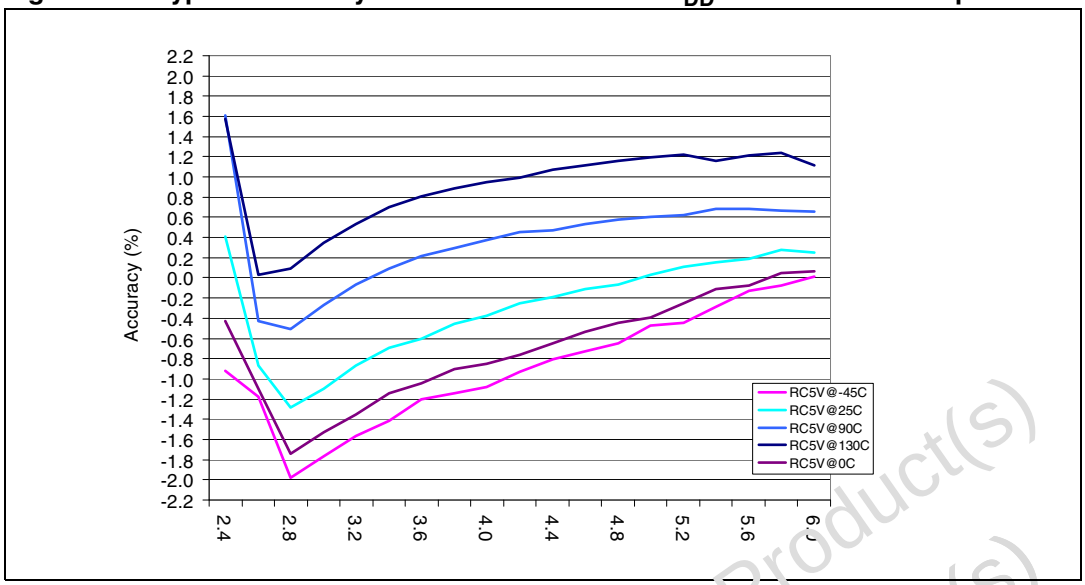


Figure 41. Typical accuracy with RCCR=RCCR1 vs V_{DD}= 2.4-6.0V and temperature

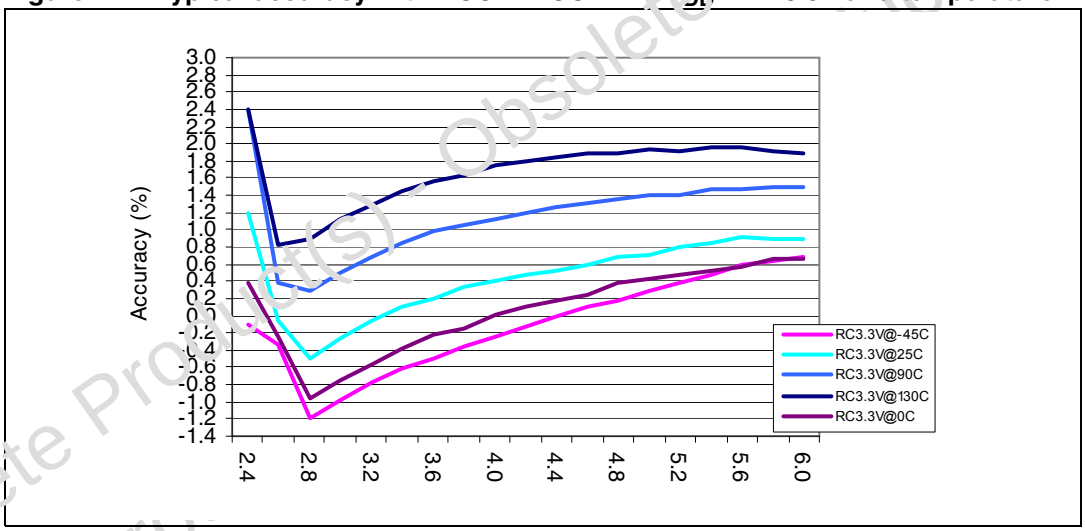


Figure 45. I_{DD} vs temp @V_{DD} 5 V & int RC = 8 MHz

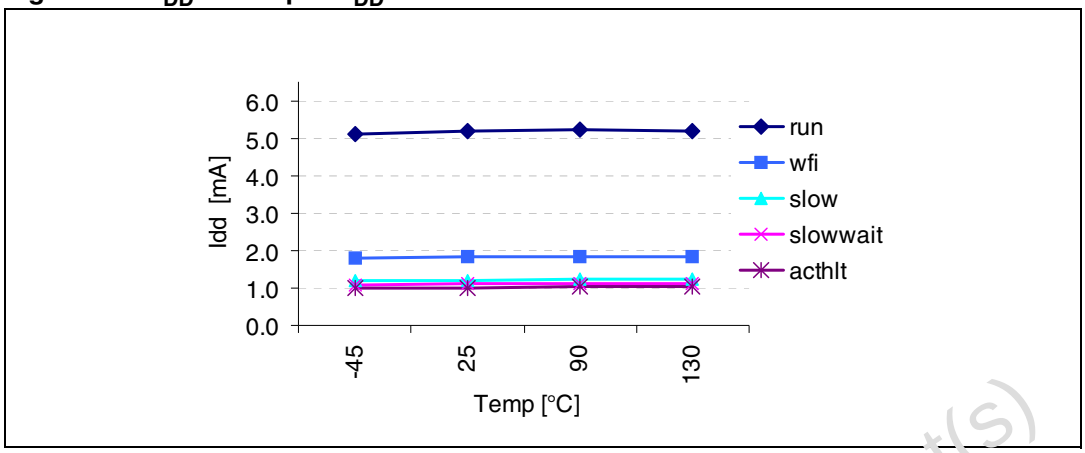


Figure 46. I_{DD} vs temp @V_{DD} 5 V & int RC = 4 MHz

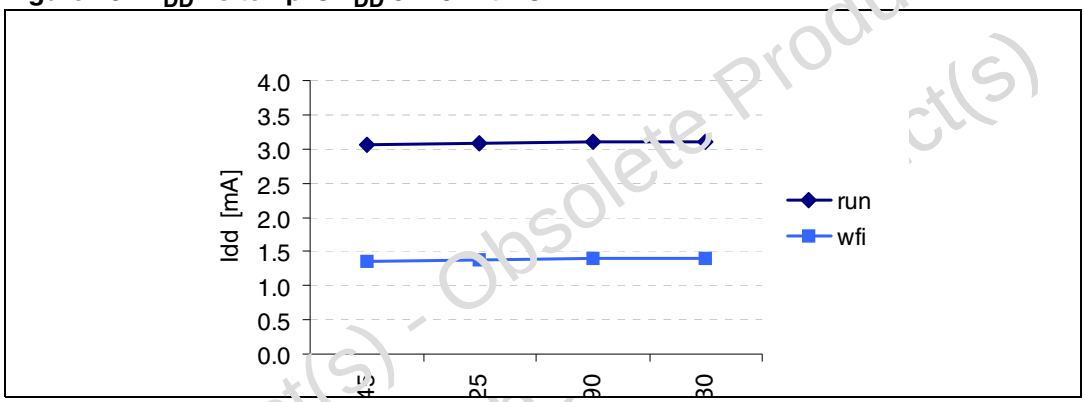


Figure 47. I_{DD} vs temp @V_{DD} 5 V & int RC = 2 MHz

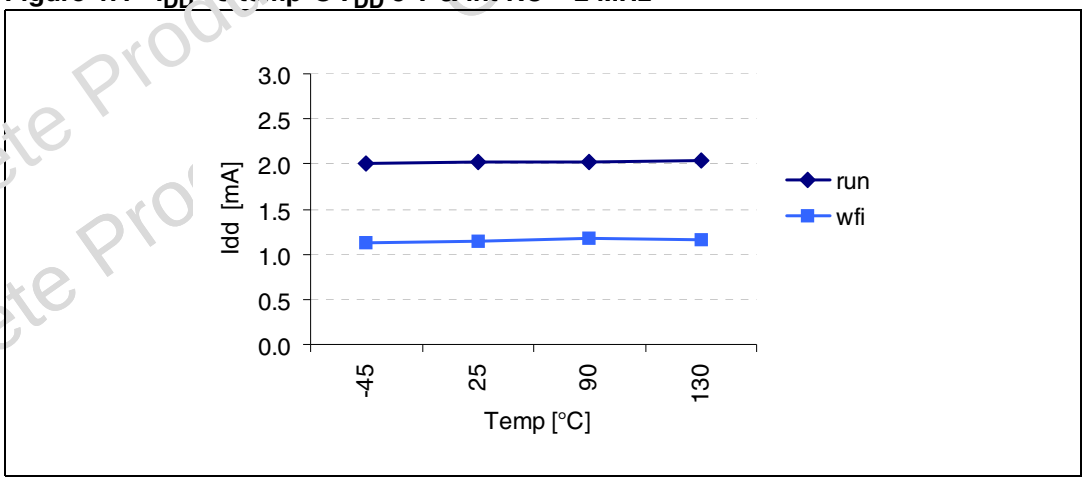


Table 80. Development tool order codes for the ST7LITEUSx family

Supported products	In-circuit Debugger, RLink series[1]		Emulator		Programming tool	
	Starter kit without demo board	Starter kit with Demo Board	DVP series	EMU series	In-circuit programmer	ST socket boards and EPBs
ST7FLITEUS2 ST7FLITEUS5	STX-RLINK[2]	STFLITE-SK/RAIS[2]	ST7MDT10-DVP3[3]	ST7MDT10-EMU3	STX-RLINK ST7-STICK[5][4]	ST7SB10-SU0[5]

1. Available from ST or from Raisonance, www.raisonance.com.
2. USB connection to PC.
3. Includes connection kit for Plastic DIP16/SO16 only. See “How to order an EMU or DVP” in ST product and tool selection guide for connection kit ordering information.
4. Parallel port connection to PC.
5. Add suffix /EU, /UK or /US for the power supply for your region.

14.4 ST7 application notes

Table 81. ST7 application notes

Identification	Description
Application examples	
AN1658	Serial numbering implementation
AN1720	Managing the readout protection in flash microcontrollers
AN1755	A high resolution/precision thermometer using ST7 and NE555
AN1756	Choosing a DALI implementation strategy with ST7DALI
AN1812	A high precision, low cost, single supply ADC for positive and negative input voltages
Example drivers	
AN 969	SCI communication between ST7 and PC
AN 970	SPI communication between ST7 and EEPROM
AN 971	I²C communication between ST7 and M24Cxx EEPROM
AN 972	ST7 software SPI master communication
AN 973	SCI software communication with a PC using ST72251 16-bit timer
AN 974	Real time clock with ST7 Timer Output Compare
AN 976	Driving a buzzer through ST7 timer PWM function
AN 979	Driving an analog keyboard with the ST7 ADC
AN 980	ST7 keypad decoding techniques, implementing wakeup on keystroke
AN1017	Using the ST7 universal serial bus microcontroller
AN1041	Using ST7 PWM signal to generate analog output (sinusoïd)
AN1042	ST7 routine for I²C slave mode management

15 Known limitations

External interrupt 2 (ei2)

Whatever the external interrupt sensitivity configured through EICR1 register, ei2 cannot exit the MCU from Halt, Active-halt and AWUFH modes when a falling edge occurs.

Workaround

None

Table 82. Document revision history (continued)

Date	Revision	Changes
18-Sep-06	3	Modified description of AVD[1:0] bits in the AVDTRH register in *Section 7.4.4* Modified description of CNTR[11:0] bits in *Section 10.2.6: Register description* Modified values in *Table 44* LVD and AVD tables updated, *Table 47*, *Table 48* and *Table 49* Internal RC oscillator data modified in *Table 50* and new table added *Table 51* Typical data in *Table 54* (on chip peripherals) modified EMC characteristics updated, *Section 12.7* R_{PU} data corrected in *Table 63* including additional notes Output driving current table updated, *Table 64* R_{ON} data corrected in *Table 65*. Modified ADC accuracy tables in *Section 12.10* *Section :* updated Errata sheet removed from document Notes modified for low voltage detector *Section 7.4.1* Notes updated in *Section 4.4* (I^2C Interface) Thermal characteristics table updated, *Table 74* Modified option list on *Section 14.2: Ordering information* Modified *Section 14.3: Development tools* Modified text in *Section :*
26-Jan-07	4	Added -40°C to 125°C temperature range Modified note on ei4 in *Table 9. Interrupt mapping* Added note 3 to *Section 7.4.2: External Interrupt Control register 2 (EICR2)* Added *Figure 41* and *Figure 40* Added a note to LVDRF in *Section 7.4.4: Register description* *Section 6.4.1: Introduction* Modified *Table 47* and *Table 48* Modified *Table 50*Updated *Table 53* Updated *Table 64* Modified R_{AIN} and ADC accuracy tables in *Section 12.10: ADC characteristics* Modified *Table 80* Modified *Table 79* Modified option list on *Figure 69: Option list*
06-Feb-2009	5	Document reformatted. Replaced ST7ULTRALITE by ST7LITEUS2 and ST7LITEUS5. Removed limitations in user and in I^2C mode from *Section 15: Known limitations*, and added *External interrupt 2 (ei2)*. Added MCO on pin 3. Updated *Section 12.3.2: Operating conditions with low voltage detector (LVD)*, *Section 12.3.3: Auxiliary voltage detector (AVD) thresholds*, *Section 12.3.4: Internal RC oscillator*, *Section 12.4: Supply current characteristics*, and *Section 12.8.2: Output driving current characteristics*. Updated internal RC prescaler to add 500 KHz. Updated ECOPACK text in *Section 13.1: Package mechanical data*. Added PDIP16 silhouette on cover page, and updated *Table 73: 16-pin plastic dual in-line package, 300-mil width, package mechanical data* and *Figure 68: 16-pin plastic dual in-line package, 300-mil width, package outline*. Changed order codes to die A version in *Table 79: Supported order codes*. Removed soldering information section. Updated option list.