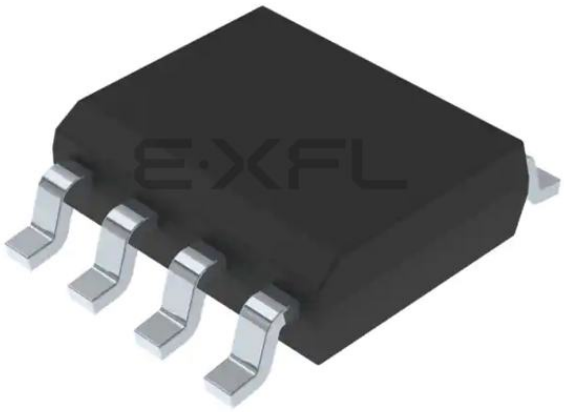


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

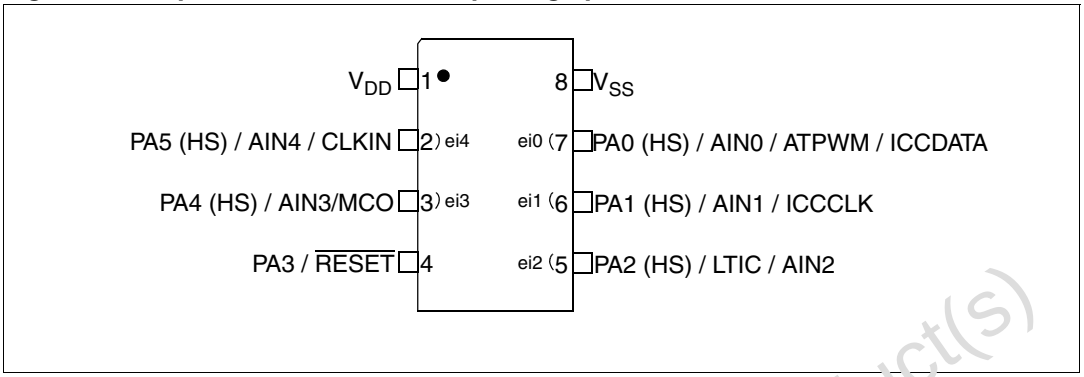
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fliteus2m3tr

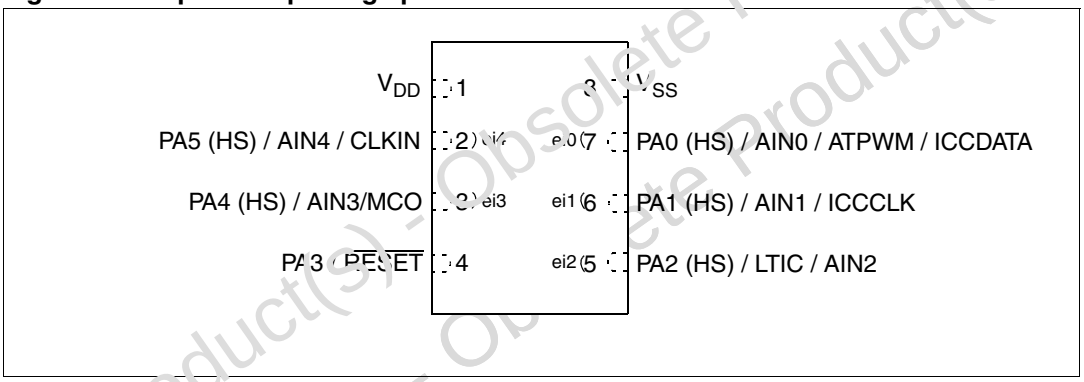
2 Pin description

Figure 2. 8-pin SO and Plastic DIP package pinout



1. HS: High sink capability.
2. eix : associated external interrupt vector

Figure 3. 8-pin DFN package pinout



1. HS: High sink capability.
2. eix : associated external interrupt vector

Table 3. Hardware register map (continued)(1)

Address	Block	Register label	Register name	Reset status	Remarks
0049h 004Ah	AWU	AWUPR AWUCSR	AWU Prescaler register AWU Control/Status register	FFh 00h	R/W R/W
004Bh 004Ch 004Dh 004Eh 004Fh 0050h	DM(4)	DMCR DMSR DMBK1H DMBK1L DMBK2H DMBK2L	DM Control register DM Status register DM Breakpoint register 1 High DM Breakpoint register 1 Low DM Breakpoint register 2 High DM Breakpoint register 2 Low	00h 00h 00h 00h 00h 00h	R/W R/W R/W R/W R/W R/W
0051h to 007Fh	Reserved area (47 bytes)				

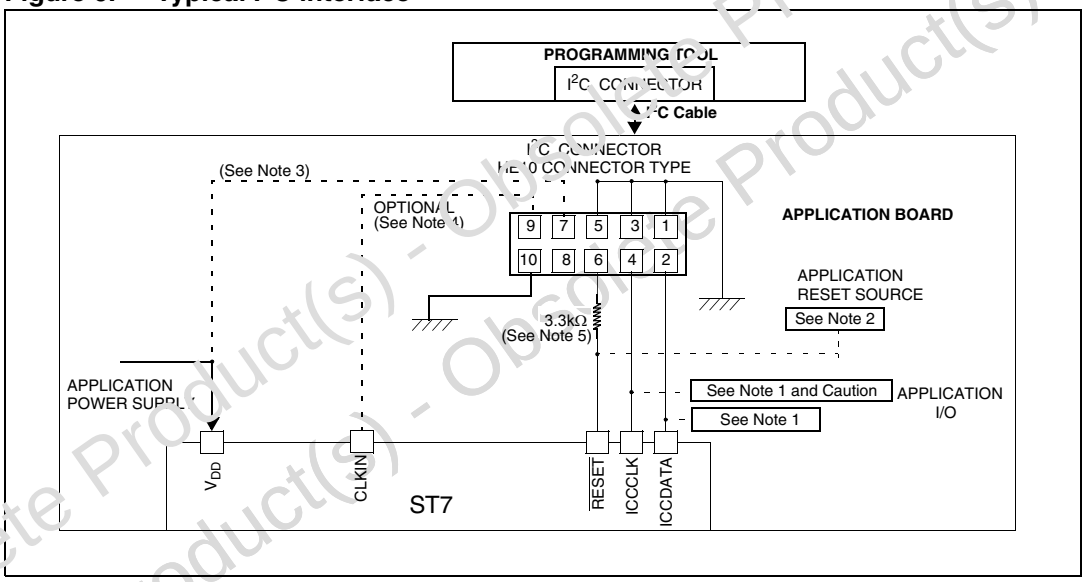
1. Legend: x=undefined, R/W=read/write
2. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.
3. The bits associated with unavailable pins must always keep their reset value.
4. For a description of the DM registers, see the ST7 I^2C Protocol Reference Manual.

Pin 9 has to be connected to the CLKIN pin of the ST7 when I^2C mode is selected with option bytes disabled (35-pulse I^2C entry mode). When option bytes are enabled (38-pulse I^2C entry mode), the internal RC clock (internal RC or AWU RC) is forced. If internal RC is selected in the option byte, the internal RC is provided. If AWU RC or external clock is selected, the AWU RC oscillator is provided.

A serial resistor must be connected to I^2C connector pin 6 in order to prevent contention on PA3/$\overline{\text{RESET}}$ pin. Contention may occur if a tool forces a state on $\overline{\text{RESET}}$ pin while PA3 pin forces the opposite state in output mode. The resistor value is defined to limit the current below 2 mA at 5 V. If PA3 is used as output push-pull, then the application must be switched off to allow the tool to take control of the $\overline{\text{RESET}}$ pin (PA3). To allow the programming tool to drive the $\overline{\text{RESET}}$ pin below V_{IL}, special care must also be taken when a pull-up is placed on PA3 for application reasons.

Caution: During normal operation, ICCCLK pin must be pulled- up, internally or externally (external pull-up of 10 kΩ mandatory in noisy environment). This is to avoid entering I^2C mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up.

Figure 6. Typical I^2C interface



4.5 Memory protection

There are two different types of memory protection: readout protection and Write/Erase Protection which can be applied individually.

4.5.1 Readout protection

Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller. Program memory is protected.

In flash devices, this protection is removed by reprogramming the option. In this case, program memory is automatically erased, and the device can be reprogrammed.

Readout protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the option list.

4.5.2 Flash Write/Erase protection

Write/erase protection, when set, makes it impossible to both overwrite and erase program memory. Its purpose is to provide advanced security to applications and prevent any change being made to the memory content.

Warning: Once set, Write/erase protection can never be removed. A write-protected flash device is no longer reprogrammable.

Write/erase protection is enabled through the FMP_W bit in the option byte.

4.6 Related documentation

For details on Flash programming and I^2C protocol, refer to the ST7 Flash programming reference manual and to the ST7 I^2C protocol reference manual.

Figure 15. Low voltage detector vs reset

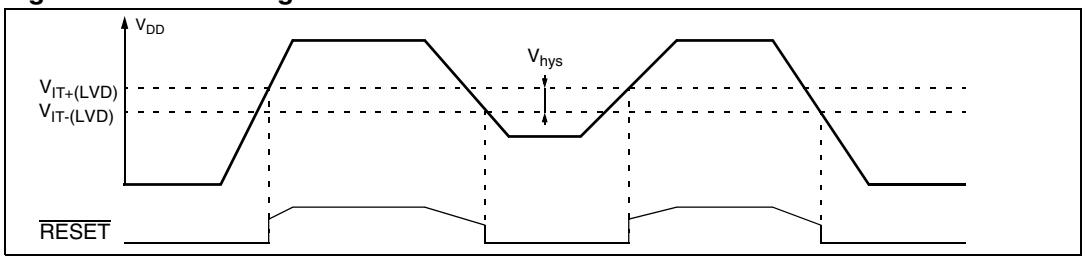
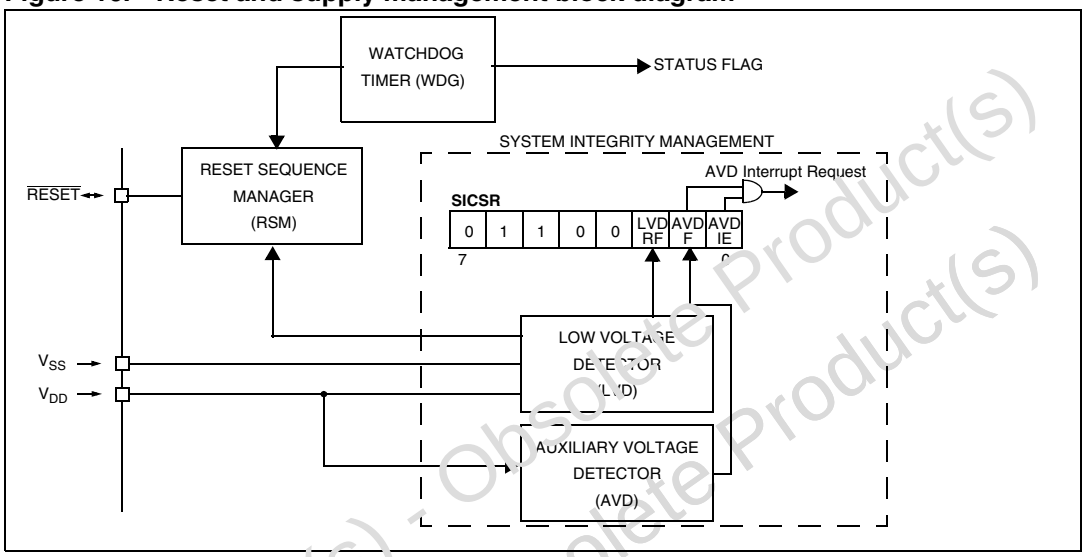


Figure 16. Reset and supply management block diagram



8.4.1 Active-halt mode

Active-halt mode is the lowest power consumption mode of the MCU with a real time clock available. It is entered by executing the 'HALT' instruction when Active-halt mode is enabled.

The MCU can exit Active-halt mode on reception of a Lite Timer / AT Timer interrupt or a reset.

- When exiting Active-halt mode by means of a reset, a 64 CPU cycle delay occurs. After the start up delay, the CPU resumes operation by fetching the reset vector which woke it up (see *Figure 22*).
- When exiting Active-halt mode by means of an interrupt, the CPU immediately resumes operation by servicing the interrupt vector which woke it up (see *Figure 22*).

When entering Active-halt mode, the I bit in the CC register is cleared to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes up immediately.

In Active-halt mode, only the main oscillator and the selected timer counter (LT/AT) are running to keep a wakeup time base. All other peripherals are not clocked except those which get their clock supply from another clock generator (such as external or auxiliary oscillator).

Caution: As soon as Active-halt is enabled, executing a HALT instruction while the watchdog is active does not generate a reset if the WDGHALT bit is reset.
This means that the device cannot spend more than a defined delay in this power saving mode.

Figure 21. Active-halt timing overview

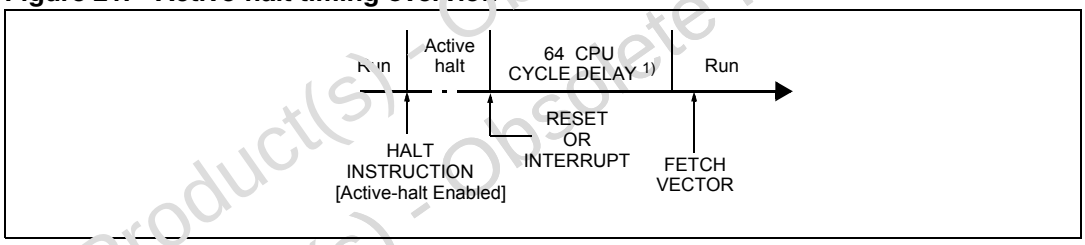
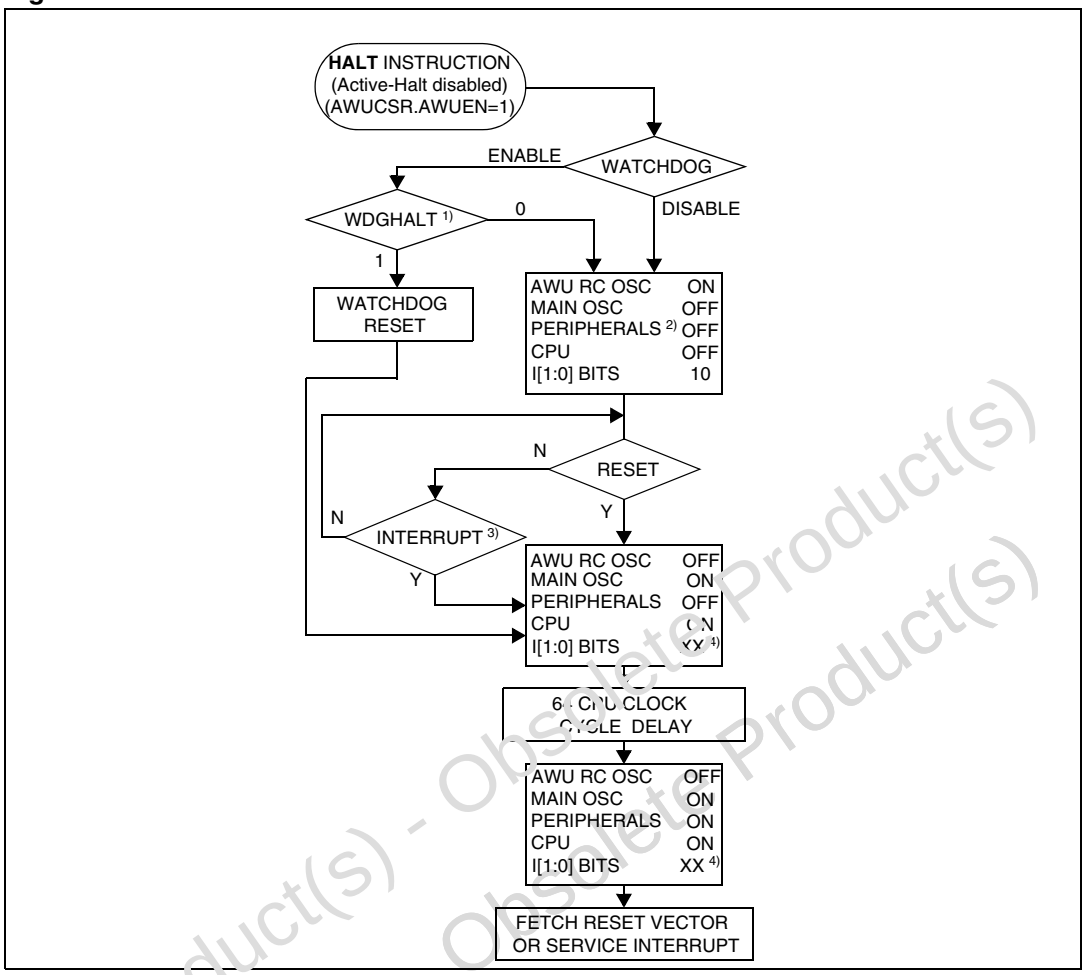


Figure 27. AWUFH mode flowchart



1. WDGHALT is an option bit. See option byte section for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only an AWUFH interrupt and some specific interrupts can exit the MCU from Halt mode (such as external interrupt). Refer to *Table 9: Interrupt mapping* for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

9.2.3 Alternate functions

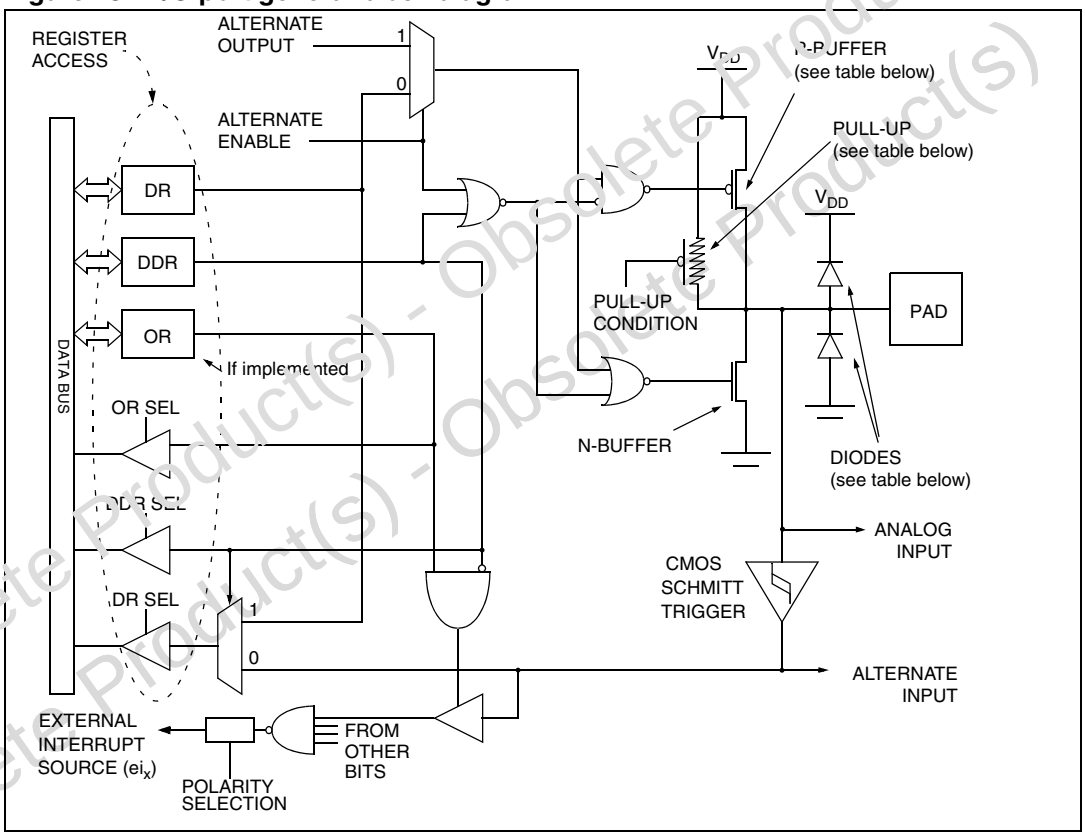
When an on-chip peripheral is configured to use a pin, the alternate function is automatically selected. This alternate function takes priority over the standard I/O programming under the following conditions:

- When the signal is coming from an on-chip peripheral, the I/O pin is automatically configured in output mode (push-pull or open drain according to the peripheral).
- When the signal is going to an on-chip peripheral, the I/O pin must be configured in floating input mode. In this case, the pin state is also digitally readable by addressing the DR register.

Note: 1 Input pull-up configuration can cause unexpected value at the input of the alternate peripheral input.

2 When an on-chip peripheral use a pin as input and output, this pin has to be configured in input floating mode.

Figure 28. I/O port general block diagram



10.2 12-bit auto-reload timer (AT)

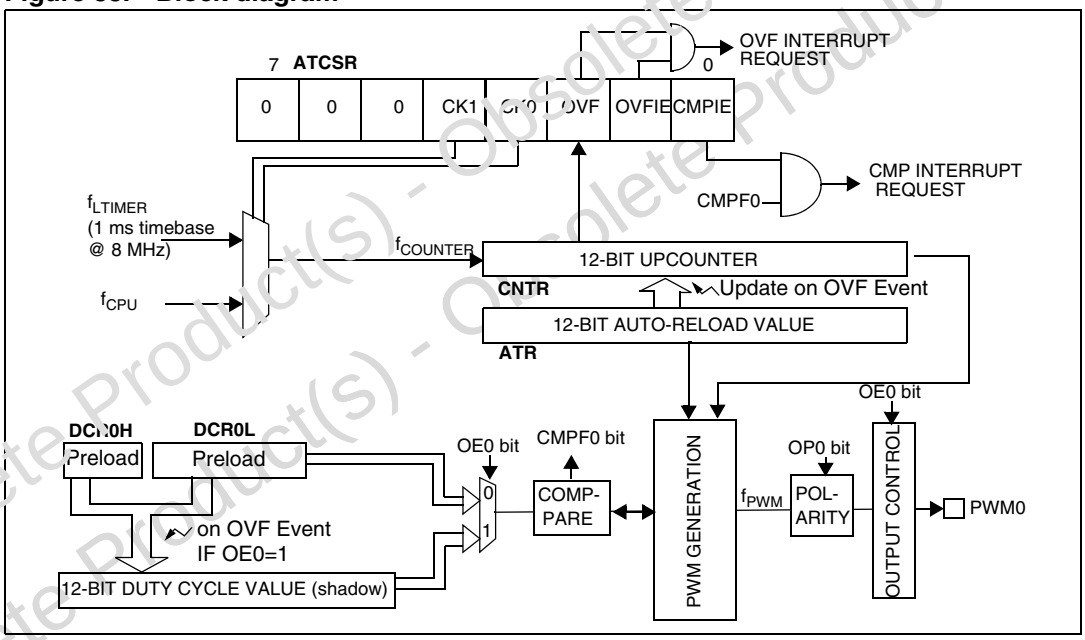
10.2.1 Introduction

The 12-bit auto-reload timer can be used for general-purpose timing functions. It is based on a free-running 12-bit upcounter with a PWM output channel.

10.2.2 Main features

- 12-bit upcounter with 12-bit auto-reload register (ATR)
- Maskable overflow interrupt
- PWM signal generator
- Frequency range 2 kHz - 4 MHz (@ 8 MHz f_{CPU})
  - Programmable duty-cycle
  - Polarity control
  - Maskable compare interrupt
- Output compare function

Figure 33. Block diagram



10.2.3 Functional description

PWM mode

This mode allows a pulse width modulated signals to be generated on the PWM0 output pin with minimum core processing overhead. The PWM0 output signal can be enabled or disabled using the OE0 bit in the PWMCR register. When this bit is set the PWM I/O pin is configured as output push-pull alternate function.

Note: CMPF0 is available in PWM mode (see Section : PWM0 control/status register (PWM0CSR)).

10.2.5 Interrupts

Table 28. Interrupt events

Interrupt event [1]	Event flag	Enable control bit	Exit from Wait	Exit from Halt	Exit from Active-halt
Overflow event	OVF	OVFIE	Yes	No	Yes[2]
CMP event	CMPFx	CMPIE	Yes	No	No

1. The interrupt events are connected to separate interrupt vectors (see Interrupts chapter). They generate an interrupt if the enable bit is set in the ATCSR register and the interrupt mask in the CC register is reset (RIM instruction).
2. Only if CK0=1 and CK1=0

10.2.6 Register description

Timer control status register (ATCSR)

Reset value: 0000 0000 (00h)

7							0
0	0	0	CK1	CK0	OVF	OVFIE	CMPIE
Read/write							

Bits 7:5 Reserved, must be kept cleared.

Bits 4:3 **CK[1:0]** *Counter Clock Selection.*
These bits are set and cleared by software and cleared by hardware after a reset. They select the clock frequency of the counter (see *Table 29: Counter clock selection*).

Bit 2 **OVF** *Overflow flag.*
This bit is set by hardware and cleared by software by reading the ATCSR register. It indicates the transition of the counter from FFFh to ATR value.
0: No counter overflow occurred
1: Counter overflow occurred
When set, the OVF bit stays high for 1 $f_{COUNTER}$ cycle (up to 1ms depending on the clock selection) after it has been cleared by software.

Bit 1 **OVFIE** *Overflow interrupt enable.*
This bit is read/write by software and cleared by hardware after a reset.
0: OVF interrupt disabled
1: OVF interrupt enabled

Bit 0 **CMPIE** *Compare interrupt enable.*
This bit is read/write by software and clear by hardware after a reset. It allows to mask the interrupt generation when CMPF bit is set.
0: CMPF interrupt disabled
1: CMPF interrupt enabled

ADC data register high (ADCDRH)

Reset value: 0000 0000 (00h)

7							0
D9	D8	D7	D6	D5	D4	D3	D2
Read only							

Bits 7:0 D[9:2] *MSB of Analog Converted value*

ADC control/data register Low (ADCDRL)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	SLOW	0	D1	D0
Read/write							

Bits 7:4 Reserved. Forced by hardware to 0.

Bit 3 **SLOW** *Slow mode*
This bit is set and cleared by software. It is used together with the SPEED bit to configure the ADC clock speed as shown on the table below (see *Table 33: Configuring the ADC clock speed*).

Bit 2 Reserved. Forced by hardware to 0.

Bits 1:0 **D[1:0]** *LSB of Analog Converted value*

Table 33. Configuring the ADC clock speed

f_{ADC}	SLOW	SPEED
$f_{CPU}/2$	0	0
f_{CPU}	0	1
$f_{CPU}/4$	1	x

Table 34. ADC register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0034h	**ADCCSR** Reset value	EOC 0	SPEED 0	ADON 0	0 0	0 0	CH2 0	CH1 0	CH0 0
0035h	**ADCDRH** Reset value	D9 0	D8 0	D7 0	D6 0	D5 0	D4 0	D3 0	D2 0
0036h	**ADCDRL** Reset value	0 0	0 0	0 0	0 0	SLOW 0	0 0	D1 0	D0 0

Table 39. Instructions supporting direct, indexed, indirect and indirect indexed addressing modes (continued)

Instructions	Function
CPL, NEG	1 or 2 complement
BSET, BRES	Bit operations
BTJT, BTJF	Bit test and jump operations
SLL, SRL, SRA, RLC, RRC	Shift and rotate operations
SWAP	Swap nibbles
CALL, JP	Call or jump subroutine

11.1.7 Relative modes (direct, indirect)

This addressing mode is used to modify the PC register value by adding an 8-bit signed offset to it.

Table 40. Instructions supporting relative modes

Available relative direct/indirect instructions	Function
JRxx	Conditional jump
CALLR	Call relative

The relative addressing mode consists of two submodes:

Relative mode (Direct)

The offset follows the opcode.

Relative mode (Indirect)

The offset is defined in memory, of which the address follows the opcode.

11.2 Instruction groups

The ST7 family devices use an Instruction Set consisting of 63 instructions. The instructions may be subdivided into 13 main groups as illustrated in the following table:

Table 41. ST7 instruction set

Load and Transfer	LD	CLR						
Stack operation	PUSH	POP	RSP					
Increment/Decrement	INC	DEC						
Compare and tests	CP	TNZ	BCP					
Logical operations	AND	OR	XOR	CPL	NEG			
Bit operation	BSET	BRES						
Conditional bit test and branch	BTJT	BTJF						
Arithmetic operations	ADC	ADD	SUB	SBC	MUL			

Figure 42. Typical I_{DD} in run mode vs. internal clock frequency and V_{DD}

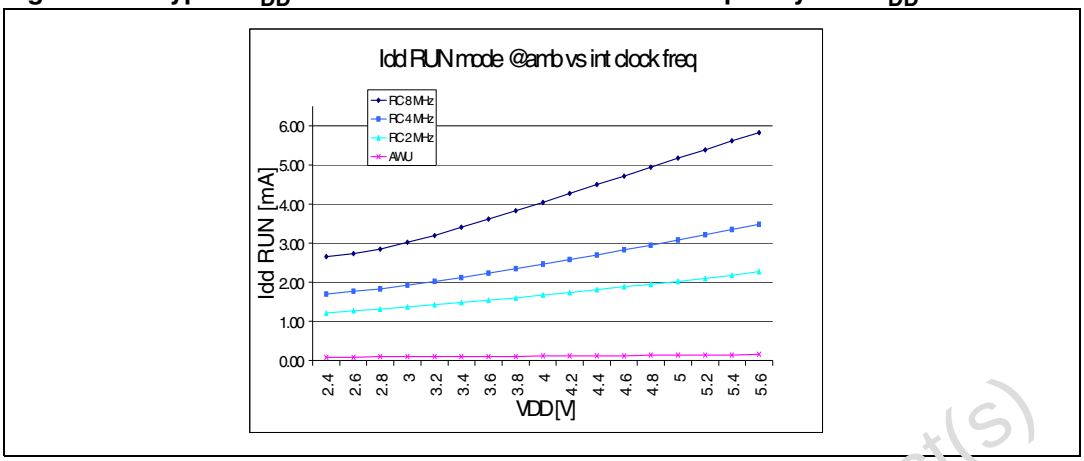


Figure 43. Typical I_{DD} in WFI mode vs. internal clock frequency and V_{DD}

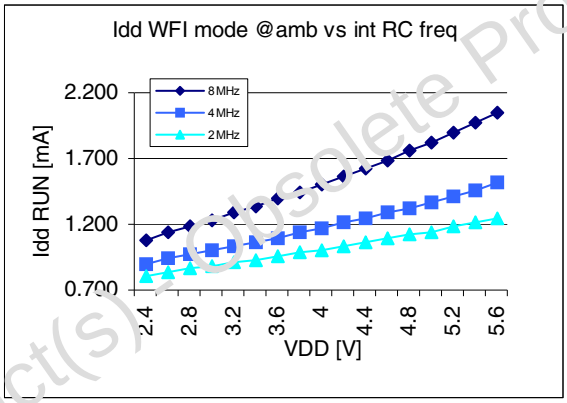


Figure 44. Typical I_{DD} in Slow, Slow-wait and Active-halt mode vs V_{DD} & int RC = 8 MHz

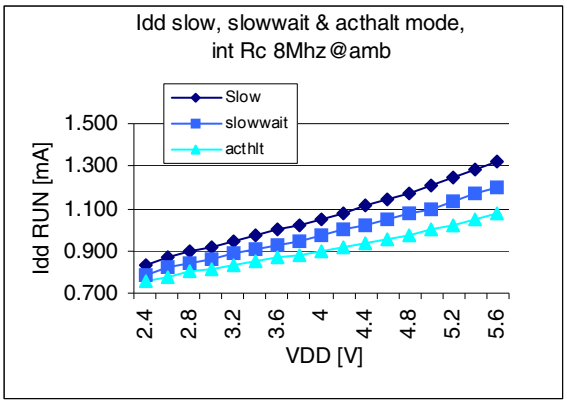


Figure 59. Typical V_{OL} vs. V_{DD} (HS pins)

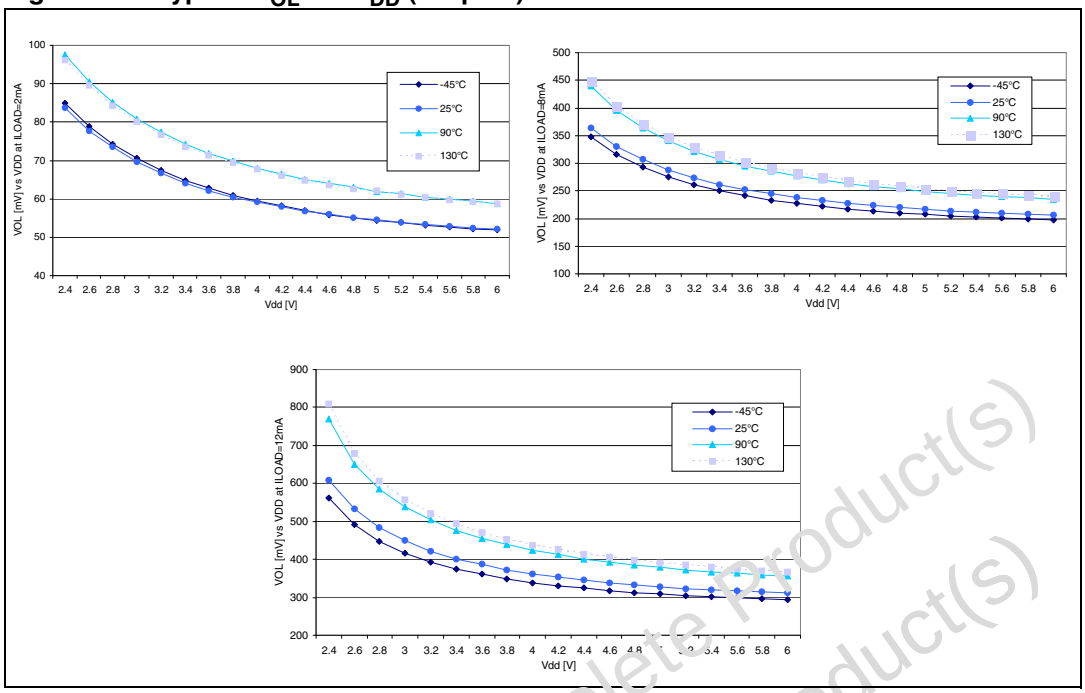
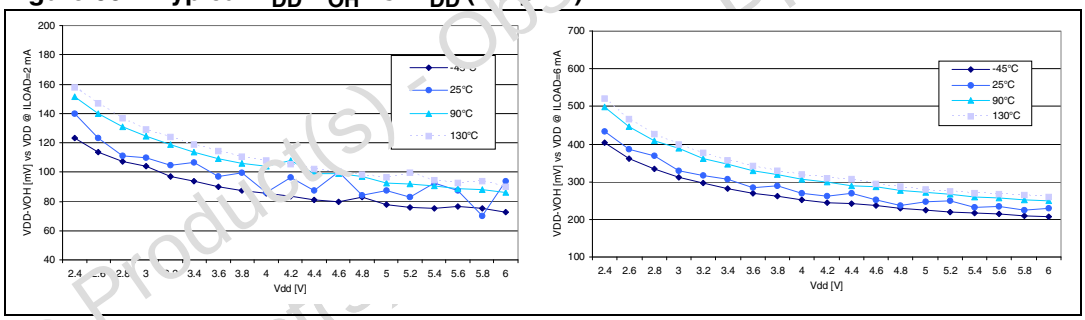


Figure 60. Typical V_{DD}-V_{OH} vs. V_{DD} (HS pins)



12.9 Control pin characteristics

The reset network protects the device against parasitic resets.

The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).

Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} max. level specified in *Table 65*. Otherwise the reset will not be taken into account internally.

Because the reset circuit is designed to allow the internal reset to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin is less than the absolute maximum value specified for $I_{INJ(RESET)}$ in *Table 44*.

Refer to *Figure 61* and *Figure 62* for a description of the $\overline{\text{RESET}}$ pin protection circuit with LVD enabled and disabled.

14 Device configuration and ordering information

Each device is available for production in user programmable versions (FLASH) as well as in factory coded versions (FASTROM). Refer to *Table 79* for the full list of supported part numbers:

- ST7FLITEUSA2xx and ST7FLITEUSA5xx XFlash devices are shipped to customers with a default program memory content (FFh).
- Factory Advanced Service Technique ROM (FASTROM) versions are also available: they are factory-programmed XFlash devices.

The FASTROM factory coded parts contain the code supplied by the customer. This implies that FLASH devices have to be configured by the customer using the Option Bytes while the FASTROM devices are factory-configured.

14.1 Option bytes

The two option bytes allow the hardware configuration of the microcontroller to be selected.

The option bytes can be accessed only in programming mode (for example using a standard ST7 programming tool).

14.1.1 OPTION BYTE 1

Bit 7:6 **CKSEL[1:0]** *Startup clock selection.*
This bit is used to select the startup frequency. By default, the internal RC is selected (see *Table 75: Startup clock selection*).

Bit 5 Reserved, must always be 1.

Bit 4 Reserved, must always be 0.

Bits 3:2 **LVD[1:0]** *Low Voltage Detection selection*
These option bits enable the LVD block with a selected threshold as shown in *Table 76: LVD threshold configuration*.

Bit 1 **WDG SW** *Hardware or software watchdog*
This option bit selects the watchdog type.
0: Hardware (watchdog always enabled)
1: Software (watchdog to be enabled by software)

Bit 0 **WDG HALT** *Watchdog Reset on Halt*
This option bit determines if a reset is generated when entering Halt mode while the watchdog is active.
0: No Reset generation when entering Halt mode
1: Reset generation when entering Halt mode

Table 78:

	OPTION BYTE 0								OPTION BYTE 1							
	7							0	7							0
	Reserved					SEC0	FMPR	FMPW	CKSEL 1	CKSEL 0	Res	Res	LVD1	LVD0	WDG SW	WDG HALT
Default value	1	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1

14.2 Ordering information

Customer code is made up of the FASTROM contents and the list of the selected options (if any). The FASTROM contents are to be sent on diskette, or by electronic means, with the S19 hexadecimal file generated by the development tool. All unused bytes must be set to FFh. The selected options are communicated to STMicroelectronics using the correctly completed option list appended.

Refer to application note AN1635 for information on the counter listing returned by ST after code has been transferred.

The STMicroelectronics Sales Organization will be pleased to provide detailed information on contractual points.

Table 79. Supported order codes (1)

Order code	Program memory (bytes)	RAM (bytes)	ADC	Temperature range	Package	Conditioning
ST7FLITEUSA2B6	1 Kbyte FLASH	128	-	-40°C +85°C	DIP8	Tube
ST7FLITEUSA2M6			-		SO8	Tube
ST7FLITEUSA2M6TR			-		SO8	Tape & Reel
ST7FLITEUSA2U6TR			-		DFN8	Tape & Reel
ST7FLITEUSA5B6	1 Kbyte FLASH	128	10-bit	-40°C +85°C	DIP8	Tube
ST7FLITEUSA5M6			10-bit		SO8	Tube
ST7FLITEUSA5M6TR			10-bit		SO8	Tape & Reel
ST7FLITEUSA5U6			10-bit		DFN8	Tray
ST7FLITEUSA5U6TR			10-bit		DFN8	Tape & Reel
ST7FLITEUSICD	1 Kbyte FLASH	128	-	-40°C +125°C	DIP16(2)	Tube
ST7PLUSA2B6	1 Kbyte FASTROM	128	-	-40°C +85°C	DIP8	Tube
ST7PLUSA2M6			-		SO8	Tube
ST7PLUSA2M6TR			-		SO8	Tape & Reel
ST7PLUSA2U6TR			-		DFN8	Tape & Reel

Table 79. Supported order codes [1] (continued)

Order code	Program memory (bytes)	RAM (bytes)	ADC	Temperature range	Package	Conditioning
ST7PLUSA5B6	1 Kbyte FASTROM	128	10-bit	-40°C +85°C	DIP8	Tube
ST7PLUSA5M6			10-bit		SO8	Tube
ST7PLUSA5M6TR			10-bit		SO8	Tape & Reel
ST7PLUSA5U6			10-bit		DFN8	Tray
ST7PLUSA5U6TR			10-bit		DFN8	Tape & Reel
ST7PLUSA2B3	1 Kbyte FLASH	128	-	-40°C +125°C	DIP8	Tube
ST7PLUSA2M3			-		SO8	Tube
ST7PLUSA2M3TR			-		SO8	Tape & Reel
ST7PLUSA2U3TR			-		DFN8	Tape & Reel
ST7PLUSA5B3	1 Kbyte FLASH	128	10-bit	-40°C +125°C	DIP8	Tube
ST7PLUSA5M3			10-bit		SO8	Tube
ST7PLUSA5M3TR			10-bit		SO8	Tape & Reel
ST7PLUSA5U3			10-bit		DFN8	Tray
ST7PLUSA5U3TR			10-bit		DFN8	Tape & Reel
ST7PLUSA2B3	1 Kbyte FASTROM	128	-	-40°C +125°C	DIP8	Tube
ST7PLUSA2M3			-		SO8	Tube
ST7PLUSA2M3TR			-		SO8	Tape & Reel
ST7PLUSA2U3TR			-		DFN8	Tape & Reel
ST7PLUSA5B3	1 Kbyte FASTROM	128	10-bit	-40°C +125°C	DIP8	Tube
ST7PLUSA5M3			10-bit		SO8	Tube
ST7PLUSA5M3TR			10-bit		SO8	Tape & Reel
ST7PLUSA5U3			10-bit		DFN8	Tray
ST7PLUSA5U3TR			10-bit		DFN8	Tape & Reel

1. Contact ST sales office for product availability.
2. For development or tool prototyping purposes only, not orderable in production quantities.

16 Revision history

Table 82. Document revision history

Date	Revision	Changes
06-Feb-06	1	Initial release
18-Apr-06	2	Removed references to 3% RC Added note below *Figure 4* Modified presentation of *Section 4.3.1* Added notes to *Section 6.2* (above *Figure 9*), replaced 8-bit calibration value to 10-bit calibration value and changed application note reference (AN2326 instead of AN1324) Modifed *Table 7: Clock register map and reset values* and added b t 1 in the description of CKCNTCSR register Modified Figure 13 (added CKCNTCSR register) Added note 2 to EICRx description Modified caution in section 7.2 on page 25 Replaced $V_{IT+(LVD)}$ by $V_{IT+(LVD)}$ in *Section : Monitoring the VDD main supply* Modified LVDRF bit description in *Section 7.4.4: Register description* Replaced “oscillator” by “main oscillator” in the second paragraph of *Section 8.4.2: Halt mode* Added note 1 to *Figure 23* and added note 5 to *Figure 24* Modified *Section 8.5: Auto-wakeup from Halt mode* Replaced bit 1 by bit 2 for AWUF bit in *Section 8.5.1: Register description* Modified *Section 9.1: Introduction*. Modified *Section : External interrupt function*.Updated *Section 9.5: Interrupts*. Modified *Section Table 47.: Operating conditions with low voltage detector (LVD)*. Modified *Table 48: Auxiliary Voltage Detector (AVD) Thresholds*. Modified *Table 49: Voltage drop between AVD flag set and LVD reset generation*. Modified *Table 50: Internal RC oscillator calibrated at 5 V*. Modified *Table 53: Supply current*. Modified *Table 54: On-chip peripherals*. Modified *Table 63: General characteristics*. Modified *Table 64: Output driving current*. Modified *Table 65: Asynchronous RESET pin characteristics*. Modified *Section 12.10: ADC characteristics*. Added *Figure 49*. Modified *Figure 61*. Removed EMC protection circuitry in *Figure 62* (device works correctly without these components). Added ECOPACK text in *Section 13: Package characteristics*. Modified first paragraph in *Section 14: Device configuration and ordering information*. Modified *Table 79*. Modified conditioning option in option list. Modified *Section 14.3: Development tools*. Added *Section 14.4: ST7 application notes*. Added *Section :* . Added erratasheet at the end of the document.