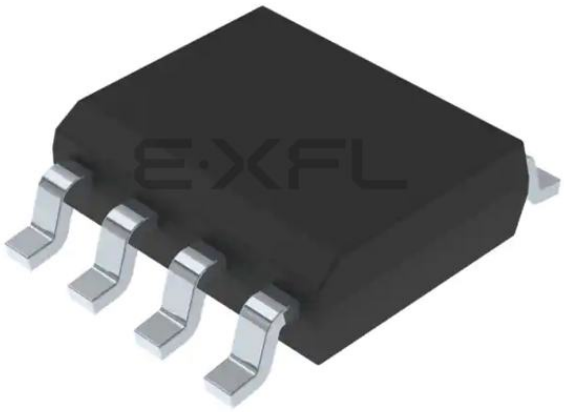

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fliteus2m6

1 Introduction

The ST7LITEUS2 and ST7LITEUS5 are members of the ST7 microcontroller family. All ST7 devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

The ST7LITEUS2 and ST7LITEUS5 feature FLASH memory with byte-by-byte In-Circuit Programming (ICP) and In-Application Programming (IAP) capability.

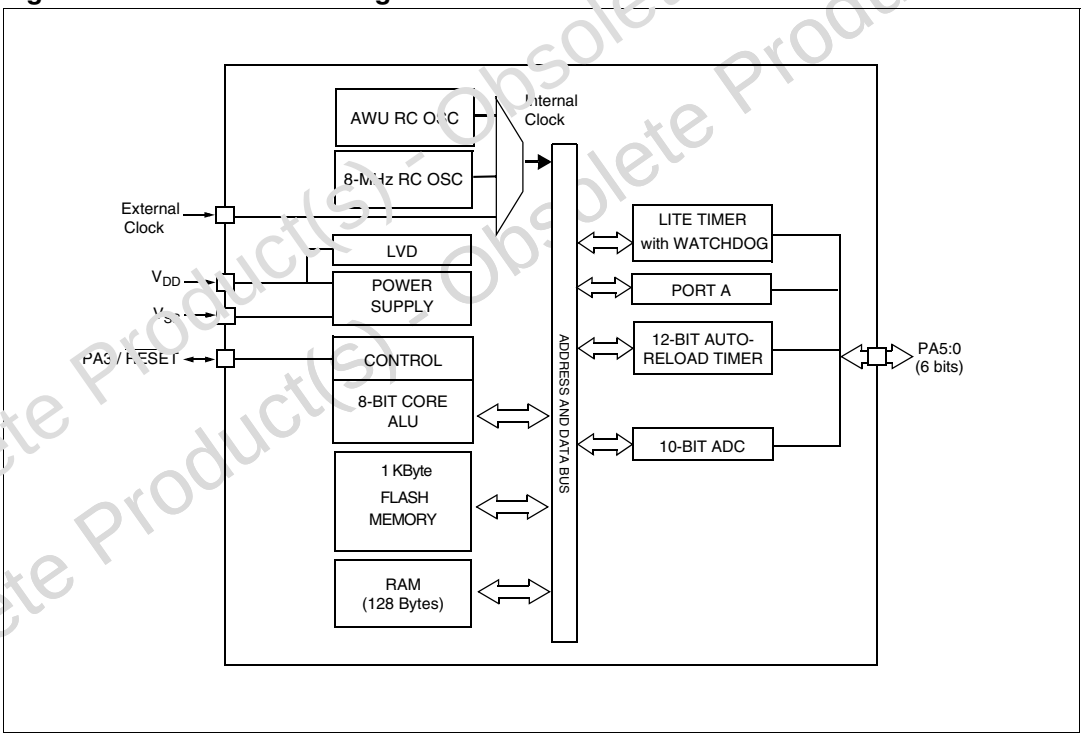
Under software control, the ST7LITEUS2 and ST7LITEUS5 can be placed in Wait, Slow, or Halt mode, reducing power consumption when the application is in idle or standby state.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

For easy reference, all parametric data are located in *Section 12 on page 92*.

The devices feature an on-chip debug module (DM) to support in circuit debugging (ICD). For a description of the DM registers, refer to the ST7 I²C protocol reference manual.

Figure 1. General block diagram



6.3.2 RC Control register (RCCR)

Reset value: 1111 1111 (FFh)

7							0
CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2
Read / Write							

Bits 7:0 **CR[9:2]** *RC Oscillator Frequency Adjustment Bits*
These bits, as well as CR[1:0] bits in the SICSR register must be written immediately after reset to adjust the RC oscillator frequency and to obtain the required accuracy. The application can store the correct value for each voltage range in Flash memory and write it to this register at startup.
00h = maximum available frequency
FFh = lowest available frequency

Note: To tune the oscillator, write a series of different values in the register until the correct frequency is reached. The fastest method is to use a dichotomy starting with 80h.

6.3.3 System Integrity (SI) Control/status register (SICSR)

Reset value: 0000 0x00 (0xh)

7							0
0	CR1	CR0	0	0	LVDRF	AVDF	AVDIE
Read / Write							

Bit 7 Reserved, must be kept cleared.

Bits 6:5 **CR[1:0]** *RC Oscillator Frequency Adjustment bits*
These bits, as well as CR[9:2] bits in the RCCR register must be written immediately after reset to adjust the RC oscillator frequency and to obtain the required accuracy. Refer to *Section 6.2 on page 28*.

Bits 4:3 Reserved, must be kept cleared.

Bits 2:0 System Integrity bits. Refer to *Section 7.4 on page 43*.

Bit 2 **RC_FLAG** *RC Selection*
This bit is set and cleared by hardware
0: No switch from RC to AWU requested
1: RC clock activated and temporization completed

Bit 1 = Reserved, must be kept cleared.

Bit 0 = **RC/AWU** *RC/AWU Selection*
0: RC enabled
1: AWU enabled (default value)

Table 7. Clock register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0038h	MCCSR Reset value	0	0	0	0	0	0	MCO 0	SMS 0
0039h	RCCR reset value	CR9 1	CR8 1	CR7 1	CR6 1	CR5 1	CR4 1	CR3 1	CR2 1
003Ah	SICSR reset value	0	CR1	CR0	0	0	LVDRF x	AVDF 0	AVDIE 0
003Eh	AVDTHCR reset value	CK2 0	CK1 0	CK0 0	0	0	0	AVD1 1	AVD2 1
003Fh	CKCNTCSR reset value	0	0	0	0	AWU_FLAG 1	RC_FLAG 0	0	RC/AWU 1

7.2 External interrupts

External interrupt vectors can be loaded into the PC register if the corresponding external interrupt occurred and if the I bit is cleared. These interrupts allow the processor to leave the Halt low power mode.

The external interrupt polarity is selected through the miscellaneous register or interrupt register (if available).

An external interrupt triggered on edge will be latched and the interrupt request automatically cleared upon entering the interrupt service routine.

Caution: The type of sensitivity defined in the Miscellaneous or Interrupt register (if available) applies to the ei source. In case of a NANDed source (as described in the I/O ports section), a low level on an I/O pin, configured as input with interrupt, masks the interrupt request even in case of rising-edge sensitivity.

7.3 Peripheral interrupts

Different peripheral interrupt flags in the status register are able to cause an interrupt when they are active if both:

- The I bit of the CC register is cleared.
- The corresponding enable bit is set in the control register.

If any of these two conditions is false, the interrupt is latched and thus remains pending.

Clearing an interrupt request is done by:

- Writing “0” to the corresponding bit in the status register or
- Access to the status register while the flag is set followed by a read or write of an associated register.

Note: The clearing sequence resets the internal latch. A pending interrupt (that is, waiting for being enabled) will therefore be lost if the clear sequence is executed.

Figure 14. Interrupt processing flowchart

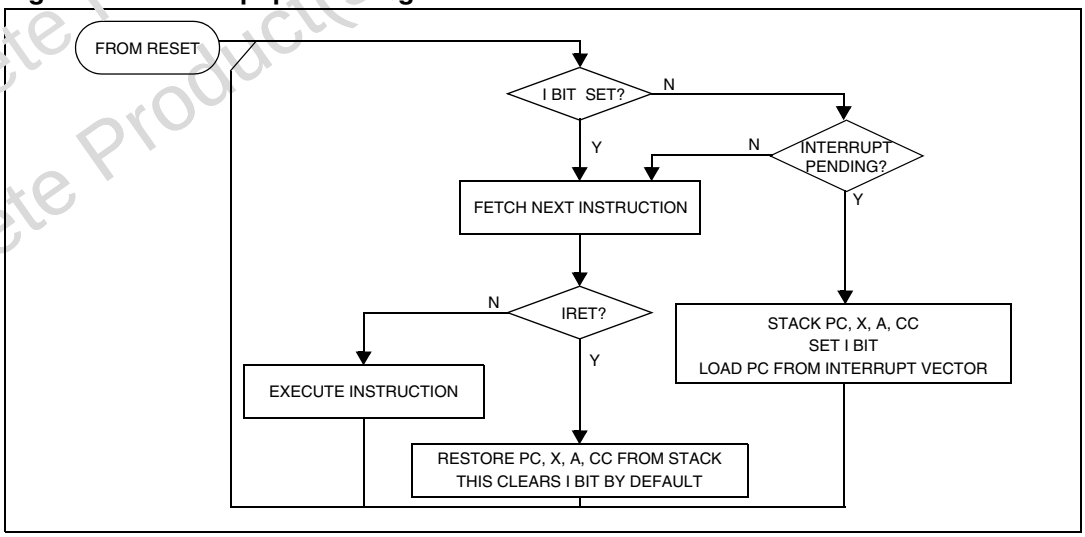


Table 9. Interrupt mapping

N°	Source block	Description	Register label	Priority order	Exit from Halt	Address vector
	RESET	Reset	N/A	Highest priority	yes	FFFEh-FFFFh
	TRAP	Software interrupt			no	FFFCh-FFFDh
0	AWU	Auto-wakeup interrupt	AWUCSR		yes(1)	FFFAh-FFFBh
1	ei0	External interrupt 0	N/A		yes	FFF8h-FFF9h
2	ei1	External interrupt 1				FFF6h-FFF7h
3	ei2	External interrupt 2				FFF4h-FFF5h
4		Not used			no	FFF2h-FFF3h
5	ei3	External interrupt 3			yes	FFF0h-FFF1h
6 2)	ei4 2)	External interrupt 4 2)			no(2)	FFEEh-FFEFh
7	SI	AVD interrupt	SICSR		no	FFECh-FFEDh
8	AT TIMER	AT TIMER Output Compare Interrupt	PWMxCSR or ATCSR		no	FFEAh-FFEBh
9		AT TIMER Overflow Interrupt	ATCSR	Lowest priority	yes(3)	FFE8h-FFE9h
10	LITE TIMER	LITE TIMER Input Capture Interrupt	LTCSR		no	FFE6h-FFE7h
11		LITE TIMER RTC1 Interrupt	LTCSR		yes(3)	FFE4h-FFE5h
12		Not used			no	FFE2h-FFE3h
13		Not used			no	FFE0h-FFE1h

1. This interrupt exits the MCU from Auto-wakeup from Halt mode only.
2. This interrupt exits the MCU from Wait and Active-halt modes only. Moreover, IS4[1:0] = 01 is the only safe configuration to avoid spurious interrupt in Halt and AWUFH mode
3. These interrupts exit the MCU from Active-halt mode only.

7.3.1 External Interrupt Control register 1 (EICR1)

Reset value: 0000 0000 (00h)

7							0
0	0	IS21	IS20	IS11	IS10	IS01	IS00
Read/Write							

Bits 7:6 Reserved

Bits 5:4 **IS2[1:0]** *ei2 sensitivity*
These bits define the interrupt sensitivity for ei2 according to *Table 10*.

Bits 3:2 **IS1[1:0]** *ei1 sensitivity*
These bits define the interrupt sensitivity for ei1 according to *Table 10*.

Bits 1:0 **IS0[1:0]** *ei0 sensitivity*
These bits define the interrupt sensitivity for ei0 according to *Table 10*.

Note: 1 These 8 bits can be written only when the I bit in the CC register is set.

2 Changing the sensitivity of a particular external interrupt clears this pending interrupt. This can be used to clear unwanted pending interrupts. Refer to Section : External interrupt function.

7.3.2 External Interrupt Control register 2 (EICR2)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	IS41	IS40	IS31	IS30
Read/Write							

Bits 7:4 Reserved

Bits 3:2 **IS4[1:0]** *ei4 sensitivity*
These bits define the interrupt sensitivity for ei1 according to *Table 10*.

Bits 1:0 **IS3[1:0]** *ei3 sensitivity*
These bits define the interrupt sensitivity for ei0 according to *Table 10*.

Note: 1 These 8 bits can be written only when the I bit in the CC register is set.

2 Changing the sensitivity of a particular external interrupt clears this pending interrupt. This can be used to clear unwanted pending interrupts. Refer to Section : External interrupt function.

3 IS4[1:0] = 01 is the only safe configuration to avoid spurious interrupt in Halt and AWUFH modes.

Table 10. Interrupt sensitivity bits

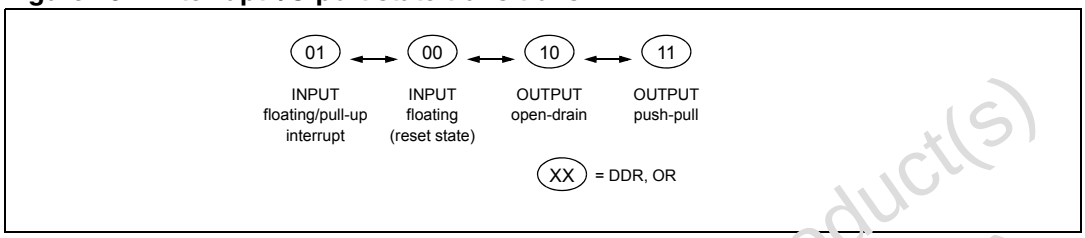
ISx1	ISx0	External interrupt sensitivity
0	0	Falling edge & low level
0	1	Rising edge only
1	0	Falling edge only
1	1	Rising and falling edge

9.6 I/O port implementation

The hardware implementation on each I/O port depends on the settings in the DDR and OR registers and specific feature of the I/O port such as ADC Input or true open drain.

Switching these I/O ports from one state to another should be done in a sequence that prevents unwanted side effects. Recommended safe transitions are illustrated in *Figure 29*. Other transitions are potentially risky and should be avoided, since they are likely to present unwanted side-effects such as spurious interrupt generation.

Figure 29. Interrupt I/O port state transitions



The I/O port register configurations are summarized in *Table 22*

Table 22. Port configuration

Port	Pin name	Input (DDR=0)		Output (DDR=1)	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA0:2, PA4:5	floating	pull-up interrupt	open drain	push-pull
	PA3	-	-	open drain	push-pull

After reset, to configure PA3 as a general purpose output, the application has to program the MUXCR0 and MUXCR1 registers. See *Section 6.5: Register description on page 37*

Table 23. I/O port register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0000h	PADR Reset value	MSB 0	0	0	0	0	0	0	LSB 0
0001h	PADDR Reset value	MSB 0	0	0	0	1	0	0	LSB 0
0002h	PAOR Reset value	MSB 0	0	0	0	0	0	1	LSB 0

PWM frequency and duty cycle

The PWM signal frequency (f_{PWM}) is controlled by the counter period and the ATR register value.

$f_{PWM} = f_{COUNTER} / (4096 - ATR)$

Following the above formula, if f_{CPU} is 8 MHz, the maximum value of f_{PWM} is 4 MHz (ATR register value = 4094), and the minimum value is 2 kHz (ATR register value = 0).

Note: The maximum value of ATR is 4094 because it must be lower than the DCR value which must be 4095 in this case.

At reset, the counter starts counting from 0.

Software must write the duty cycle value in the DCR0H and DCR0L preload registers. The DCR0H register must be written first. See caution below.

When a upcounter overflow occurs (OVF event), the ATR value is loaded in the upcounter, the preloaded Duty cycle value is transferred to the Duty Cycle register and the PWM0 signal is set to a high level. When the upcounter matches the DCRx value the PWM0 signals is set to a low level. To obtain a signal on the PWM0 pin, the contents of the DCR0 register must be greater than the contents of the ATR register.

The polarity bit can be used to invert the output signal.

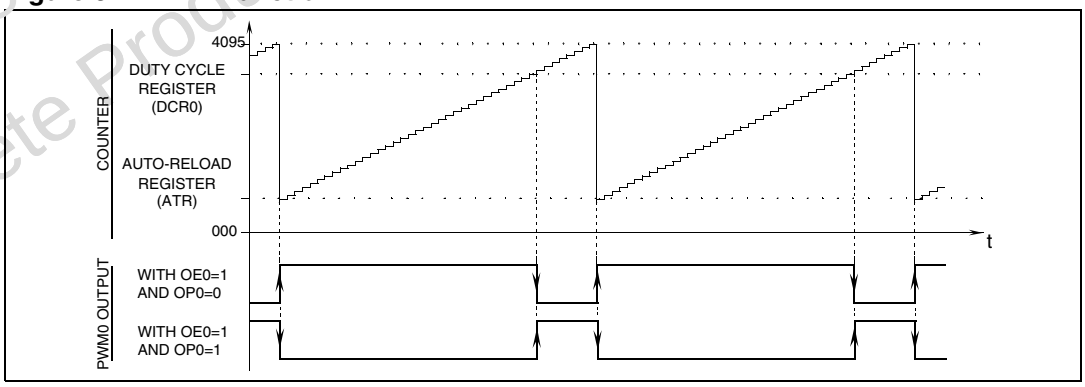
The maximum available resolution for the PWM0 duty cycle is:

Resolution = 1 / (4096 - ATR)

Note: To get the maximum resolution (1/4096), the ATR register must be 0. With this maximum resolution and assuming that DCR=ATR, a 0% or 100% duty cycle can be obtained by changing the polarity.

Caution: As soon as the DCR0H is written, the compare function is disabled and will start only when the DCR0L value is written. If the DCR0H write occurs just before the compare event, the signal on the PWM output may not be set to a low level. In this case, the DCRx register should be updated just after an OVF event. If the DCR and ATR values are close, then the DCRx register should be updated just before an OVF event, in order not to miss a compare event and to have the right signal applied on the PWM output.

Figure 34. PWM function



12 Electrical characteristics

12.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

12.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25 °C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean+3Σ).

12.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25 °C, V_{DD}=5 V (for the 4.5 V≤V_{DD}≤5.5 V voltage range), V_{DD}=3.75 V (for the 3 V≤V_{DD}≤4.5 V voltage range) and V_{DD}=2.7 V (for the 2.4 V≤V_{DD}≤3 V voltage range). They are given only as design guidelines and are not tested.

12.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

12.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 37*.

Figure 37. Pin loading conditions

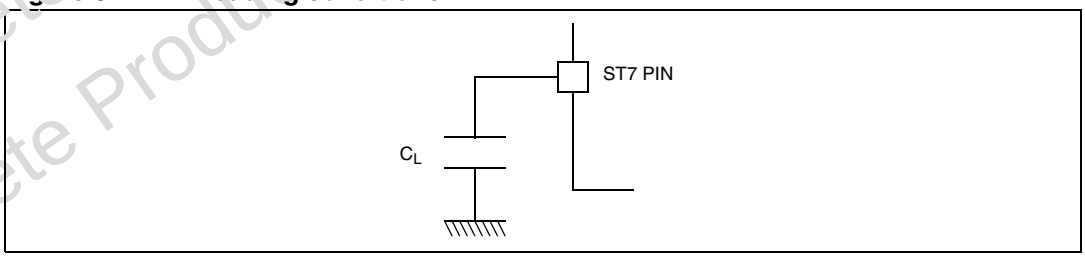


Table 44. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	75	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any standard I/O and control pin	20	
	Output current sunk by any high sink I/O pin	40	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$ (2)(3)	Injected current on $\overline{RESET}$ pin	± 5	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(4)	± 20	

1. All power (V_{DD}) and ground (V_{SS}) lines must always be connected to the external supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. In particular, it induces leakage currents throughout the device including the analog inputs. To avoid undesirable effects on the analog functions, care must be taken:
- Analog input pins must have a negative injection less than 0.8 mA (assuming that the impedance of the analog voltage is lower than the specified limits)
- Pure digital pins must have a negative injection less than 1.6 mA. In addition, it is recommended to inject the current as far as possible from the analog input pins.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterisation with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 45. Thermal characteristics

Symbol	Ratings	value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see *Section 13: Package characteristics*)		

12.3 Operating conditions

12.3.1 General operating conditions

T_A = -40 to +125 °C unless otherwise specified.

Table 46. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	f_{CPU} = 4 MHz max.	2.4	5.5	V
		f_{CPU} = 8 MHz max.	3.3	5.5	
f_{CPU}	CPU clock frequency	3.3 V≤ V_{DD}≤5.5 V	up to 8		MHz
		2.4 V≤V_{DD}<3.3 V	up to 4		

12.3.3 Auxiliary voltage detector (AVD) thresholds

T_A = –40 to 125°C, unless otherwise specified.

Table 48. Operating characteristics with AVD(1)

Symbol	Parameter	Conditions	Min (2)	Typ (2)	Max (2)	Unit
$V_{IT+(AVD)}$	1 => 0 AVDF flag toggle threshold (V_{DD} rise)	High threshold Med. threshold Low threshold	4.0 3.4 2.6	4.4 3.7 2.9	4.8 4.1 3.2	V
$V_{IT-(AVD)}$	0 => 1 AVDF flag toggle threshold (V_{DD} fall)	High threshold Med. threshold Low threshold	3.9 3.3 2.5	4.3 3.6 2.8	4.7 4.0 3.1	
V_{hys}	AVD voltage threshold hysteresis	$V_{IT+(AVD)}$-$V_{IT-(AVD)}$		150		mV

1. Refer to *Section : Monitoring the VDD main supply*.
2. Not tested in production, guaranteed by characterization.

Table 49. Voltage drop between AVD flag set and LVD reset generation

Parameter	Min (1)	Typ (1)	Max (1)	Unit
AVD med. threshold - AVD low. threshold	800	850	950	mV
AVD high. threshold - AVD low threshold	1400	1450	1550	
AVD high. threshold - AVD med. threshold	600	650	750	
AVD low threshold - LVD low threshold	100	200	250	
AVD med. threshold - LVD low threshold	950	1050	1150	
AVD med. threshold - LVD med. threshold	250	300	400	
AVD high. threshold - LVD low threshold	1600	1700	1800	
AVD high. threshold - LVD med. threshold	900	1000	1050	

1. Not tested in production, guaranteed by characterization.

12.3.4 Internal RC oscillator

To improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100 nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

Internal RC oscillator calibrated at 5.0 V

The ST7 internal clock can be supplied by an internal RC oscillator (selectable by option byte).

12.4.2 Internal RC oscillator supply current characteristics

Table 53. Internal RC oscillator supply current

Symbol	Parameter	Conditions		Min	Typ	Max (1)	Unit
I_{DD}	Supply current in Run mode (2)	RC oscillator calibrated at 5.0V	T_A=25 °C, int RC = 4 MHz		3.2	5.5	mA
			T_A=25 °C, int RC = 8 MHz		5.7	8.5	
			T_A=25 °C, AWU RC		0.13	0.2	
	Supply current in Wait mode (3)		T_A=25 °C, int RC = 4 MHz		1.5	3.0	
			T_A=25 °C, int RC = 8 MHz		1.9	4.5	
	Supply current in Slow mode (4)		T_A=25 °C, int RC/32 = 250 kHz		1.3	2.0	
	Supply current in Slow-Wait mode (5)		T_A=25 °C, int RC/32 = 250 kHz		1.1	1.8	
	Supply current in Active-halt mode				0.8	1.25	
I_{DD}	Supply current in Run mode (2)	RC oscillator calibrated at 3.3 V	T_A=25 °C, int RC = 4 MHz		2.0	3.0	mA
			T_A=25 °C, int RC = 2 MHz		1.3	2.0	
			T_A=25 °C, AWU RC		0.1	0.18	
	Supply current in Wait mode (3)		T_A=25 °C, int RC = 4 MHz		1.0	1.6	
			T_A=25 °C, int RC = 2 MHz		0.9	1.5	
	Supply current in Slow mode (4)		T_A=25 °C, int RC/32 = 250 kHz		0.95	1.5	
	Supply current in Slow-Wait mode (5)		T_A=25 °C, int RC/32 = 250 kHz		0.85	1.4	
	Supply current in Active-halt mode				0.8	1.3	

1. Data based on characterization results, not tested in production.
2. CPU running with memory access, all I/O pins in input mode with a static value at VDD or VSS (no load), all peripherals in reset state; CPU clock provided by the internal RC, LVD disabled.
3. All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; CPU clock provided by the internal RC, LVD disabled.
4. Slow mode selected with f_{CPU} based on f_{OSC} divided by 32. All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; CPU clock provided by the internal RC, LVD disabled.
5. Slow-Wait mode selected with f_{CPU} based on f_{OSC} divided by 32. All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; CPU clock provided by the internal RC, LVD disabled.

12.8 I/O port pin characteristics

12.8.1 General characteristics

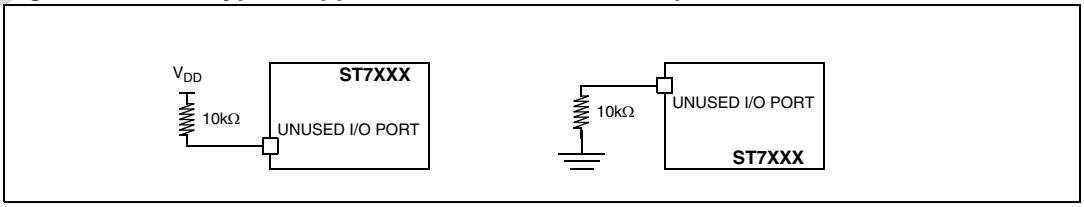
Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 63. General characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage	-40°C to 125°C				$0.3V_{DD}$	V
V_{IH}	Input high level voltage			$0.7V_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis(1)				400		mV
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$				±1	µA
I_S	Static current consumption induced by each floating input pin(2)	Floating input mode			100		
R_{PU}	Weak pull-up equivalent resistor(3) (4)	$V_{IN}=V_{SS}$	V_{DD}=5 V	80	120	170	kΩ
			V_{DD}=3 V		200(1)		
C_{IO}	I/O pin capacitance				5		pF
$t_{f(IO)out}$	Output high to low level fall time 1)	C_L=50 pF Between 10% and 90%			25		ns
$t_{r(IO)out}$	Output low to high level rise time 1)				25		
$t_{w(IT)in}$	External interrupt pulse time(5)			1			t_{CPU}

1. Data based on characterization results, not tested in production.
2. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see *Figure 48*). Static peak current value taken at a fixed V_{IN} value, based on design simulation and technology characteristics, not tested in production. This value depends on V_{DD} and temperature values.
3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 49*).
4. R_{PU} not applicable on PA3 because it is multiplexed on $\overline{\text{RESET}}$ pin
5. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 48. Two typical applications with unused I/O pin



1. **Caution**: During normal operation the ICCCLK pin must be pulled- up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering I^2C mode unexpectedly during a reset.
2. I/O can be left unconnected if it is configured as output (0 or 1) by the software. This has the advantage of greater EMC robustness and lower cost.

Figure 67. 8-pin plastic dual in-line package, 300-mil width package outline

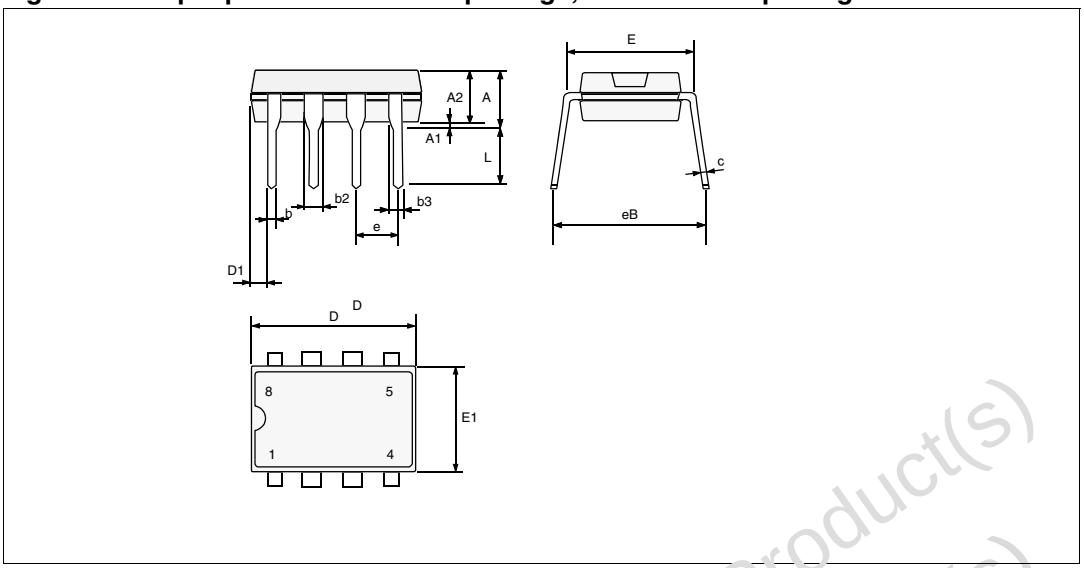


Table 72. 8-pin plastic dual in-line package, 300-mil width package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			5.33			0.2100
A1	0.38			0.0150		
A2	2.92	3.30	4.95	0.1150	0.1300	0.1950
b	0.36	0.46	0.56	0.0140	0.0180	0.0220
b2	1.14	1.52	1.78	0.0450	0.0600	0.0700
b3	0.76	0.99	1.14	0.0300	0.0390	0.0450
c	0.20	0.25	0.36	0.0080	0.0100	0.0140
D	9.02	9.27	10.16	0.3550	0.3650	0.4000
D1	0.13			0.0050		
e		2.54			0.1000	
eB			10.92			0.4300
E	7.62	7.87	8.26	0.3000	0.3100	0.3250
E1	6.10	6.35	7.11	0.2400	0.2500	0.2800
L	2.92	3.30	3.81	0.1150	0.1300	0.1500
	Number of pins					
N	8					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 79. Supported order codes [1] (continued)

Order code	Program memory (bytes)	RAM (bytes)	ADC	Temperature range	Package	Conditioning
ST7PLUSA5B6	1 Kbyte FASTROM	128	10-bit	-40°C +85°C	DIP8	Tube
ST7PLUSA5M6			10-bit		SO8	Tube
ST7PLUSA5M6TR			10-bit		SO8	Tape & Reel
ST7PLUSA5U6			10-bit		DFN8	Tray
ST7PLUSA5U6TR			10-bit		DFN8	Tape & Reel
ST7PLUSA2B3	1 Kbyte FLASH	128	-	-40°C +125°C	DIP8	Tube
ST7PLUSA2M3			-		SO8	Tube
ST7PLUSA2M3TR			-		SO8	Tape & Reel
ST7PLUSA2U3TR			-		DFN8	Tape & Reel
ST7PLUSA5B3	1 Kbyte FLASH	128	10-bit	-40°C +125°C	DIP8	Tube
ST7PLUSA5M3			10-bit		SO8	Tube
ST7PLUSA5M3TR			10-bit		SO8	Tape & Reel
ST7PLUSA5U3			10-bit		DFN8	Tray
ST7PLUSA5U3TR			10-bit		DFN8	Tape & Reel
ST7PLUSA2B3	1 Kbyte FASTROM	128	-	-40°C +125°C	DIP8	Tube
ST7PLUSA2M3			-		SO8	Tube
ST7PLUSA2M3TR			-		SO8	Tape & Reel
ST7PLUSA2U3TR			-		DFN8	Tape & Reel
ST7PLUSA5B3	1 Kbyte FASTROM	128	10-bit	-40°C +125°C	DIP8	Tube
ST7PLUSA5M3			10-bit		SO8	Tube
ST7PLUSA5M3TR			10-bit		SO8	Tape & Reel
ST7PLUSA5U3			10-bit		DFN8	Tray
ST7PLUSA5U3TR			10-bit		DFN8	Tape & Reel

1. Contact ST sales office for product availability.
2. For development or tool prototyping purposes only, not orderable in production quantities.

14.3 Development tools

Development tools for the ST7 microcontrollers include a complete range of hardware systems and software tools from STMicroelectronics and third-party tool suppliers. The range of tools includes solutions to help you evaluate microcontroller peripherals, develop and debug your application, and program your microcontrollers.

14.3.1 Starter kits

ST offers complete, affordable **starter kits**. Starter kits are complete, affordable hardware/software tool packages that include features and samples to help you quickly start developing your application.

14.3.2 Development and debugging tools

Application development for ST7 is supported by fully optimizing **C Compilers** and the **ST7 Assembler-Linker** toolchain, which are all seamlessly integrated in the ST7 integrated development environments in order to facilitate the debugging and fine-tuning of your application. The Cosmic C Compiler is available in a free version that outputs up to 16 Kbytes of code.

The range of hardware tools includes full-featured **ST7-EMU3 series emulators,** cost effective **ST7-DVP3 series emulators** and the low-cost **RLink** in-circuit debugger/programmer. These tools are supported by the **ST7 Toolset** from STMicroelectronics, which includes the ST7VD7 integrated development environment (IDE) with high-level language debugger, editor, project manager and integrated programming interface.

14.3.3 Programming tools

During the development cycle, the **ST7-DVP3** and **ST7-EMU3 series emulators** and the **RLink** provide in-circuit programming capability for programming the Flash microcontroller on your application board.

ST also provides a low-cost dedicated in-circuit programmer, the **ST7-STICK**, as well as **ST7 Socket Boards** which provide all the sockets required for programming any of the devices in a specific ST7 sub-family on a platform that can be used with any tool with in-circuit programming capability for ST7.

For production programming of ST7 devices, ST's third-party tool partners also provide a complete range of gang and automated programming solutions, which are ready to integrate into your production environment.

14.3.4 Order codes for development and programming tools

Table 80 below lists the ordering codes for the ST7LITEUSx development and programming tools. For additional ordering codes for spare parts and accessories, refer to the online product selector at www.st.com/mcu.

Table 81. ST7 application notes (continued)

Identification	Description
AN1044	Multiple interrupt sources management for ST7 MCUs
AN1045	ST7 S/W implementation of I²C bus master
AN1046	UART emulation software
AN1047	Managing reception errors with the ST7 SCI peripherals
AN1048	ST7 software LCD driver
AN1078	PWM duty cycle switch implementing true 0% & 100% duty cycle
AN1082	Description of the ST72141 motor control peripherals registers
AN1083	ST72141 BLDC motor control software and flowchart example
AN1105	ST7 pCAN peripheral driver
AN1129	PWM management for BLDC motor drives using the ST72141
AN1130	An introduction to sensorless brushless DC motor drive applications with the ST72141
AN1148	Using the ST7263 for designing a USB mouse
AN1149	Handling Suspend mode on a USB mouse
AN1180	Using the ST7263 Kit to implement a USB game pad
AN1276	BLDC motor start routine for the ST72141 microcontroller
AN1321	Using the ST72141 motor control MCU in sensor mode
AN1325	Using the ST7 USB low-speed firmware V4.x
AN1445	Emulated 16-bit slave SPI
AN1475	Developing an ST72x5x mass storage application
AN1504	Starting a PWM signal directly at high level using the ST7 16-bit timer
AN1602	16-bit timing operations using ST7262 or ST7263B ST7 USB MCUs
AN1633	Device firmware upgrade (DFU) implementation in ST7 non-USB applications
AN1712	Generating a high resolution sinewave using ST7 PWMART
AN1713	SMBus slave driver for ST7 I2C peripherals
AN1753	Software UART using 12-bit ART
AN1947	ST7MC PMAC sine wave motor control software library
General purpose	
AN1476	Low cost power supply for home appliances
AN1526	ST7FLITE0 quick reference note
AN1709	EMC design for ST Microcontrollers
AN1752	ST72324 quick reference note
Product evaluation	
AN 910	Performance benchmarking
AN 990	ST7 benefits vs industry standard

Table 81. ST7 application notes (continued)

Identification	Description
AN 987	ST7 serial test controller programming
AN 988	Starting with ST7 assembly tool chain
AN1039	ST7 math utility routines
AN1071	Half duplex USB-to-serial bridge using the ST72611 USB microcontroller
AN1106	Translating assembly code from HC05 to ST7
AN1179	Programming ST7 Flash microcontrollers in remote ISP mode (In-situ programming)
AN1446	Using the ST72521 emulator to debug an ST72324 target application
AN1477	Emulated data EEPROM with Xflash memory
AN1527	Developing a USB smartcard reader with ST7SCR
AN1575	On-board programming methods for XFLASH and HDFLASH ST7 MCUs
AN1576	In-application programming (IAP) drivers for ST7 HDFLASH or XFLASH MCUs
AN1577	Device firmware upgrade (DFU) implementation for ST7 USB applications
AN1601	Software implementation for ST7DALI-EVAL
AN1603	Using the ST7 USB device firmware upgrade development kit (DFU-DK)
AN1635	ST7 customer ROM code release information
AN1754	Data logging program for testing ST7 applications via I^2C
AN1796	Field updates for FLASH based ST7 applications using a PC comm port
AN1900	Hardware implementation for ST7DALI-EVAL
AN1904	ST7MC three-phase AC induction motor control software library
AN1905	ST7MC three-phase BLDC motor control software library
System optimization	
AN1711	Software techniques for compensating ST7 ADC errors
AN1827	Implementation of SIGMA-DELTA ADC with ST7FLITE05/09
AN2009	PWM Management for 3-phase BLDC motor drives using the ST7FMC
AN2030	Back EMF detection during PWM on time by ST7MC

Table 82. Document revision history (continued)

Date	Revision	Changes
18-Sep-06	3	Modified description of AVD[1:0] bits in the AVDTRH register in *Section 7.4.4* Modified description of CNTR[11:0] bits in *Section 10.2.6: Register description* Modified values in *Table 44* LVD and AVD tables updated, *Table 47*, *Table 48* and *Table 49* Internal RC oscillator data modified in *Table 50* and new table added *Table 51* Typical data in *Table 54* (on chip peripherals) modified EMC characteristics updated, *Section 12.7* R_{PU} data corrected in *Table 63* including additional notes Output driving current table updated, *Table 64* R_{ON} data corrected in *Table 65*. Modified ADC accuracy tables in *Section 12.10* *Section :* updated Errata sheet removed from document Notes modified for low voltage detector *Section 7.4.1* Notes updated in *Section 4.4* (I^2C Interface) Thermal characteristics table updated, *Table 74* Modified option list on *Section 14.2: Ordering information* Modified *Section 14.3: Development tools* Modified text in *Section :*
26-Jan-07	4	Added -40°C to 125°C temperature range Modified note on ei4 in *Table 9. Interrupt mapping* Added note 3 to *Section 7.4.2: External Interrupt Control register 2 (EICR2)* Added *Figure 41* and *Figure 40* Added a note to LVDRF in *Section 7.4.4: Register description* *Section 6.4.1: Introduction* Modified *Table 47* and *Table 48* Modified *Table 50*Updated *Table 53* Updated *Table 64* Modified R_{AIN} and ADC accuracy tables in *Section 12.10: ADC characteristics* Modified *Table 80* Modified *Table 79* Modified option list on *Figure 69: Option list*
06-Feb-2009	5	Document reformatted. Replaced ST7ULTRALITE by ST7LITEUS2 and ST7LITEUS5. Removed limitations in user and in I^2C mode from *Section 15: Known limitations*, and added *External interrupt 2 (ei2)*. Added MCO on pin 3. Updated *Section 12.3.2: Operating conditions with low voltage detector (LVD)*, *Section 12.3.3: Auxiliary voltage detector (AVD) thresholds*, *Section 12.3.4: Internal RC oscillator*, *Section 12.4: Supply current characteristics*, and *Section 12.8.2: Output driving current characteristics*. Updated internal RC prescaler to add 500 KHz. Updated ECOPACK text in *Section 13.1: Package mechanical data*. Added PDIP16 silhouette on cover page, and updated *Table 73: 16-pin plastic dual in-line package, 300-mil width, package mechanical data* and *Figure 68: 16-pin plastic dual in-line package, 300-mil width, package outline*. Changed order codes to die A version in *Table 79: Supported order codes*. Removed soldering information section. Updated option list.

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