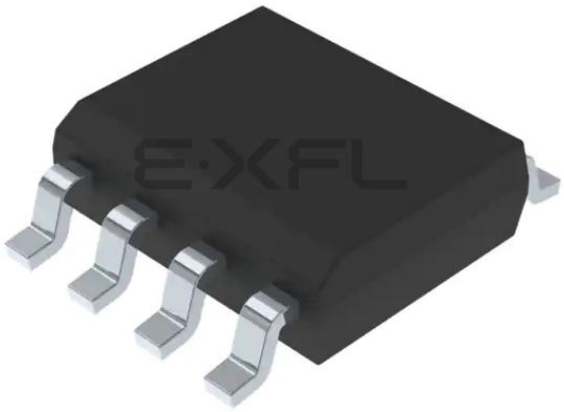

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What is "Embedded - Microcontrollers"?

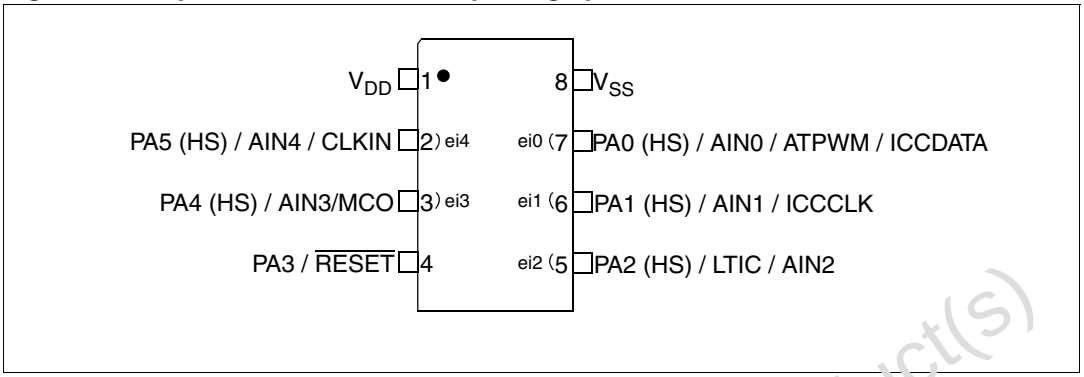
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fliteus5m3

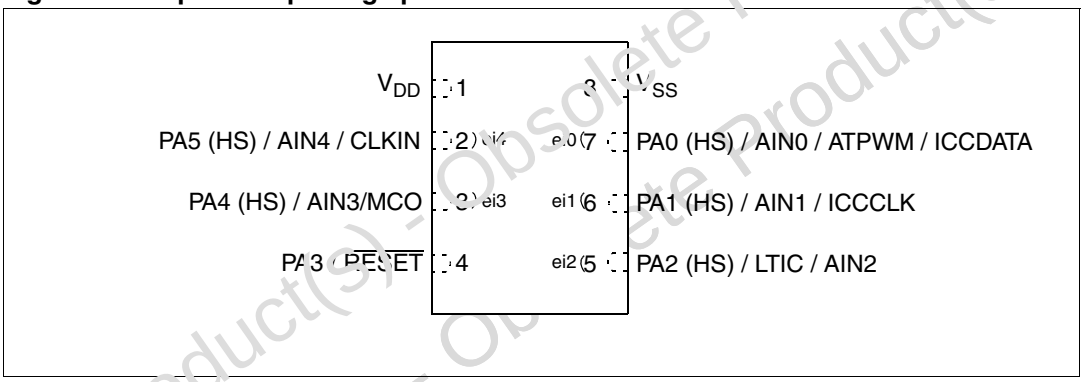
2 Pin description

Figure 2. 8-pin SO and Plastic DIP package pinout



1. HS: High sink capability.
2. eix : associated external interrupt vector

Figure 3. 8-pin DFN package pinout



1. HS: High sink capability.
2. eix : associated external interrupt vector

In flash devices, this protection is removed by reprogramming the option. In this case, program memory is automatically erased, and the device can be reprogrammed.

Readout protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the option list.

4.5.2 Flash Write/Erase protection

Write/erase protection, when set, makes it impossible to both overwrite and erase program memory. Its purpose is to provide advanced security to applications and prevent any change being made to the memory content.

Warning: Once set, Write/erase protection can never be removed. A write-protected flash device is no longer reprogrammable.

Write/erase protection is enabled through the FMP_W bit in the option byte.

4.6 Related documentation

For details on Flash programming and I^2C protocol, refer to the ST7 Flash programming reference manual and to the ST7 I^2C protocol reference manual.

5.3.5 Stack Pointer (SP)

Reset value: 00 FFh

15							8
0	0	0	0	0	0	0	0
Read/write							

7							0
1	1	SP5	SP4	SP3	SP2	SP1	SP0
Read/write							

The Stack Pointer is a 16-bit register which is always pointing to the next free location in the stack. It is then decremented after data has been pushed onto the stack and incremented before data is popped from the stack (see *Figure 8*).

Since the stack is 64 bytes deep, the 10 most significant bits are forced by hardware. Following an MCU Reset, or after a Reset Stack Pointer instruction (RSP), the Stack Pointer contains its reset value (the SP5 to SP0 bits are set) which is the stack higher address.

The least significant byte of the Stack Pointer (called S) can be directly accessed by a LD instruction.

Note: When the lower limit is exceeded, the Stack Pointer wraps around to the stack upper limit, without indicating the stack overflow. The previously stored information is then overwritten and therefore lost. The stack also wraps in case of an underflow.

The stack is used to save the return address during a subroutine call and the CPU context during an interrupt. The user may also directly manipulate the stack by means of the PUSH and POP instructions. In the case of an interrupt, the PCL is stored at the first location pointed to by the SP. Then the other registers are stored in the next locations as shown in *Figure 8*.

- When an interrupt is received, the SP is decremented and the context is pushed on the stack.
- On return from interrupt, the SP is incremented and the context is popped from the stack.

A subroutine call is located at two locations and an interrupt five locations in the stack area.

Bit 2 **RC_FLAG** *RC Selection*
This bit is set and cleared by hardware
0: No switch from RC to AWU requested
1: RC clock activated and temporization completed

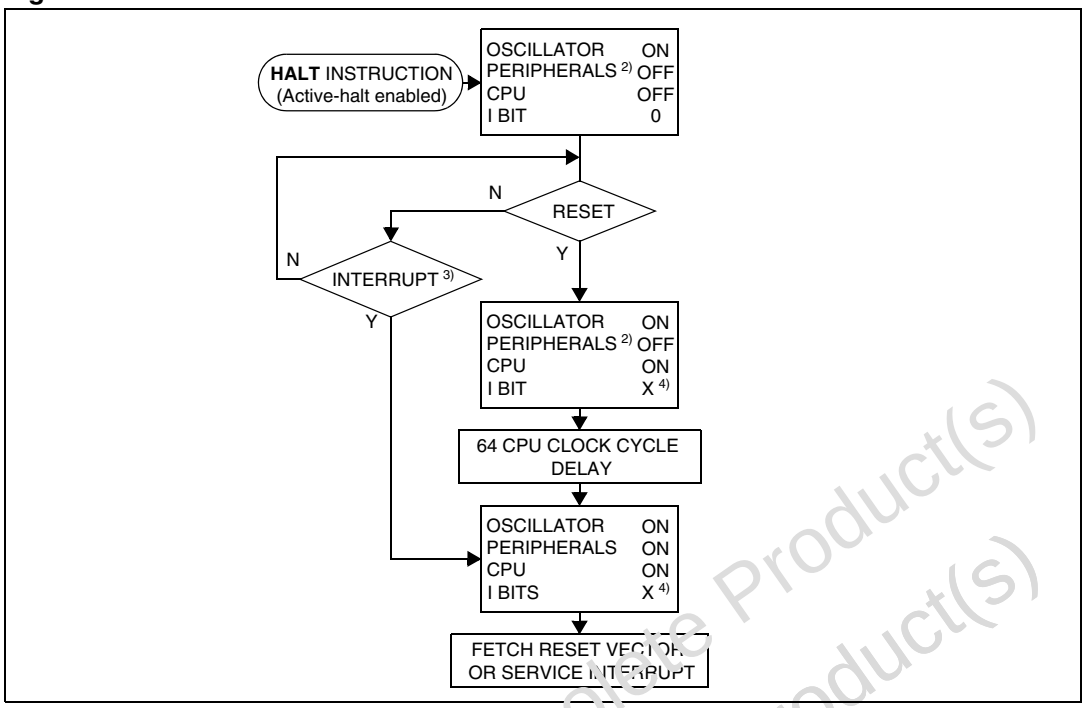
Bit 1 = Reserved, must be kept cleared.

Bit 0 = **RC/AWU** *RC/AWU Selection*
0: RC enabled
1: AWU enabled (default value)

Table 7. Clock register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0038h	MCCSR Reset value	0	0	0	0	0	0	MCO 0	SMS 0
0039h	RCCR reset value	CR9 1	CR8 1	CR7 1	CR6 1	CR5 1	CR4 1	CR3 1	CR2 1
003Ah	SICSR reset value	0	CR1	CR0	0	0	LVDRF x	AVDF 0	AVDIE 0
003Eh	AVDTHCR reset value	CK2 0	CK1 0	CK0 0	0	0	0	AVD1 1	AVD2 1
003Fh	CKCNTCSR reset value	0	0	0	0	AWU_FLAG 1	RC_FLAG 0	0	RC/AWU 1

Figure 22. Active-halt mode flowchart



1. This delay occurs only if the MCU exits Active-halt mode by means of a reset.
2. Peripherals clocked with an external clock source can still be active.
3. Only the Lite Timer RTC and AT Timer interrupts can exit the MCU from Active-halt mode.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I bit of the CC register is set during the interrupt routine and cleared when the CC register is popped.

8.4.2 Halt mode

The Halt mode is the lowest power consumption mode of the MCU. It is entered by executing the 'HALT' instruction when Active-halt mode is disabled.

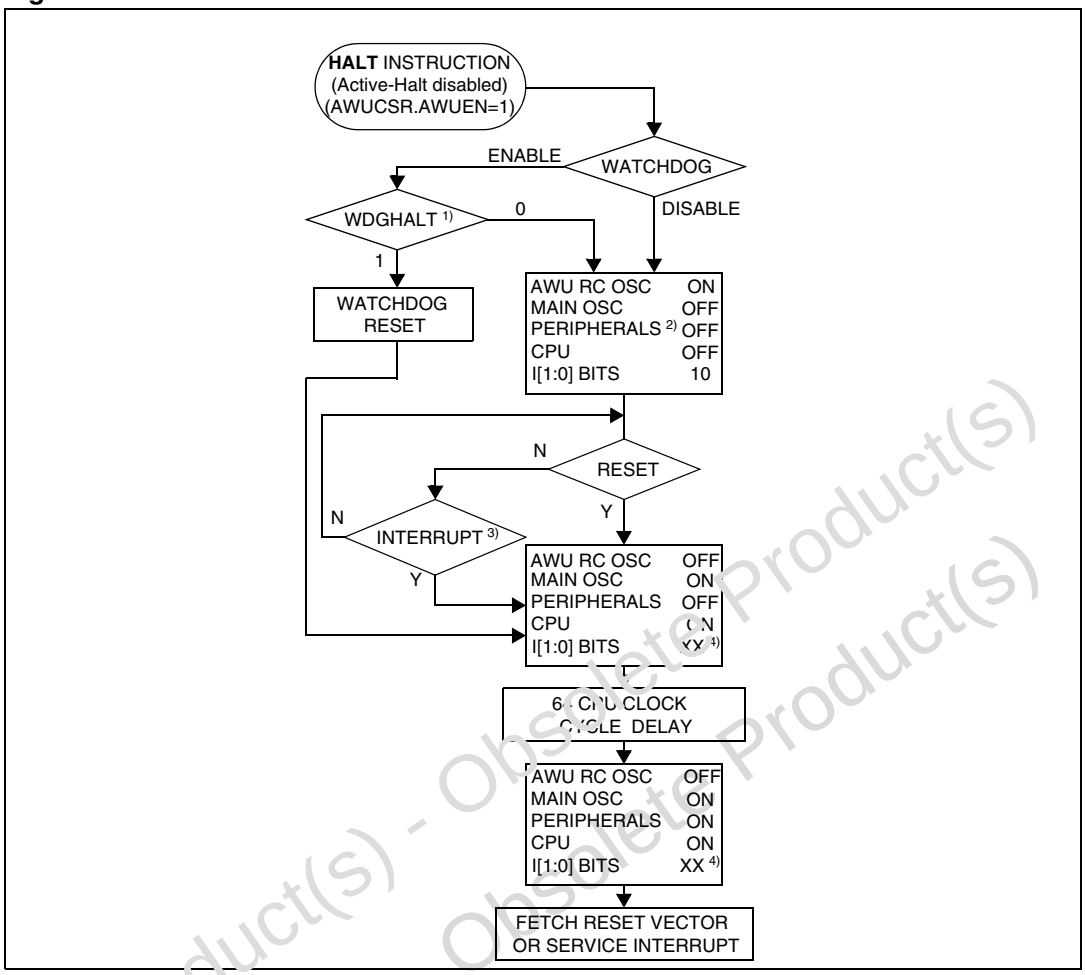
The MCU can exit Halt mode on reception of either a specific interrupt (see *Table 9: Interrupt mapping*) or a reset. When exiting Halt mode by means of a reset or an interrupt, the main oscillator is immediately turned on and the 64 CPU cycle delay is used to stabilize it. After the start up delay, the CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see *Figure 24*).

When entering Halt mode, the I bit in the CC register is forced to 0 to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes immediately.

In Halt mode, the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. All peripherals are not clocked except the ones which get their clock supply from another clock generator (such as an external or auxiliary oscillator).

The compatibility of watchdog operation with Halt mode is configured by the "WDGHALT" option bit of the option byte. The HALT instruction when executed while the watchdog system is enabled, can generate a watchdog reset (see *Section 14.1: Option bytes* for more details).

Figure 27. AWUFH mode flowchart



1. WDGHALT is an option bit. See option byte section for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only an AWUFH interrupt and some specific interrupts can exit the MCU from Halt mode (such as external interrupt). Refer to *Table 9: Interrupt mapping* for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

9 I/O ports

9.1 Introduction

The I/O port offers different functional modes:

- Transfer of data through digital inputs and outputs

and for specific pins:

- External interrupt generation
- Alternate signal input/output for the on-chip peripherals.

An I/O port contains up to 6 pins. Each pin (except PA3/$\overline{\text{RESET}}$) can be programmed independently as digital input (with or without interrupt generation) or digital output.

9.2 Functional description

Each port has 2 main registers:

- Data register (DR)
- Data Direction register (DDR)

and one optional register:

- Option register (OR)

Each I/O pin may be programmed using the corresponding register bits in the DDR and OR registers: bit X corresponding to pin X of the port. The same correspondence is used for the DR register.

The following description takes into account the OR register, (for specific ports which do not provide this register refer to the I/O Port Implementation section). The generic I/O block diagram is shown in *Figure 28*.

9.2.1 Input modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Different input modes can be selected by software through the OR register.

Note: 1 Writing the DR register modifies the latch value but does not affect the pin status.

2 PA3 cannot be configured as input.

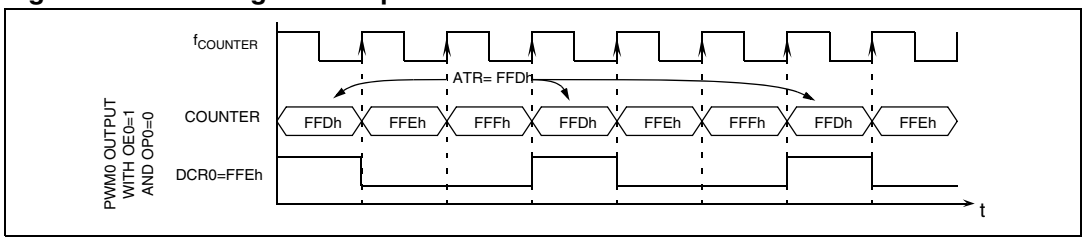
External interrupt function

When an I/O is configured as Input with Interrupt, an event on this I/O can generate an external interrupt request to the CPU.

Each pin can independently generate an interrupt request. The interrupt sensitivity is independently programmable using the sensitivity bits in the EICR register.

External interrupts are hardware interrupts. Fetching the corresponding interrupt vector automatically clears the request latch. Changing the sensitivity of a particular external interrupt clears this pending interrupt. This can be used to clear unwanted pending interrupts.

Figure 35. PWM signal example



Output compare mode

To use this function, the OE bit must be 0, otherwise the compare is done with the shadow register instead of the DCRx register. Software must then write a 12-bit value in the DCR0H and DCR0L registers. This value will be loaded immediately (without waiting for an OVF event).

The DCR0H must be written first, the output compare function starts only when the DCR0L value is written.

When the 12-bit upcounter (CNTR) reaches the value stored in the DCR0H and DCR0L registers, the CMPF0 bit in the PWM0CSR register is set and an interrupt request is generated if the CMPIE bit is set.

Note: The output compare function is only available for DCRx values other than 0 (reset value).

Caution: At each OVF event, the DCRx value is written in a shadow register, even if the DCR0L value has not yet been written (in this case, the shadow register will contain the new DCR0H value and the old DCR0L value), then:

- If OE=1 (PWM mode): the compare is done between the timer counter and the shadow register (and not DCRx)
- If OE=0 (OCMP mode): the compare is done between the timer counter and DCRx. There is no PWM signal.
  The compare between DCRx or the shadow register and the timer counter is locked until DCR0L is written.

10.2.4 Low power modes

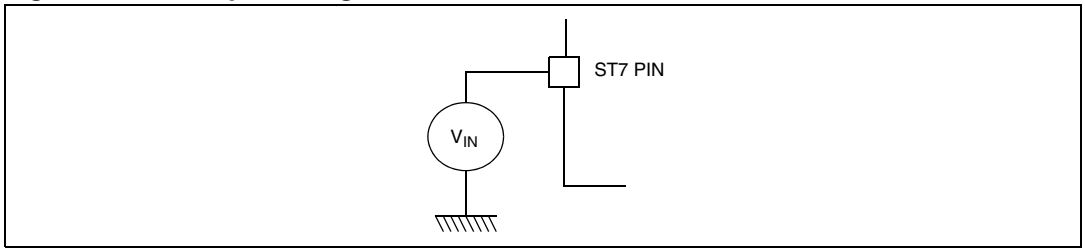
Table 27. Description of low power modes

Mode	Description
Slow	The input frequency is divided by 32
Wait	No effect on AT timer
Active-halt	AT timer halted except if CK0=1, CK1=0 and OVFIE=1
Halt	AT timer halted

12.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 38*.

Figure 38. Pin input voltage



12.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. Directly connecting the I/O pins to V_{DD} or V_{SS} could damage the device if an unexpected change of the I/O configuration occurs (for example due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 10 kΩ for I/Os). Unused I/O pins must be tied in the same way to V_{DD} or V_{SS} according to their reset configuration

Table 43. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
V_{DD} - V_{SS}	Supply voltage	7.0	V
V_{IN}	Input voltage on any pin(1)	V_{SS}-0.3 to V_{DD}+0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *Section 12.7.2*	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	see *Section 12.7.2*	

1. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

Figure 40. Typical accuracy with RCCR=RCCR0 vs V_{DD}= 2.4-6.0 V and temperature

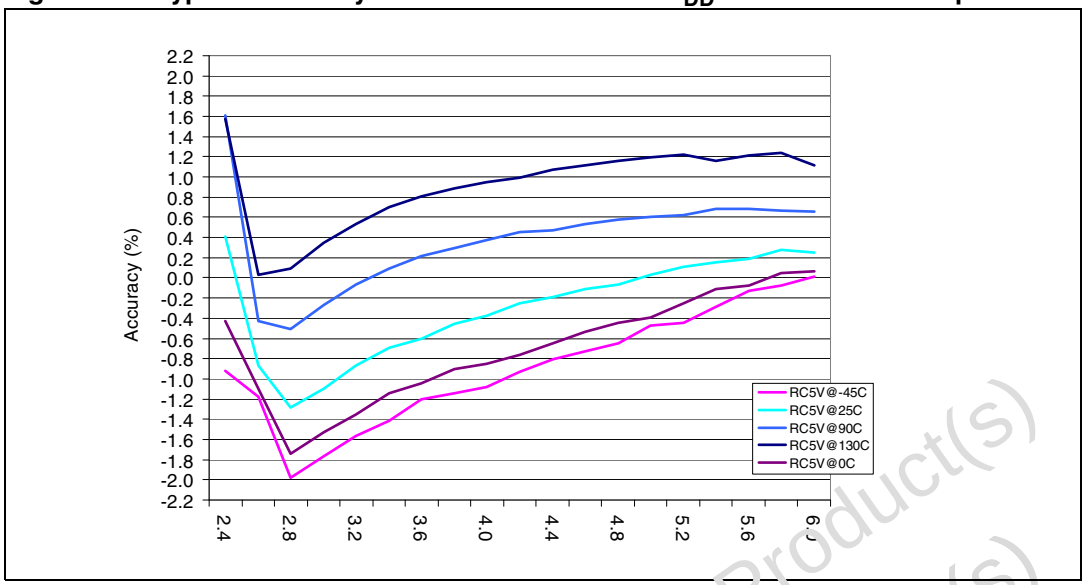


Figure 41. Typical accuracy with RCCR=RCCR1 vs V_{DD}= 2.4-6.0V and temperature

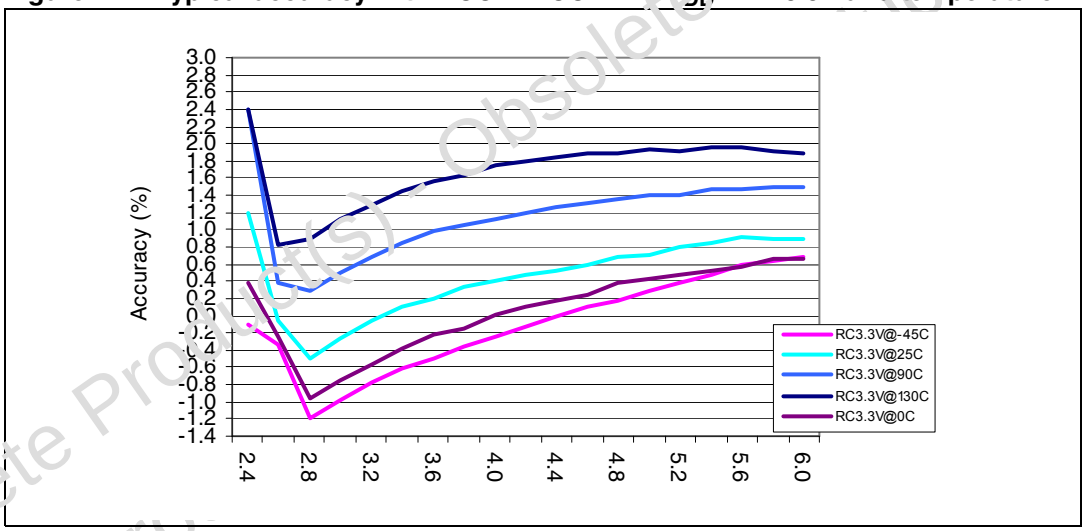


Figure 42. Typical I_{DD} in run mode vs. internal clock frequency and V_{DD}

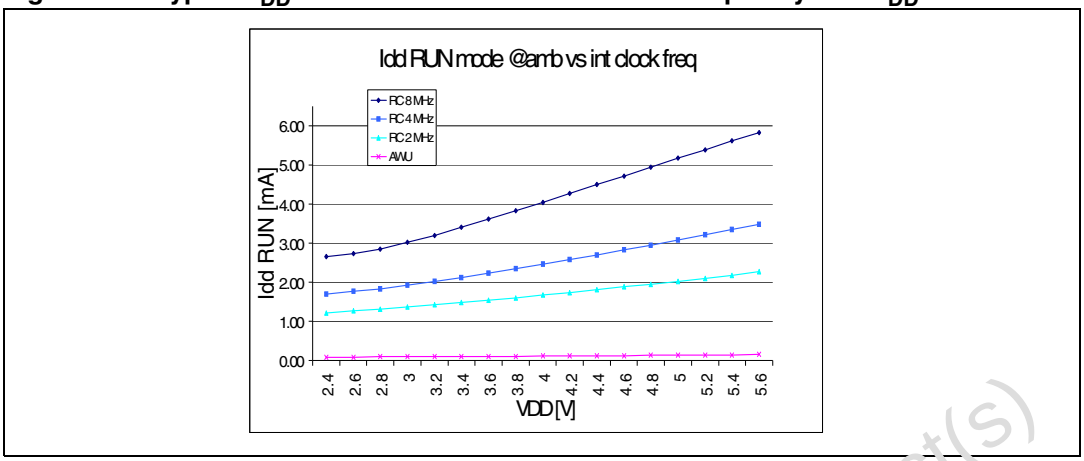


Figure 43. Typical I_{DD} in WFI mode vs. internal clock frequency and V_{DD}

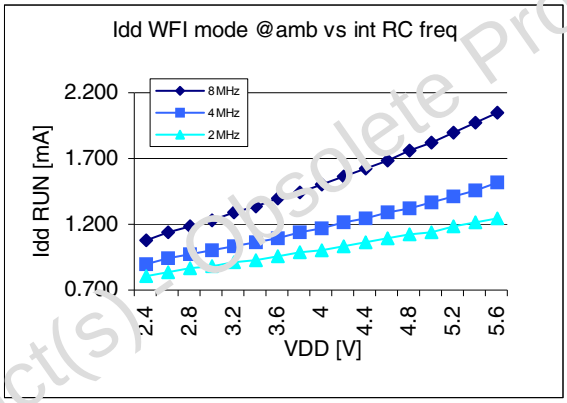
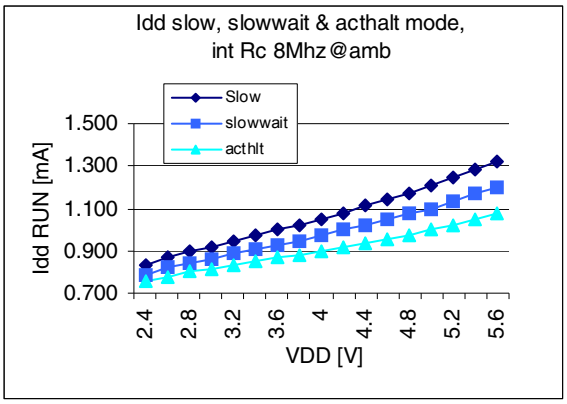


Figure 44. Typical I_{DD} in Slow, Slow-wait and Active-halt mode vs V_{DD} & int RC = 8 MHz



12.4.3 On-chip peripherals

Table 54. On-chip peripheral characteristics

Symbol	Parameter	Conditions		Typ (1)	Unit
$I_{DD(AT)}$	12-bit auto-reload timer supply current (2)	f_{CPU} = 4 MHz	V_{DD}= 3.0 V	15	µA
		f_{CPU} = 8 MHz	V_{DD}= 5.0 V	30	
$I_{DD(ADC)}$	ADC supply current when converting (3)	f_{ADC} = 2 MHz	V_{DD}= 3.0 V	450	
		f_{ADC} = 4 MHz	V_{DD}= 5.0 V	750	

1. Not tested in production, guaranteed by characterization.
2. Data based on a differential I_{DD} measurement between reset configuration (timer stopped) and the timer running in PWM mode at f_{cpu} = 8 MHz.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions with amplifier off.

12.5 Clock and timing characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

Table 55. General timings

Symbol	Parameter(1)	Conditions	Min	Typ(2)	Max	Unit
$t_{c(INST)}$	Instruction cycle time	f_{CPU}=8 MHz	2	3	12	t_{CPU}
			250	375	1500	ns
$t_{v(IT)}$	Interrupt reaction time(3) $t_{v(IT)} = \Delta t_{c(INST)} + 10$	f_{CPU}=8 MHz	10		22	t_{CPU}
			1.25		2.75	µs

1. Data based on characterization. Not tested in production.
2. Data based on typical application software.
3. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

Table 56. Auto-wakeup RC oscillator

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage Range		2.4	5.0	5.5	V
Operating Temperature Range		-40	25	125	°C
Current Consumption(1)	Without prescaler	2.0	8.0	14.0	µA
Consumption(1)	AWU RC switched off		0		µA
Output Frequency(1)		20	33	60	kHz

1. Data guaranteed by design.

12.6 Memory characteristics

T_A = -40 to 125 °C, unless otherwise specified;

Table 57. RAM and Hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode [1]	Halt mode (or Reset)	1.6			V

Table 58. Flash Program memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage for Flash write/erase		2.4(1)		5.5	V
t_{prog}	Programming time for 1~32 bytes(2)	T_A=–40 to +125°C		5	10	ms
	Programming time for 1 kByte	T_A=+25°C		0.16	0.32	s
t_{RET}	Data retention(3)	T_A=+55°C(4)	20			years
N_{RW}	Write erase cycles	T_A=+25°C	10k(5)			cycles
I_{DD}	Supply current(6)	Read / Write / Erase modes f_{CPU} = 8 MHz, V_{DD} = 5.5 V			2.6	mA
		No Read/No Write Mode			100	µA
		Power down mode / Halt		0	0.1	µA

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in Halt mode or under reset) or in hardware registers (only in Halt mode). Guaranteed by construction, not tested in production.
2. Up to 32 bytes can be programmed at a time.
3. Data based on reliability test results and monitored in production.
4. The data retention time increases when the T_A decreases.
5. Design target value pending full product characterization.
6. Guaranteed by Design. Not tested in production.

12.7 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

12.7.1 Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Pre-qualification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the $\overline{\text{RESET}}$ pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 59. EMC characteristics

Symbol	Parameter	Conditions	Level/ class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5 V, T_A=+25 °C, f_{OSC}=8 MHz, SO8 package, conforms to IEC 1000-4-2	3B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5 V, T_A=+25 °C, f_{OSC}=8 MHz, SO8 package, conforms to IEC 1000-4-4	4B

Figure 63. Typical application with ADC

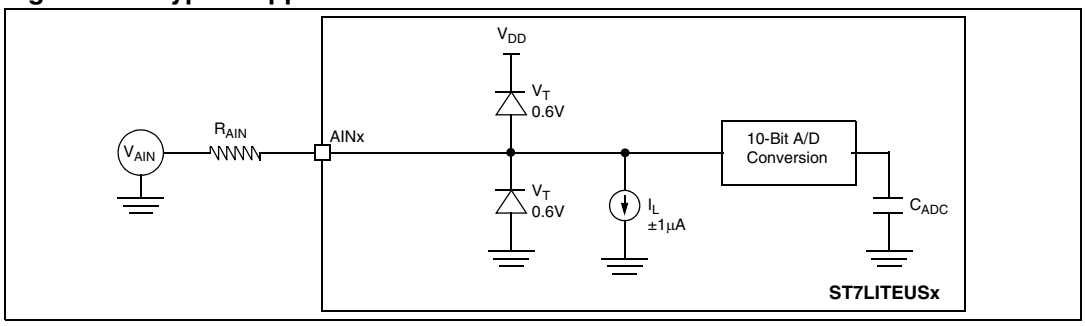


Table 67. ADC accuracy with V_{DD} = 3.3 to 5.5 V

Symbol (1)	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error	f_{CPU}=8 MHz, f_{ADC}=4 MHz(1)	2.1	3.0	LSB
$\|E_O\|$	Offset error		0.2	2.5	
$\|E_G\|$	Gain Error		0.3	1.5	
$\|E_D\|$	Differential linearity error		1.9	3.5	
$\|E_L\|$	Integral linearity error		1.9	4.5	

1. Data based on characterization results over the whole temperature range.

Table 68. ADC accuracy with V_{DD} = 2.7 to 3.3 V

Symbol (1)	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error	f_{CPU}=4 MHz, f_{ADC}=2 MHz(1)	2.0	3.0	LSB
$\|E_O\|$	Offset error		0.1	1.5	
$\|E_G\|$	Gain Error		0.4	1.4	
$\|E_D\|$	Differential linearity error		1.8	2.5	
$\|E_L\|$	Integral linearity error		1.7	2.5	

1. Data based on characterization results over the whole temperature range.

Table 69. ADC accuracy with V_{DD} = 2.4V to 2.7V

Symbol (1)	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error	f_{CPU}=2 MHz, f_{ADC}=1 MHz(1)	2.2	3.5	LSB
$\|E_O\|$	Offset error		0.5	1.5	
$\|E_G\|$	Gain Error		0.5	1.5	
$\|E_D\|$	Differential linearity error		1.8	2.5	
$\|E_L\|$	Integral linearity error		1.8	2.5	

1. Data based on characterization results at a temperature ≥ 25°C.

13 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

13.1 Package mechanical data

Figure 65. 8-lead very thin fine pitch dual flat no-lead package outline

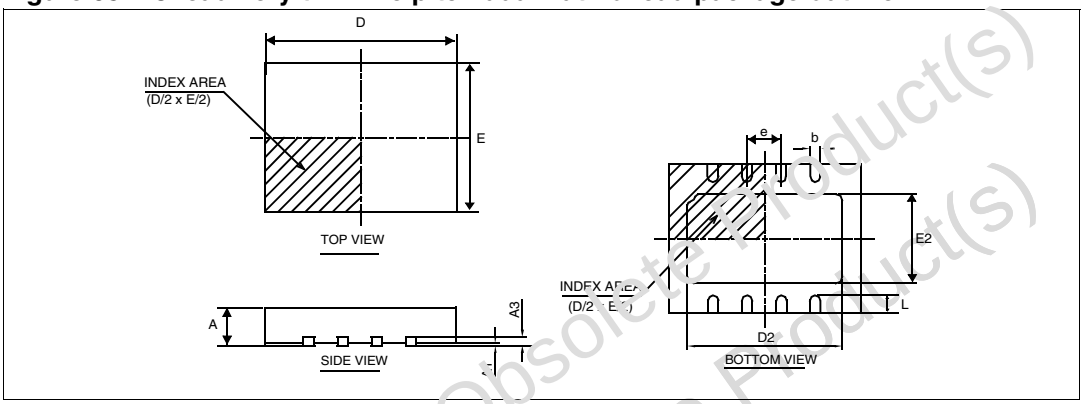


Table 70. 8-lead very thin fine pitch dual flat no-lead package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0310	0.0350	0.0390
A1	0.00	0.02	0.05	0.0000	0.0010	0.0020
A3		0.20			0.0080	
b	0.25	0.30	0.35	0.0100	0.0120	0.0140
D		4.50			0.1770	
D2	3.50	3.65	3.75	0.1380	0.1440	0.1480
E		3.50			0.1380	
E2	1.96	2.11	2.21	0.0770	0.0830	0.0870
e		0.80			0.0310	
L	0.30	0.40	0.50	0.0120	0.0160	0.0200
	Number of pins					
N	8					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 75. Startup clock selection

Configuration	CKSEL1	CKSEL0
Internal RC as Startup Clock	0	0
Reserved	0	0
AWU RC as a Startup Clock	0	1
Reserved	1	0
External Clock on pin PA5	1	1

Table 76. LVD threshold configuration

Configuration	LVD1	LVD0
LVD Off	1	1
Highest voltage threshold	1	0
Medium voltage threshold	0	1
Lowest voltage threshold	0	0

14.1.2 OPTION BYTE 0

Bits 7:4 Reserved, must always be 1.

Bit 3 Reserved, must always be 0.

Bit 2 **SEC0** *Sector 0 size definition*
This option bit indicates the size of sector 0 according to the following table (see *Table 77: Definition of sector 0 size*).

Bit 1 **FMP_R** *Readout protection*
Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Erasing the option bytes when the FMP_R option is selected will cause the whole memory to be erased first, and the device can be reprogrammed. Refer to *Section 4.5* and the ST7 Flash Programming Reference Manual for more details.
0: Readout protection off
1: Readout protection on

Bit 0 **FMP_W** *FLASH write protection*
This option indicates if the FLASH program memory is write protected.
Warning: When this option is selected, the program memory (and the option bit itself) can never be erased or programmed again.
0: Write protection off
1: Write protection on

Table 77. Definition of sector 0 size

Sector 0 Size	SEC0
0.5k	0
1k	1

Table 80. Development tool order codes for the ST7LITEUSx family

Supported products	In-circuit Debugger, RLink series[1]		Emulator		Programming tool	
	Starter kit without demo board	Starter kit with Demo Board	DVP series	EMU series	In-circuit programmer	ST socket boards and EPBs
ST7FLITEUS2 ST7FLITEUS5	STX-RLINK[2]	STFLITE-SK/RAIS[2]	ST7MDT10-DVP3[3]	ST7MDT10-EMU3	STX-RLINK ST7-STICK[5][4]	ST7SB10-SU0[5]

1. Available from ST or from Raisonance, www.raisonance.com.
2. USB connection to PC.
3. Includes connection kit for Plastic DIP16/SO16 only. See “How to order an EMU or DVP” in ST product and tool selection guide for connection kit ordering information.
4. Parallel port connection to PC.
5. Add suffix /EU, /UK or /US for the power supply for your region.

14.4 ST7 application notes

Table 81. ST7 application notes

Identification	Description
Application examples	
AN1658	Serial numbering implementation
AN1720	Managing the readout protection in flash microcontrollers
AN1755	A high resolution/precision thermometer using ST7 and NE555
AN1756	Choosing a DALI implementation strategy with ST7DALI
AN1812	A high precision, low cost, single supply ADC for positive and negative input voltages
Example drivers	
AN 969	SCI communication between ST7 and PC
AN 970	SPI communication between ST7 and EEPROM
AN 971	I²C communication between ST7 and M24Cxx EEPROM
AN 972	ST7 software SPI master communication
AN 973	SCI software communication with a PC using ST72251 16-bit timer
AN 974	Real time clock with ST7 Timer Output Compare
AN 976	Driving a buzzer through ST7 timer PWM function
AN 979	Driving an analog keyboard with the ST7 ADC
AN 980	ST7 keypad decoding techniques, implementing wakeup on keystroke
AN1017	Using the ST7 universal serial bus microcontroller
AN1041	Using ST7 PWM signal to generate analog output (sinusoïd)
AN1042	ST7 routine for I²C slave mode management

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