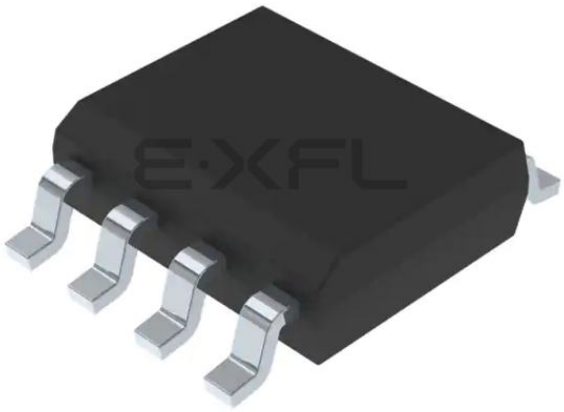

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fliteus5m6

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Table 3. Hardware register map (continued)(1)

Address	Block	Register label	Register name	Reset status	Remarks
0049h 004Ah	AWU	AWUPR AWUCSR	AWU Prescaler register AWU Control/Status register	FFh 00h	R/W R/W
004Bh 004Ch 004Dh 004Eh 004Fh 0050h	DM(4)	DMCR DMSR DMBK1H DMBK1L DMBK2H DMBK2L	DM Control register DM Status register DM Breakpoint register 1 High DM Breakpoint register 1 Low DM Breakpoint register 2 High DM Breakpoint register 2 Low	00h 00h 00h 00h 00h 00h	R/W R/W R/W R/W R/W R/W
0051h to 007Fh	Reserved area (47 bytes)				

1. Legend: x=undefined, R/W=read/write
2. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.
3. The bits associated with unavailable pins must always keep their reset value.
4. For a description of the DM registers, see the ST7 I^2C Protocol Reference Manual.

4 Flash program memory

4.1 Introduction

The ST7 single voltage extended Flash (XFlash) is a non-volatile memory that can be electrically erased and programmed either on a byte-by-byte basis or up to 32 bytes in parallel.

The XFlash devices can be programmed off-board (plugged in a programming tool) or on-board using in-circuit programming or in-application programming.

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- ICP (in-circuit programming)
- IAP (in-application programming)
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Sector 0 size configurable by option byte
- Readout and write protection

4.3 Programming modes

The ST7 can be programmed in three different ways:

- Insertion in a programming tool

  In this mode, FLASH sectors 0 and 1 and option byte row can be programmed or erased.
- In-circuit programming

  In this mode, FLASH sectors 0 and 1 and option byte row can be programmed or erased without removing the device from the application board.
- In-application programming

  In this mode, sector 1 can be programmed or erased without removing the device from the application board and while the application is running.

4.3.1 In-circuit programming (ICP)

ICP uses a protocol called I^2C (in-circuit communication) which allows an ST7 plugged on a printed circuit board (PCB) to communicate with an external programming device connected via cable. ICP is performed in three steps:

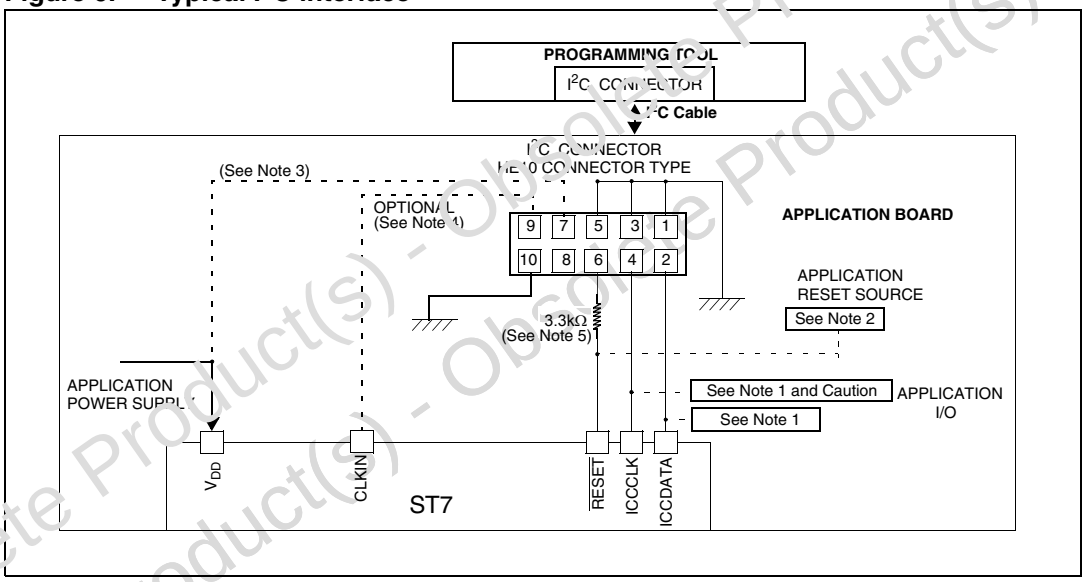
- Switch the ST7 to I^2C mode. This is done by driving a specific signal sequence on the ICCCLK/DATA pins while the $\overline{\text{RESET}}$ pin is pulled low. When the ST7 enters I^2C mode, it fetches a specific RESET vector which points to the ST7 system memory containing

Pin 9 has to be connected to the CLKIN pin of the ST7 when I^2C mode is selected with option bytes disabled (35-pulse I^2C entry mode). When option bytes are enabled (38-pulse I^2C entry mode), the internal RC clock (internal RC or AWU RC) is forced. If internal RC is selected in the option byte, the internal RC is provided. If AWU RC or external clock is selected, the AWU RC oscillator is provided.

A serial resistor must be connected to I^2C connector pin 6 in order to prevent contention on PA3/$\overline{\text{RESET}}$ pin. Contention may occur if a tool forces a state on $\overline{\text{RESET}}$ pin while PA3 pin forces the opposite state in output mode. The resistor value is defined to limit the current below 2 mA at 5 V. If PA3 is used as output push-pull, then the application must be switched off to allow the tool to take control of the $\overline{\text{RESET}}$ pin (PA3). To allow the programming tool to drive the $\overline{\text{RESET}}$ pin below V_{IL}, special care must also be taken when a pull-up is placed on PA3 for application reasons.

Caution: During normal operation, ICCCLK pin must be pulled- up, internally or externally (external pull-up of 10 kΩ mandatory in noisy environment). This is to avoid entering I^2C mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up.

Figure 6. Typical I^2C interface



4.5 Memory protection

There are two different types of memory protection: readout protection and Write/Erase Protection which can be applied individually.

4.5.1 Readout protection

Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller. Program memory is protected.

6 Supply, reset and clock management

The device includes a range of utility features for securing the application in critical situations (for example in case of a power brown-out), and reducing the number of external components.

6.1 Main features

- Clock management
  - 8 MHz internal RC oscillator (enabled by option byte)
  - External clock Input (enabled by option byte)
- Reset sequence manager (RSM)
- System integrity management (SI)
  - Main supply low voltage detection (LVD) with reset generation (enabled by option byte)
  - Auxiliary voltage detector (AVD) with interrupt capability for monitoring the main supply

6.2 Internal RC oscillator adjustment

The ST7 contains an internal RC oscillator with a specific accuracy for a given device, temperature and voltage. It can be selected as the start up clock through the CKSEL[1:0] option bits (see *Section 14.1 on page 123*). It must be calibrated to obtain the frequency required in the application. This is done by software writing a 10-bit calibration value in the RCCR (RC Control register) and in the bits [6:5] in the SICSR (SI Control Status register).

Whenever the microcontroller is reset, the RCCR returns to its default value (FFh), i.e. each time the device is reset, the calibration value must be loaded in the RCCR. Predefined calibration values are stored in Flash memory for 3.3 and 5 V V_{DD} supply voltages at 25°C, as shown in the following table.

Table 5. Predefined RC oscillator calibration values

RCCR	Conditions	ST7LITEUS2/ST7LITEUS5 address
RCCRH0	V_{DD}=5 V T_A=25 °C f_{RC}=8 MHz	DEE0h(1) (CR[9:2] bits)
RCCRL0		DEE1h 1) (CR[1:0] bits)
RCCRH1	V_{DD}=3.3 V T_A=25 °C f_{RC}=8 MHz	DEE2h 1) (CR[9:2] bits)
RCCRL1		DEE3h 1) (CR[1:0] bits)

1. DEE0h, DEE1h, DEE2h and DEE3h are located in a reserved area butare special bytes containing also the RC calibration values which are read-accessible only in user mode. If all the Flash space (including the RC calibration value locations) has been erased (after the readout protection removal), then the RC calibration values can still be obtained through these two addresses.

Note: 1 In I^2C mode, the internal RC oscillator is forced as a clock source, regardless of the selection in the option byte. Refer to note 5 in Section 4.4 on page 19 for further details.

2 See Section 12: Electrical characteristics for more information on the frequency and accuracy of the RC oscillator.

3 To improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

Caution: If the voltage or temperature conditions change in the application, the frequency may need to be recalibrated.

Refer to application note AN2326 for information on how to calibrate the RC frequency using an external reference signal.

The ST7LITEUS2 and ST7LITEUS5 also contain an Auto-wakeup RC oscillator. This RC oscillator should be enabled to enter Auto-wakeup from Halt mode.

The Auto-wakeup RC oscillator can also be configured as the startup clock through the CKSEL[1:0] option bits (see *Section 14.1 on page 123*).

This is recommended for applications where very low power consumption is required.

Switching from one startup clock to another can be done in run mode as follows (see *Figure 9*):

Case 1

Switching from internal RC to AWU:

1. Set the RC/AWU bit in the CKCNTCSR register to enable the AWU RC oscillator
2. The RC_FLAG is cleared and the clock output is at 1.
3. Wait 3 AWU RC cycles till the AWU_FLAG is set
4. The switch to the AWU clock is made at the positive edge of the AWU clock signal
5. Once the switch is made, the internal RC is stopped

Case 2

Switching from AWU RC to internal RC:

1. Reset the RC/AWU bit to enable the internal RC oscillator
2. Using a 4-bit counter, wait until 8 internal RC cycles have elapsed. The counter is running on internal RC clock.
3. Wait till the AWU_FLAG is cleared (1AWU RC cycle) and the RC_FLAG is set (2 RC cycles)
4. The switch to the internal RC clock is made at the positive edge of the internal RC clock signal
5. Once the switch is made, the AWU RC is stopped

Note: 1 When the internal RC is not selected, it is stopped so as to save power consumption.

2 When the internal RC is selected, the AWU RC is turned on by hardware when entering Auto-wakeup from Halt mode.

3 When the external clock is selected, the AWU RC oscillator is always on.

7.4.2 Auxiliary voltage detector (AVD)

The voltage detector function (AVD) is based on an analog comparison between a $V_{IT-(AVD)}$ and $V_{IT+(AVD)}$ reference value and the V_{DD} main supply voltage (V_{AVD}). The $V_{IT-(AVD)}$ reference value for falling voltage is lower than the $V_{IT+(AVD)}$ reference value for rising voltage in order to avoid parasitic detection (hysteresis).

The output of the AVD comparator is directly readable by the application software through a real time status bit (AVDF) in the SICSR register. This bit is read only.

Monitoring the V_{DD} main supply

The AVD threshold is selected by the AVD[1:0] bits in the AVDTHCR register.

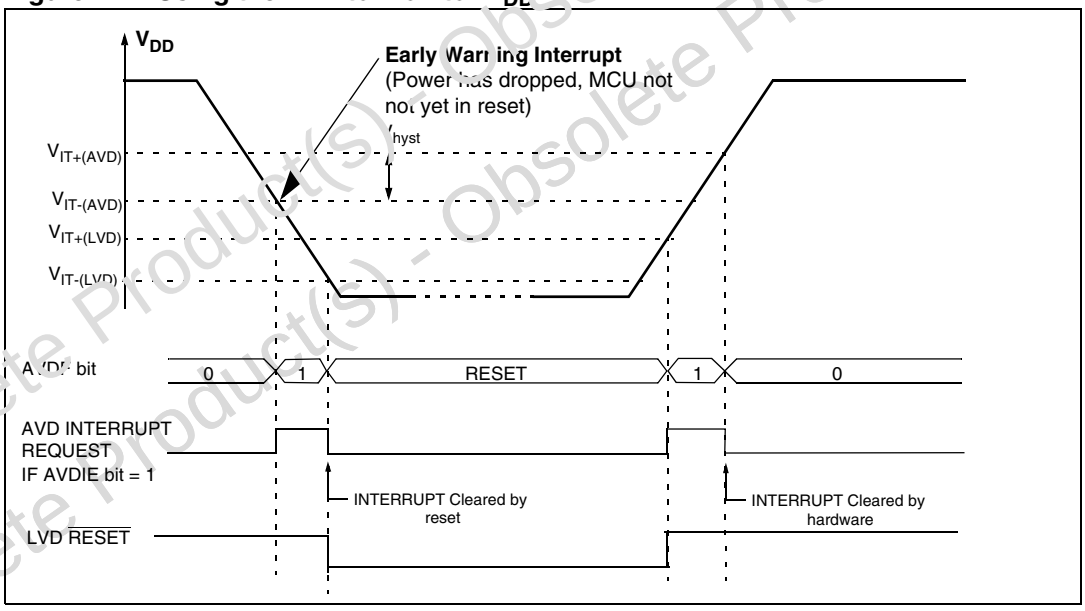
If the AVD interrupt is enabled, an interrupt is generated when the voltage crosses the $V_{IT+(AVD)}$ or $V_{IT-(AVD)}$ threshold (AVDF bit is set).

In the case of a drop in voltage, the AVD interrupt acts as an early warning, allowing software to shut down safely before the LVD resets the microcontroller. See *Figure 17*.

The interrupt on the rising edge is used to inform the application that the V_{DD} warning state is over

Note: Make sure the right combination of LVD and AVD threshold is used as LVD and AVD levels are not correlated. Refer to Table 47 on page 95 and Table 48 on page 96 for more details.

Figure 17. Using the AVD to monitor V_{DD}



8.2 Slow mode

This mode has two targets:

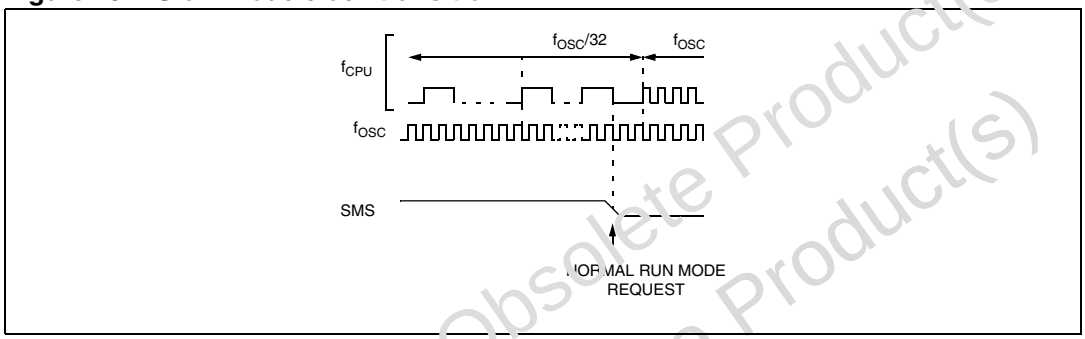
- To reduce power consumption by decreasing the internal clock in the device,
- To adapt the internal clock frequency (f_{CPU}) to the available supply voltage.

Slow mode is controlled by the SMS bit in the MCCSR register which enables or disables Slow mode.

In this mode, the oscillator frequency is divided by 32. The CPU and peripherals are clocked at this lower frequency.

Note: Slow-wait mode is activated when entering Wait mode while the device is already in Slow mode.

Figure 19. Slow mode clock transition



8.3 Wait mode

Wait mode places the MCU in a low power consumption mode by stopping the CPU.

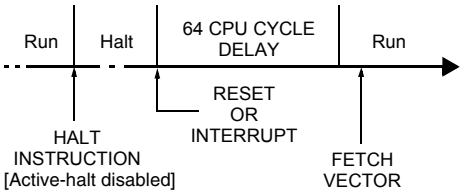
This power saving mode is selected by calling the 'WFI' instruction.

All peripherals remain active. During Wait mode, the I bit of the CC register is cleared, to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in Wait mode until an interrupt or reset occurs, whereupon the Program Counter branches to the starting address of the interrupt or Reset service routine.

The MCU will remain in Wait mode until a Reset or an Interrupt occurs, causing it to wakeup.

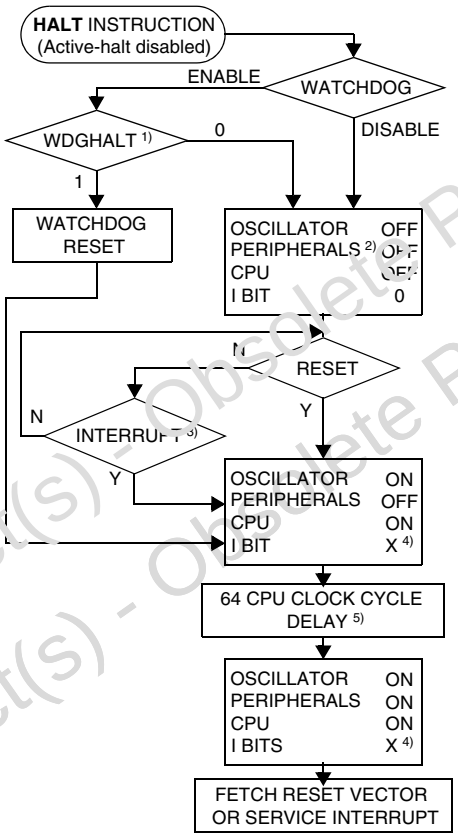
Refer to *Figure 20* for a description of the Wait mode flowchart.

Figure 23. Halt timing overview



1. A reset pulse of at least 42µs must be applied when exiting from Halt mode.

Figure 24. Halt mode flowchart



1. WDGHALT is an option bit. See option byte section for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only some specific interrupts can exit the MCU from Halt mode (such as external interrupt). Refer to *Table 9: Interrupt mapping* for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I bit of the CC register is set during the interrupt routine and cleared when the CC register is popped.
5. The CPU clock must be switched to 1 MHz (RC/8) or AWU RC before entering Halt mode.

Caution: The alternate function must not be activated as long as the pin is configured as input with interrupt, in order to avoid generating spurious interrupts.

Analog alternate function

When the pin is used as an ADC input, the I/O must be configured as floating input. The analog multiplexer (controlled by the ADC registers) switches the analog voltage present on the selected pin to the common analog rail which is connected to the ADC input.

It is recommended not to change the voltage level or loading on any port pin while conversion is in progress. Furthermore it is recommended not to have clocking pins located close to a selected analog pin.

Warning: The analog input voltage level must be within the limits stated in the absolute maximum ratings.

9.3 Unused I/O pins

Unused I/O pins must be connected to fixed voltage levels. Refer to *Section 12.8*.

9.4 Low power modes

Table 20. Effect of low power modes on I/O ports

Mode	Description
Wait	No effect on I/O ports. External interrupts cause the device to exit from Wait mode.
Halt	No effect on I/O ports. External interrupts cause the device to exit from Halt mode.

9.5 Interrupts

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR and OR registers and the interrupt mask in the CC register is not active (RIM instruction).

Table 21. Description of interrupt events

Interrupt event	Event flag	Enable control bit	Exit from Wait	Exit from Halt
External interrupt on selected external event	-	DDRx ORx	Yes	Yes

10.2.5 Interrupts

Table 28. Interrupt events

Interrupt event [1]	Event flag	Enable control bit	Exit from Wait	Exit from Halt	Exit from Active-halt
Overflow event	OVF	OVFIE	Yes	No	Yes[2]
CMP event	CMPFx	CMPIE	Yes	No	No

1. The interrupt events are connected to separate interrupt vectors (see Interrupts chapter). They generate an interrupt if the enable bit is set in the ATCSR register and the interrupt mask in the CC register is reset (RIM instruction).
2. Only if CK0=1 and CK1=0

10.2.6 Register description

Timer control status register (ATCSR)

Reset value: 0000 0000 (00h)

7							0
0	0	0	CK1	CK0	OVF	OVFIE	CMPIE
Read/write							

Bits 7:5 Reserved, must be kept cleared.

Bits 4:3 **CK[1:0]** *Counter Clock Selection.*
These bits are set and cleared by software and cleared by hardware after a reset. They select the clock frequency of the counter (see *Table 29: Counter clock selection*).

Bit 2 **OVF** *Overflow flag.*
This bit is set by hardware and cleared by software by reading the ATCSR register. It indicates the transition of the counter from FFFh to ATR value.
0: No counter overflow occurred
1: Counter overflow occurred
When set, the OVF bit stays high for 1 $f_{COUNTER}$ cycle (up to 1ms depending on the clock selection) after it has been cleared by software.

Bit 1 **OVFIE** *Overflow interrupt enable.*
This bit is read/write by software and cleared by hardware after a reset.
0: OVF interrupt disabled
1: OVF interrupt enabled

Bit 0 **CMPIE** *Compare interrupt enable.*
This bit is read/write by software and clear by hardware after a reset. It allows to mask the interrupt generation when CMPF bit is set.
0: CMPF interrupt disabled
1: CMPF interrupt enabled

10.3.5 Interrupts

None.

10.3.6 Register description

Control/Status register (ADCCSR)

Reset value: 0000 0000 (00h)

7							0
EOC	SPEED	ADON	0	0	CH2	CH1	CH0
Read/Write (Except bit 7 read only)							

Bit 7 **EOC** *End of Conversion*
This bit is set by hardware. It is cleared by software reading the ADCDRH register.
0: Conversion is not complete
1: Conversion complete

Bit 6 **SPEED** *ADC clock selection*
This bit is set and cleared by software. It is used together with the SLOW bit to configure the ADC clock speed. Refer to the table in the SLOW bit description.

Bit 5 **ADON** *A/D Converter on*
This bit is set and cleared by software.
0: A/D converter is switched off
1: A/D converter is switched on

Bits 4:3 **Reserved.** Must be kept cleared.

Bits 2:0 **CH[2:0]** *Channel Selection*
These bits are set and cleared by software. They select the analog input to convert.

Note: A write to the ADCCSR register (with ADON set) aborts the current conversion, resets the EOC bit and starts a new conversion.

Table 32. Channel selection

Channel pin	CH2	CH1	CH0
AIN0	0	0	0
AIN1	0	0	1
AIN2	0	1	0
AIN3	0	1	1
AIN4	1	0	0

ADC data register high (ADCDRH)

Reset value: 0000 0000 (00h)

7							0
D9	D8	D7	D6	D5	D4	D3	D2
Read only							

Bits 7:0 D[9:2] *MSB of Analog Converted value*

ADC control/data register Low (ADCDRL)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	SLOW	0	D1	D0
Read/write							

Bits 7:4 Reserved. Forced by hardware to 0.

Bit 3 **SLOW** *Slow mode*
This bit is set and cleared by software. It is used together with the SPEED bit to configure the ADC clock speed as shown on the table below (see *Table 33: Configuring the ADC clock speed*).

Bit 2 Reserved. Forced by hardware to 0.

Bits 1:0 **D[1:0]** *LSB of Analog Converted value*

Table 33. Configuring the ADC clock speed

f_{ADC}	SLOW	SPEED
$f_{CPU}/2$	0	0
f_{CPU}	0	1
$f_{CPU}/4$	1	x

Table 34. ADC register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0034h	**ADCCSR** Reset value	EOC 0	SPEED 0	ADON 0	0 0	0 0	CH2 0	CH1 0	CH0 0
0035h	**ADCDRH** Reset value	D9 0	D8 0	D7 0	D6 0	D5 0	D4 0	D3 0	D2 0
0036h	**ADCDRL** Reset value	0 0	0 0	0 0	0 0	SLOW 0	0 0	D1 0	D0 0

11 Instruction set

11.1 ST7 addressing modes

The ST7 Core features 17 different addressing modes which can be classified in seven main groups:

Table 35. Description of addressing modes

Addressing mode	Example
Inherent	nop
Immediate	ld A,#$55
Direct	ld A,$55
Indexed	ld A,($55,X)
Indirect	ld A ([$55],X)
Relative	jrne loop
Bit operation	bset byte,#5

The ST7 instruction set is designed to minimize the number of bytes required per instruction: To do so, most of the addressing modes may be subdivided in two submodes called long and short:

- Long addressing mode is more powerful because it can use the full 64 Kbyte address space, however it uses more bytes and more CPU cycles.
- Short addressing mode is less powerful because it can generally only access page zero (0000h - 00FFh range), but the instruction size is more compact, and faster. All memory to memory instructions use short addressing modes only (CLR, CPL, NEG, BSET, BRES, BTJT, BTJF, INC, DEC, RLC, RRC, SLL, SRL, SRA, SWAP)

The ST7 Assembler optimizes the use of long and short addressing modes.

Table 36. ST7 addressing mode overview (1)

Mode			Syntax	Destination/ source	Pointer address	Pointer size	Length (bytes)
Inherent			nop				+ 0
Immediate			ld A,#$55				+ 1
Short	Direct		ld A,$10	00..FF			+ 1
Long	Direct		ld A,$1000	0000..FFFF			+ 2
No Offset	Direct	Indexed	ld A,(X)	00..FF			+ 0 (with X register) + 1 (with Y register)
Short	Direct	Indexed	ld A,($10,X)	00..1FE			+ 1
Long	Direct	Indexed	ld A,($1000,X)	0000..FFFF			+ 2
Short	Indirect		ld A,[$10]	00..FF	00..FF	byte	+ 2
Long	Indirect		ld A,[$10.w]	0000..FFFF	00..FF	word	+ 2
Short	Indirect	Indexed	ld A,([$10],X)	00..1FE	00..FF	byte	+ 2

11.1.2 Immediate

Immediate instructions have 2 bytes, the first byte contains the opcode, the second byte contains the operand value.

Table 38. Instructions supporting inherent immediate addressing mode

Immediate instruction	Function
LD	Load
CP	Compare
BCP	Bit compare
AND, OR, XOR	Logical operations
ADC, ADD, SUB, SBC	Arithmetic operations

11.1.3 Direct

In Direct instructions, the operands are referenced by their memory address.

The direct addressing mode consists of two submodes:

Direct (short) addressing mode

the address is a byte, thus requires only 1 byte after the opcode, but only allows 00 - FF addressing space.

Direct (long) addressing mode

The address is a word, thus allowing 64 Kbyte addressing space, but requires 2 bytes after the opcode.

11.1.4 Indexed mode (no offset, short, long)

In this mode, the operand is referenced by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset.

The indirect addressing mode consists of three submodes:

Indexed mode (no offset)

There is no offset (no extra byte after the opcode), and allows 00 - FF addressing space.

Indexed mode (short)

The offset is a byte, thus requires only 1 byte after the opcode and allows 00 - 1FE addressing space.

Indexed mode (long)

The offset is a word, thus allowing 64 Kbyte addressing space and requires 2 bytes after the opcode.

11.1.5 Indirect modes (short, long)

The required data byte to do the operation is found by its memory address, located in memory (pointer).

The pointer address follows the opcode. The indirect addressing mode consists of two submodes:

Indirect mode (short)

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - FF addressing space, and requires 1 byte after the opcode.

Indirect mode (long)

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

11.1.6 Indirect indexed modes (short, long)

This is a combination of indirect and short indexed addressing modes. The operand is referenced by its memory address, which is defined by the unsigned addition of an index register value (X or Y) with a pointer value located in memory. The pointer address follows the opcode.

The indirect indexed addressing mode consists of two submodes:

Indirect indexed mode (short)

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - 1FE addressing space, and requires 1 byte after the opcode.

Indirect indexed mode (long)

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

Table 30. Instructions supporting direct, indexed, indirect and indirect indexed addressing modes

Instructions	Function
Long and short instructions	
LD	Load
CP	Compare
AND, OR, XOR	Logical operations
ADC, ADD, SUB, SBC	Arithmetic addition/subtraction operations
BCP	Bit compare
Short instructions only	
CLR	Clear
INC, DEC	Increment/decrement
TNZ	Test negative or zero

Figure 40. Typical accuracy with RCCR=RCCR0 vs V_{DD}= 2.4-6.0 V and temperature

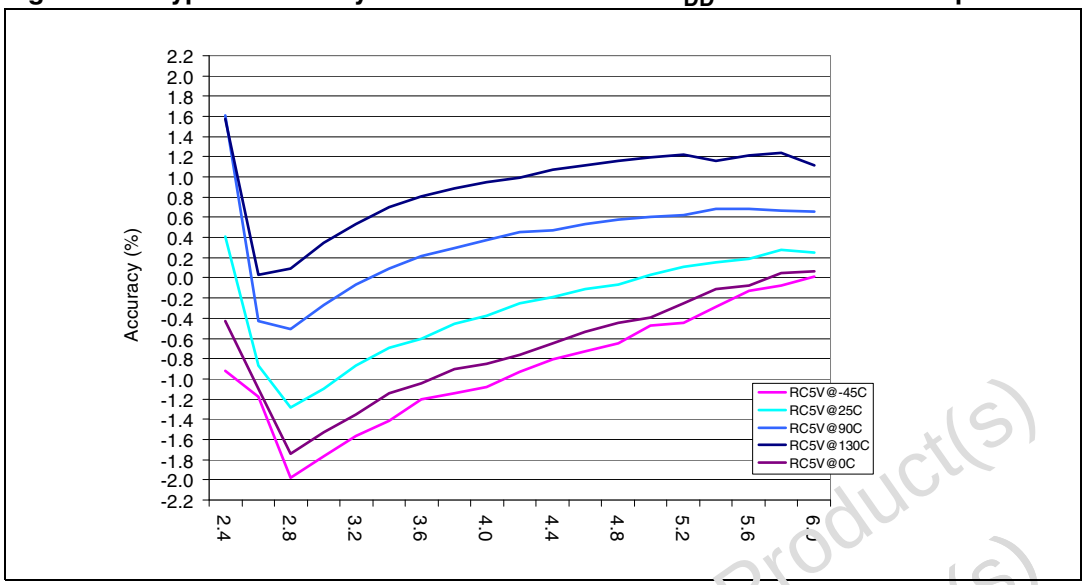


Figure 41. Typical accuracy with RCCR=RCCR1 vs V_{DD}= 2.4-6.0V and temperature

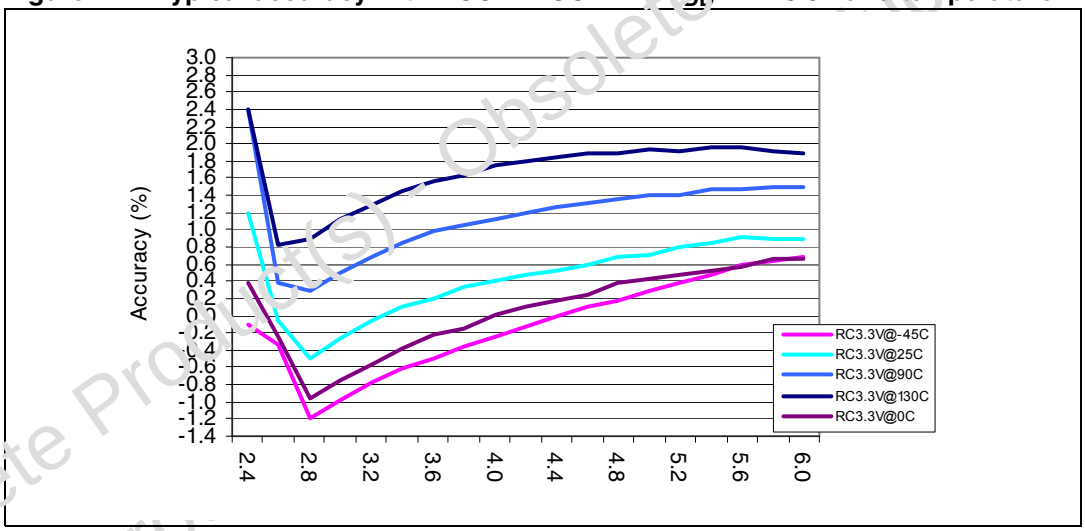
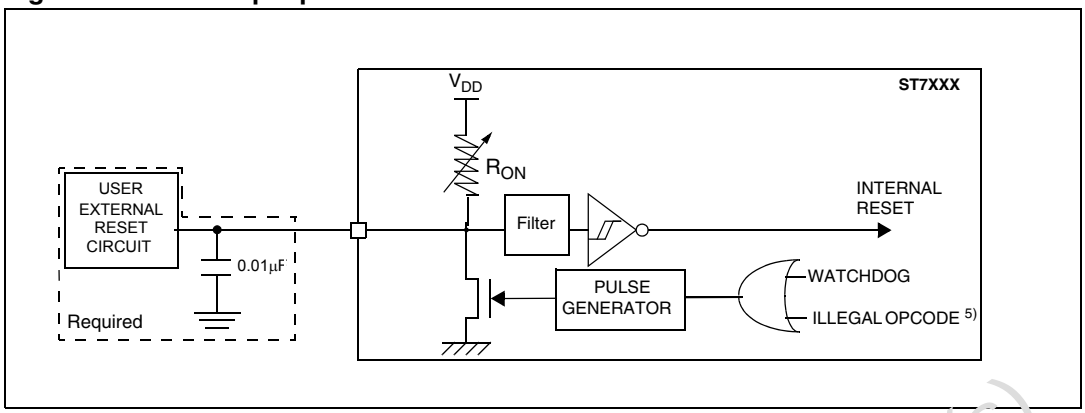


Figure 62. $\overline{\text{RESET}}$ pin protection when LVD is disabled



12.10 ADC characteristics

Subject to general operating condition for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 66. 10-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency(2)				4	MHz
V_{AIN}	Conversion voltage range(3)		V_{SSA}		V_{DDA}	V
R_{AIN}	External input resistor	V_{DD} = 5 V, f_{ADC}=4 MHz			8(4)	kΩ
		V_{DD} = 3.3 V, f_{ADC}=4 MHz			7(4)	
		2.7 V ≤ V_{DD} ≤5.5 V, f_{ADC}=2 MHz			10(4)	
		2.4 V ≤ V_{DD} ≤2.7 V, f_{ADC}=1 MHz			TBD(4)	
C_{ADC}	Internal sample and hold capacitor			3		pF
t_{STAB}	Stabilization time after ADC enable	f_{CPU}=8 MHz, f_{ADC}=4 MHz		0(5)		µs
t_{ADC}	Conversion time (Sample+Hold)			3.5		
	- Sample capacitor loading time - Hold conversion time			4 10		$1/f_{ADC}$

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}-V_{SS}=5 V. They are given only as design guidelines and are not tested.
2. The maximum ADC clock frequency allowed within V_{DD} = 2.4 to 2.7 V operating range is 1 MHz.
3. When V_{DDA} and V_{SSA} pins are not available on the pinout, the ADC refers to V_{DD} and V_{SS}.
4. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.
5. The stabilization time of the A/D converter is masked by the first t_{LOAD}. The first conversion after the enable is then always valid.

Figure 66. 8-pin plastic small outline package, 150-mil width package outline

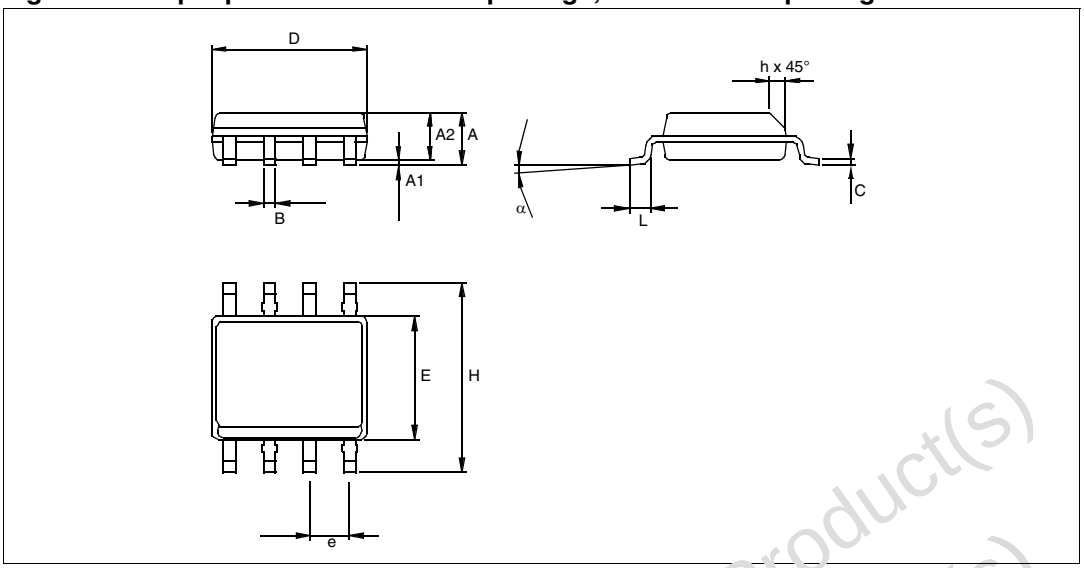


Table 71. 8-pin plastic small outline package, 150-mil width, package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.0530		0.0690
A1	0.10		0.25	0.0040		0.0100
A2	1.10		1.65	0.0430		0.0650
B	0.33		0.51	0.0130		0.0200
C	0.19		0.25	0.0070		0.0100
D	4.80		5.00	0.1890		0.1970
E	3.80		4.00	0.1500		0.1580
e		1.27			0.0500	
H	5.80		6.20	0.2280		0.2440
h	0.25		0.50	0.0100		0.0200
α	0d		8d			
L	0.40		1.27	0.0160		0.0500
	Number of pins					
N	8					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 75. Startup clock selection

Configuration	CKSEL1	CKSEL0
Internal RC as Startup Clock	0	0
Reserved	0	0
AWU RC as a Startup Clock	0	1
Reserved	1	0
External Clock on pin PA5	1	1

Table 76. LVD threshold configuration

Configuration	LVD1	LVD0
LVD Off	1	1
Highest voltage threshold	1	0
Medium voltage threshold	0	1
Lowest voltage threshold	0	0

14.1.2 OPTION BYTE 0

Bits 7:4 Reserved, must always be 1.

Bit 3 Reserved, must always be 0.

Bit 2 **SEC0** *Sector 0 size definition*
This option bit indicates the size of sector 0 according to the following table (see *Table 77: Definition of sector 0 size*).

Bit 1 **FMP_R** *Readout protection*
Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Erasing the option bytes when the FMP_R option is selected will cause the whole memory to be erased first, and the device can be reprogrammed. Refer to *Section 4.5* and the ST7 Flash Programming Reference Manual for more details.
0: Readout protection off
1: Readout protection on

Bit 0 **FMP_W** *FLASH write protection*
This option indicates if the FLASH program memory is write protected.
Warning: When this option is selected, the program memory (and the option bit itself) can never be erased or programmed again.
0: Write protection off
1: Write protection on

Table 77. Definition of sector 0 size

Sector 0 Size	SEC0
0.5k	0
1k	1