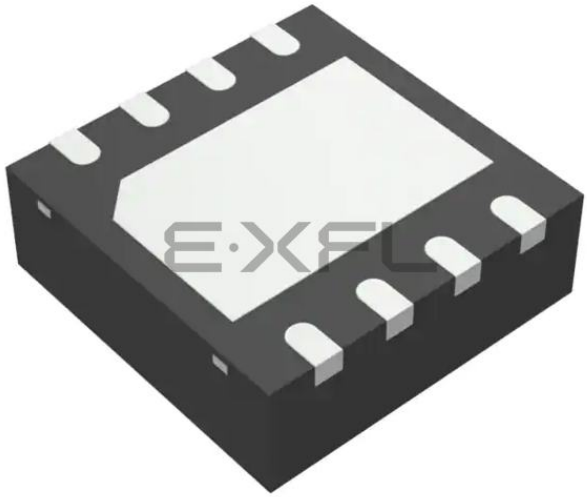

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fliteus5u6-tr

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List of tables

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In flash devices, this protection is removed by reprogramming the option. In this case, program memory is automatically erased, and the device can be reprogrammed.

Readout protection selection depends on the device type:

- In Flash devices it is enabled and removed through the FMP_R bit in the option byte.
- In ROM devices it is enabled by mask option specified in the option list.

4.5.2 Flash Write/Erase protection

Write/erase protection, when set, makes it impossible to both overwrite and erase program memory. Its purpose is to provide advanced security to applications and prevent any change being made to the memory content.

Warning: Once set, Write/erase protection can never be removed. A write-protected flash device is no longer reprogrammable.

Write/erase protection is enabled through the FMP_W bit in the option byte.

4.6 Related documentation

For details on Flash programming and I^2C protocol, refer to the ST7 Flash programming reference manual and to the ST7 I^2C protocol reference manual.

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4.7 Register description

4.7.1 Flash Control/Status register (FCSR)

This register controls the XFlash erasing and programming using ICP, IAP or other programming methods.

1st RASS Key: 0101 0110 (56h)

2nd RASS Key: 1010 1110 (AEh)

When an EPB or another programming tool is used (in socket or ICP mode), the RASS keys are sent automatically.

Reset value: 000 0000 (00h)

7							0
0	0	0	0	0	OPT	LAT	PGM
Read/write							

Table 4. FLASH register map and reset values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
002Fh	FCSR Reset value	0	0	0	0	0	OPT 0	LAT 0	PGM 0

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Obsolete Product(s) - Obsolete Product(s)

6.3.2 RC Control register (RCCR)

Reset value: 1111 1111 (FFh)

7							0
CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2
Read / Write							

Bits 7:0 **CR[9:2]** *RC Oscillator Frequency Adjustment Bits*
These bits, as well as CR[1:0] bits in the SICSR register must be written immediately after reset to adjust the RC oscillator frequency and to obtain the required accuracy. The application can store the correct value for each voltage range in Flash memory and write it to this register at startup.
00h = maximum available frequency
FFh = lowest available frequency

Note: To tune the oscillator, write a series of different values in the register until the correct frequency is reached. The fastest method is to use a dichotomy starting with 80h.

6.3.3 System Integrity (SI) Control/status register (SICSR)

Reset value: 0000 0x00 (0xh)

7							0
0	CR1	CR0	0	0	LVDRF	AVDF	AVDIE
Read / Write							

Bit 7 Reserved, must be kept cleared.

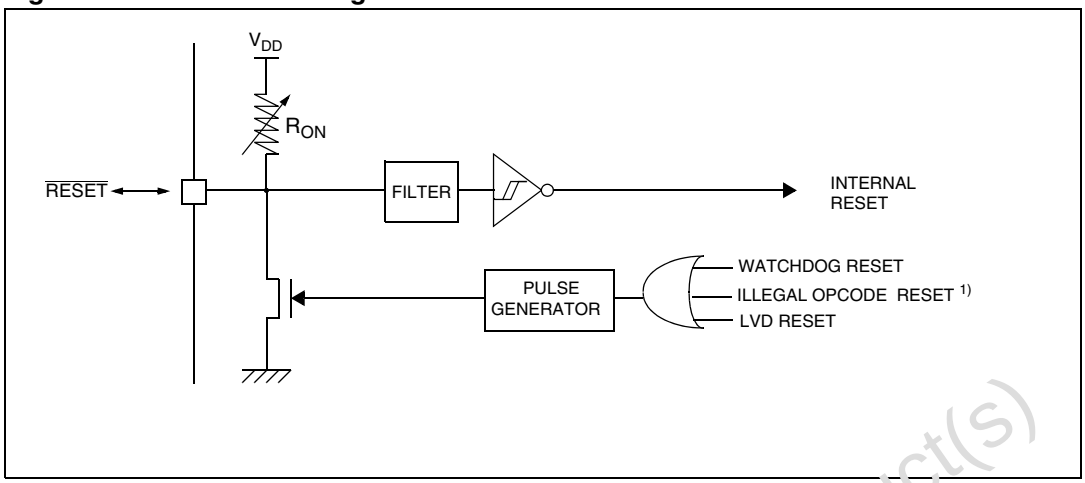
Bits 6:5 **CR[1:0]** *RC Oscillator Frequency Adjustment bits*
These bits, as well as CR[9:2] bits in the RCCR register must be written immediately after reset to adjust the RC oscillator frequency and to obtain the required accuracy. Refer to *Section 6.2 on page 28*.

Bits 4:3 Reserved, must be kept cleared.

Bits 2:0 System Integrity bits. Refer to *Section 7.4 on page 43*.

Obsolete Product(s) - Obsolete Product(s)

Figure 12. Reset block diagram



1. *Section 11.2.1: Illegal opcode reset* for more details on illegal opcode reset conditions

6.4.2 Asynchronous external $\overline{\text{RESET}}$ pin

The $\overline{\text{RESET}}$ pin is both an input and an open-drain output with integrated R_{ON} weak pull-up resistor. This pull-up has no fixed value but varies in accordance with the input voltage. It can be pulled low by external circuitry to reset the device. See Electrical Characteristic section for more details.

A $\overline{\text{RESET}}$ signal originating from an external source must have a duration of at least $t_{h(RSTL)in}$ in order to be recognized (see *Figure 13*). This detection is asynchronous and therefore the MCU can enter reset state even in Halt mode.

The $\overline{\text{RESET}}$ pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in the electrical characteristics section.

6.4.3 External Power-on reset

If the LVD is disabled by option byte, to start up the microcontroller correctly, the user must ensure by means of an external reset circuit that the reset signal is held low until V_{DD} is over the minimum level specified for the selected f_{CLKIN} frequency.

A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the $\overline{\text{RESET}}$ pin.

6.4.4 Internal low voltage detector (LVD) reset

Two different reset sequences caused by the internal LVD circuitry can be distinguished:

- Power-on reset
- Voltage Drop reset

The device $\overline{\text{RESET}}$ pin acts as an output that is pulled low when $V_{DD}<V_{IT+}$ (rising edge) or $V_{DD}<V_{IT-}$ (falling edge) as shown in *Figure 13*.

The LVD filters spikes on V_{DD} larger than $t_{g(VDD)}$ to avoid parasitic resets.

Obsolete Product(s) - Obsolete Product(s)

Note: 1 These 8 bits can be written only when the I bit in the CC register is set.

2 Changing the sensitivity of a particular external interrupt clears this pending interrupt. This can be used to clear unwanted pending interrupts. Refer to Section : External interrupt function.

7.3.2 External Interrupt Control register 2 (EICR2)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	IS41	IS40	IS31	IS30
Read/Write							

Bits 7:4 Reserved

Bits 3:2 **IS4[1:0]** *ei4 sensitivity*
These bits define the interrupt sensitivity for ei1 according to *Table 10*.

Bits 1:0 **IS3[1:0]** *ei3 sensitivity*
These bits define the interrupt sensitivity for ei0 according to *Table 10*.

Note: 1 These 8 bits can be written only when the I bit in the CC register is set.

2 Changing the sensitivity of a particular external interrupt clears this pending interrupt. This can be used to clear unwanted pending interrupts. Refer to Section : External interrupt function.

3 IS4[1:0] = 01 is the only safe configuration to avoid spurious interrupt in Halt and AWUFH modes.

Table 10. Interrupt sensitivity bits

ISx1	ISx0	External interrupt sensitivity
0	0	Falling edge & low level
0	1	Rising edge only
1	0	Falling edge only
1	1	Rising and falling edge

Obsolete Product(s) - Obsolete Product(s)

7.4.3 Low power modes

Table 11. Description of low power modes

Mode	Description
Wait	No effect on SI. AVD interrupts cause the device to exit from Wait mode.
Halt	The SICSR register is frozen. The AVD remains active but the AVD interrupt cannot be used to exit from Halt mode.

Interrupts

The AVD interrupt event generates an interrupt if the corresponding Enable Control Bit (AVDIE) is set and the interrupt mask in the CC register is reset (RIM instruction).

Table 12. Description of interrupt events

Interrupt Event	Event flag	Enable control bit	Exit from Wait	Exit from Halt
AVD event	AVDF	AVDIE	Yes	No

7.4.4 Register description

System Integrity (SI) Control/Status register (SICSR)

Reset value: 0000 0x00 (0xh)

7							0
0	CR1	CR0	0	0	LVDRF	AVDF	AVDIE
Read/write							

Bit 7 Reserved, must be kept cleared.

Bits 6:5 **CR[1:0]** *RC Oscillator Frequency Adjustment bits*

These bits, as well as CR[9:2] bits in the RCCR register must be written immediately after reset to adjust the RC oscillator frequency and to obtain the required accuracy. Refer to *Section 6.2: Internal RC oscillator adjustment on page 28*.

Bits 4:3 Reserved, must be kept cleared.

Obsolete Product(s) - Obsolete Product(s)

8.2 Slow mode

This mode has two targets:

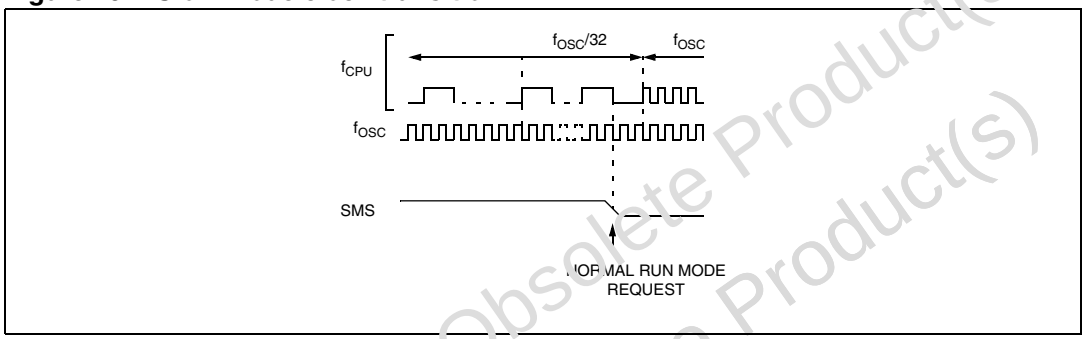
- To reduce power consumption by decreasing the internal clock in the device,
- To adapt the internal clock frequency (f_{CPU}) to the available supply voltage.

Slow mode is controlled by the SMS bit in the MCCSR register which enables or disables Slow mode.

In this mode, the oscillator frequency is divided by 32. The CPU and peripherals are clocked at this lower frequency.

Note: Slow-wait mode is activated when entering Wait mode while the device is already in Slow mode.

Figure 19. Slow mode clock transition



8.3 Wait mode

Wait mode places the MCU in a low power consumption mode by stopping the CPU.

This power saving mode is selected by calling the 'WFI' instruction.

All peripherals remain active. During Wait mode, the I bit of the CC register is cleared, to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in Wait mode until an interrupt or reset occurs, whereupon the Program Counter branches to the starting address of the interrupt or Reset service routine.

The MCU will remain in Wait mode until a Reset or an Interrupt occurs, causing it to wakeup.

Refer to *Figure 20* for a description of the Wait mode flowchart.

Obsolete Product(s) - Obsolete Product(s)

Table 15. Configuring the dividing factor

AWUPR[7:0]	Dividing factor
00h	Forbidden
01h	1
...	...
FEh	254
FFh	255

In AWU mode, the period that the MCU stays in Halt Mode (t_{AWU} in *Figure 26*) is defined by

$$t_{AWU} = 64 \times AWUPR \times \frac{1}{f_{AWURC}} + t_{RCSTRT}$$

This prescaler register can be programmed to modify the time that the MCU stays in Halt mode before waking up automatically.

Note: If 00h is written to AWUPR, depending on the product, an interrupt is generated immediately after a HALT instruction, or the AWUPR remains unchanged.

Table 16. AWU register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0049h	**AWUPR** Reset value	AWUPR7 1	AWUPR6 1	AWUPR5 1	AWUPR4 1	AWUPR3 1	AWUPR2 1	AWUPR1 1	AWUPR0 1
004Ah	**AWUCSR** Reset value	0	0	0	0	0	AWUF	AWUM	AWUEN

Obsolete Product(s) - Obsolete Product(s)

9 I/O ports

9.1 Introduction

The I/O port offers different functional modes:

- Transfer of data through digital inputs and outputs

and for specific pins:

- External interrupt generation
- Alternate signal input/output for the on-chip peripherals.

An I/O port contains up to 6 pins. Each pin (except PA3/$\overline{\text{RESET}}$) can be programmed independently as digital input (with or without interrupt generation) or digital output.

9.2 Functional description

Each port has 2 main registers:

- Data register (DR)
- Data Direction register (DDR)

and one optional register:

- Option register (OR)

Each I/O pin may be programmed using the corresponding register bits in the DDR and OR registers: bit X corresponding to pin X of the port. The same correspondence is used for the DR register.

The following description takes into account the OR register, (for specific ports which do not provide this register refer to the I/O Port Implementation section). The generic I/O block diagram is shown in *Figure 28*.

9.2.1 Input modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Different input modes can be selected by software through the OR register.

Note: 1 Writing the DR register modifies the latch value but does not affect the pin status.

2 PA3 cannot be configured as input.

External interrupt function

When an I/O is configured as Input with Interrupt, an event on this I/O can generate an external interrupt request to the CPU.

Each pin can independently generate an interrupt request. The interrupt sensitivity is independently programmable using the sensitivity bits in the EICR register.

External interrupts are hardware interrupts. Fetching the corresponding interrupt vector automatically clears the request latch. Changing the sensitivity of a particular external interrupt clears this pending interrupt. This can be used to clear unwanted pending interrupts.

Obsolete Product(s) - Obsolete Product(s)

Bit 2 **WDGRF** *Force Reset/ Reset Status Flag*

This bit is used in two ways: it is set by software to force a watchdog reset. It is set by hardware when a watchdog reset occurs and cleared by hardware or by software. It is cleared by hardware only when an LVD reset occurs. It can be cleared by software after a read access to the LTCSR register.

0: No watchdog reset occurred.

1: Force a watchdog reset (write), or, a watchdog reset occurred (read).

Bit 1 **WDGE** *Watchdog Enable*

This bit is set and cleared by software.

0: Watchdog disabled

1: Watchdog enabled

Bit 0 **WDGD** *Watchdog Reset Delay*

This bit is set by software. It is cleared by hardware at the end of each WDG period.

0: Watchdog reset not delayed

1: Watchdog reset delayed

Lite Timer Input Capture register (LTICR)

Reset value: 0000 0000 (00h)

7							0
ICR7	ICR6	ICR5	ICR4	ICR3	ICR2	ICR1	ICR0
Read only							

Bit 7:0 **ICR[7:0]** *Input capture value*

These bits are read by software and cleared by hardware after a reset. If the ICF bit in the LTCSR is cleared, the value of the 8-bit up-counter will be captured when a rising or falling edge occurs on the LTIC pin.

Table 26. Lite timer register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0B	**LTCSR** Reset value	ICIE 0	ICF 0	TB 0	TBIE 0	TBF 0	WDGRF x	WDGE 0	WDGD 0
0C	**LTICR** Reset value	ICR7 0	ICR6 0	ICR5 0	ICR4 0	ICR3 0	ICR2 0	ICR1 0	ICR0 0

Obsolete Product(s) - Obsolete Product(s)

10.2 12-bit auto-reload timer (AT)

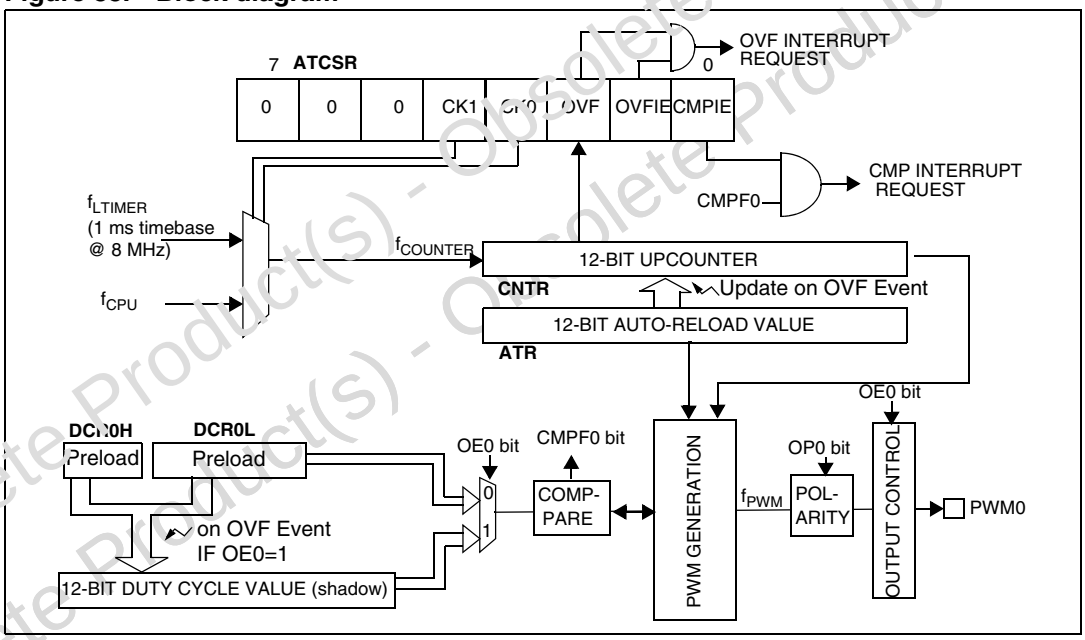
10.2.1 Introduction

The 12-bit auto-reload timer can be used for general-purpose timing functions. It is based on a free-running 12-bit upcounter with a PWM output channel.

10.2.2 Main features

- 12-bit upcounter with 12-bit auto-reload register (ATR)
- Maskable overflow interrupt
- PWM signal generator
- Frequency range 2 kHz - 4 MHz (@ 8 MHz f_{CPU})
  - Programmable duty-cycle
  - Polarity control
  - Maskable compare interrupt
- Output compare function

Figure 33. Block diagram



10.2.3 Functional description

PWM mode

This mode allows a pulse width modulated signals to be generated on the PWM0 output pin with minimum core processing overhead. The PWM0 output signal can be enabled or disabled using the OE0 bit in the PWMCR register. When this bit is set the PWM I/O pin is configured as output push-pull alternate function.

Note: CMPF0 is available in PWM mode (see Section : PWM0 control/status register (PWM0CSR)).

Obsolete Product(s) - Obsolete Product(s)

PWM0 control/status register (PWM0CSR)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	OP0	CMPF0
Read/Write							

Bit 7:2 Reserved, must be kept cleared.

Bit 1 **OP0** *PWM0 output polarity.*
This bit is read/write by software and cleared by hardware after a reset. This bit selects the polarity of the PWM0 signal.
0: The PWM0 signal is not inverted.
1: The PWM0 signal is inverted.

Bit 0 **CMPF0** PWM0 *Compare Flag.*
This bit is set by hardware and cleared by software by reading the PWM0CSR register. It indicates that the upcounter value matches the DCR0 register value.
0: Upcounter value does not match DCR value.
1: Upcounter value matches DCR value.

PWM output control register (PWMCR)

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	0	OE0
Read/Write							

Bits 7:1 Reserved, must be kept cleared.

Bit 0 **OE0** *PWM0 Output enable*.
This bit is set and cleared by software.
0: PWM0 output Alternate Function disabled (I/O pin free for general purpose I/O)
1: PWM0 output enabled

Table 30. Register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0D	**ATCSR** Reset value	0	0	0	CK1 0	CK0 0	OVF 0	OVFIE 0	CMPIE 0
0E	**CNTRH** Reset value	0	0	0	0	CN11 0	CN10 0	CN9 0	CN8 0
0F	**CNTRL** Reset value	CN7 0	CN6 0	CN5 0	CN4 0	CN3 0	CN2 0	CN1 0	CN0 0
10	**ATRH** Reset value	0	0	0	0	ATR11 0	ATR10 0	ATR9 0	ATR8 0

Obsolete Product(s) - Obsolete Product(s)

cycles) and the C_{ADC} sample capacitor is disconnected from the analog input pin to get the optimum analog to digital conversion accuracy.

- The total conversion time:
  $t_{CONV} = t_{SAMPLE} + t_{HOLD}$

While the ADC is on, these two phases are continuously repeated.

At the end of each conversion, the sample capacitor is kept loaded with the previous measurement load. The advantage of this behavior is that it minimizes the current consumption on the analog pin in case of single input channel measurement.

A/D conversion

The analog input ports must be configured as input, no pull-up, no interrupt. Refer to the “I/O ports” chapter. Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the ADCCSR register, select the CS[2:0] bits to assign the analog channel to convert.

ADC conversion mode

In the ADCCSR register, set the ADON bit to enable the A/D converter and to start the conversion. From this time on, the ADC performs a continuous conversion of the selected channel. When a conversion is complete:

- The EOC bit is set by hardware.
- The result is in the ADCDR registers.

A read to the ADCDRH resets the EOC bit.

To read the 10 bits, perform the following steps:

1. Poll EOC bit
2. Read ADCDRL
3. Read ADCDRH. This clears EOC automatically.

To read only 8 bits, perform the following steps:

1. Poll EOC bit
1. Read ADCDRH. This clears EOC automatically.

10.3.4 Low power modes

The A/D converter may be disabled by resetting the ADON bit. This feature allows reduced power consumption when no conversion is needed and between single shot conversions.

Table 31. Effect of low power modes

Mode	Description
Wait	No effect on A/D converter
Halt	A/D converter disabled. After wakeup from Halt mode, the A/D converter requires a stabilization time t_{STAB} (see *Section 12: Electrical characteristics*) before accurate conversions can be performed.

Obsolete Product(s) - Obsolete Product(s)

12.4.3 On-chip peripherals

Table 54. On-chip peripheral characteristics

Symbol	Parameter	Conditions		Typ (1)	Unit
$I_{DD(AT)}$	12-bit auto-reload timer supply current (2)	f_{CPU} = 4 MHz	V_{DD}= 3.0 V	15	µA
		f_{CPU} = 8 MHz	V_{DD}= 5.0 V	30	
$I_{DD(ADC)}$	ADC supply current when converting (3)	f_{ADC} = 2 MHz	V_{DD}= 3.0 V	450	
		f_{ADC} = 4 MHz	V_{DD}= 5.0 V	750	

1. Not tested in production, guaranteed by characterization.
2. Data based on a differential I_{DD} measurement between reset configuration (timer stopped) and the timer running in PWM mode at f_{cpu} = 8 MHz.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions with amplifier off.

12.5 Clock and timing characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

Table 55. General timings

Symbol	Parameter(1)	Conditions	Min	Typ(2)	Max	Unit
$t_{c(INST)}$	Instruction cycle time	f_{CPU}=8 MHz	2	3	12	t_{CPU}
			250	375	1500	ns
$t_{v(IT)}$	Interrupt reaction time(3) $t_{v(IT)} = \Delta t_{c(INST)} + 10$	f_{CPU}=8 MHz	10		22	t_{CPU}
			1.25		2.75	µs

1. Data based on characterization. Not tested in production.
2. Data based on typical application software.
3. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

Table 56. Auto-wakeup RC oscillator

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage Range		2.4	5.0	5.5	V
Operating Temperature Range		-40	25	125	°C
Current Consumption(1)	Without prescaler	2.0	8.0	14.0	µA
Consumption(1)	AWU RC switched off		0		µA
Output Frequency(1)		20	33	60	kHz

1. Data guaranteed by design.

Obsolete Product(s) - Obsolete Product(s)

12.7.2 Electromagnetic Interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 60. EMI characteristics(1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC}/f_{CPU}]	Unit
				-/8 MHz	
S_{EMI}	Peak level	V_{DD}=5 V, T_A=+25 °C, SO8 package, conforming to SAE J 1752/3	0.1 MHz to 30 MHz	21	dBµV
			30 MHz to 130 MHz	23	
			130 MHz to 1 GHz	10	
			SAE EMI Level	3	-

1. Data based on characterization results, not tested in production.

12.7.3 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human Body Model. This test conforms to the JESD22-A114A/A115A standard.

Table 61. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25°C	> 4000	V

1. Data based on characterization results, not tested in production.

Static and dynamic latchup

- **LU**: 3 complementary static tests are required on 10 parts to assess the latchup performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latchup standard. For more details, refer to the application note AN1181.
- **DLU**: Electrostatic discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latchup performance in

Obsolete Product(s) - Obsolete Product(s)

13 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

13.1 Package mechanical data

Figure 65. 8-lead very thin fine pitch dual flat no-lead package outline

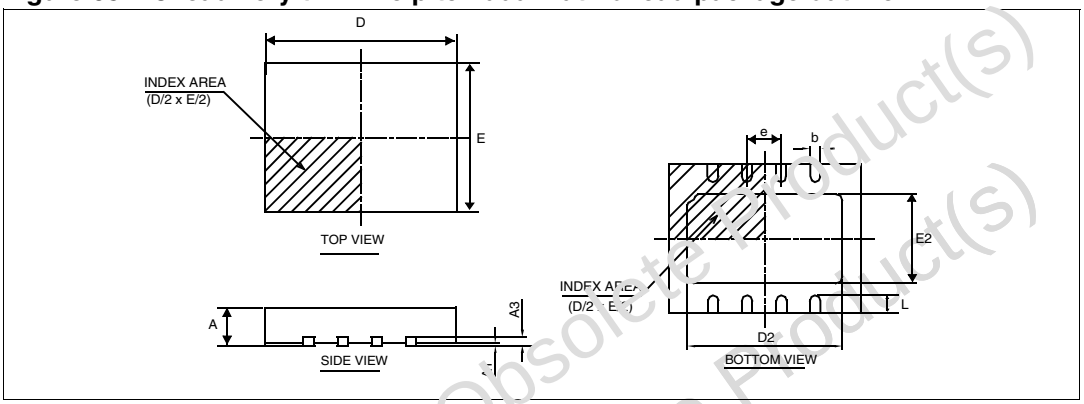


Table 70. 8-lead very thin fine pitch dual flat no-lead package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0310	0.0350	0.0390
A1	0.00	0.02	0.05	0.0000	0.0010	0.0020
A3		0.20			0.0080	
b	0.25	0.30	0.35	0.0100	0.0120	0.0140
D		4.50			0.1770	
D2	3.50	3.65	3.75	0.1380	0.1440	0.1480
E		3.50			0.1380	
E2	1.96	2.11	2.21	0.0770	0.0830	0.0870
e		0.80			0.0310	
L	0.30	0.40	0.50	0.0120	0.0160	0.0200
	Number of pins					
N	8					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Obsolete Product(s) - Obsolete Product(s)

Table 75. Startup clock selection

Configuration	CKSEL1	CKSEL0
Internal RC as Startup Clock	0	0
Reserved	0	0
AWU RC as a Startup Clock	0	1
Reserved	1	0
External Clock on pin PA5	1	1

Table 76. LVD threshold configuration

Configuration	LVD1	LVD0
LVD Off	1	1
Highest voltage threshold	1	0
Medium voltage threshold	0	1
Lowest voltage threshold	0	0

14.1.2 OPTION BYTE 0

Bits 7:4 Reserved, must always be 1.

Bit 3 Reserved, must always be 0.

Bit 2 **SEC0** *Sector 0 size definition*
This option bit indicates the size of sector 0 according to the following table (see *Table 77: Definition of sector 0 size*).

Bit 1 **FMP_R** *Readout protection*
Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Erasing the option bytes when the FMP_R option is selected will cause the whole memory to be erased first, and the device can be reprogrammed. Refer to *Section 4.5* and the ST7 Flash Programming Reference Manual for more details.
0: Readout protection off
1: Readout protection on

Bit 0 **FMP_W** *FLASH write protection*
This option indicates if the FLASH program memory is write protected.
Warning: When this option is selected, the program memory (and the option bit itself) can never be erased or programmed again.
0: Write protection off
1: Write protection on

Table 77. Definition of sector 0 size

Sector 0 Size	SEC0
0.5k	0
1k	1

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16 Revision history

Table 82. Document revision history

Date	Revision	Changes
06-Feb-06	1	Initial release
18-Apr-06	2	Removed references to 3% RC Added note below *Figure 4* Modified presentation of *Section 4.3.1* Added notes to *Section 6.2* (above *Figure 9*), replaced 8-bit calibration value to 10-bit calibration value and changed application note reference (AN2326 instead of AN1324) Modifed *Table 7: Clock register map and reset values* and added b t 1 in the description of CKCNTCSR register Modified Figure 13 (added CKCNTCSR register) Added note 2 to EICRx description Modified caution in section 7.2 on page 25 Replaced $V_{IT+(LVD)}$ by $V_{IT+(LVD)}$ in *Section : Monitoring the VDD main supply* Modified LVDRF bit description in *Section 7.4.4: Register description* Replaced “oscillator” by “main oscillator” in the second paragraph of *Section 8.4.2: Halt mode* Added note 1 to *Figure 23* and added note 5 to *Figure 24* Modified *Section 8.5: Auto-wakeup from Halt mode* Replaced bit 1 by bit 2 for AWUF bit in *Section 8.5.1: Register description* Modified *Section 9.1: Introduction*. Modified *Section : External interrupt function*.Updated *Section 9.5: Interrupts*. Modified *Section Table 47.: Operating conditions with low voltage detector (LVD)*. Modified *Table 48: Auxiliary Voltage Detector (AVD) Thresholds*. Modified *Table 49: Voltage drop between AVD flag set and LVD reset generation*. Modified *Table 50: Internal RC oscillator calibrated at 5 V*. Modified *Table 53: Supply current*. Modified *Table 54: On-chip peripherals*. Modified *Table 63: General characteristics*. Modified *Table 64: Output driving current*. Modified *Table 65: Asynchronous RESET pin characteristics*. Modified *Section 12.10: ADC characteristics*. Added *Figure 49*. Modified *Figure 61*. Removed EMC protection circuitry in *Figure 62* (device works correctly without these components). Added ECOPACK text in *Section 13: Package characteristics*. Modified first paragraph in *Section 14: Device configuration and ordering information*. Modified *Table 79*. Modified conditioning option in option list. Modified *Section 14.3: Development tools*. Added *Section 14.4: ST7 application notes*. Added *Section :* . Added erratasheet at the end of the document.

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