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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	5MHz
Connectivity	-
Peripherals	LED, POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c1505vscr2306

GENERAL DESCRIPTION (Continued)

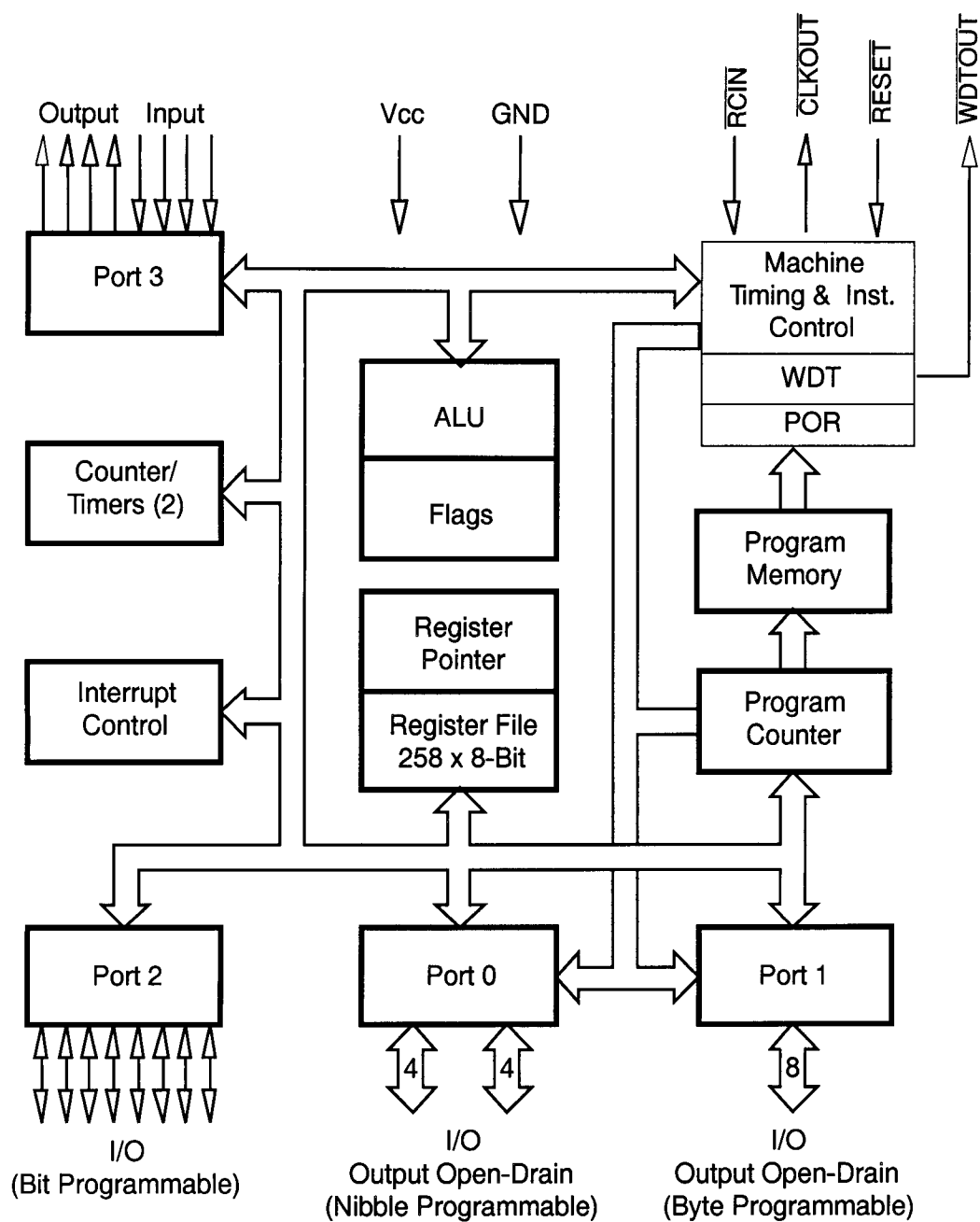
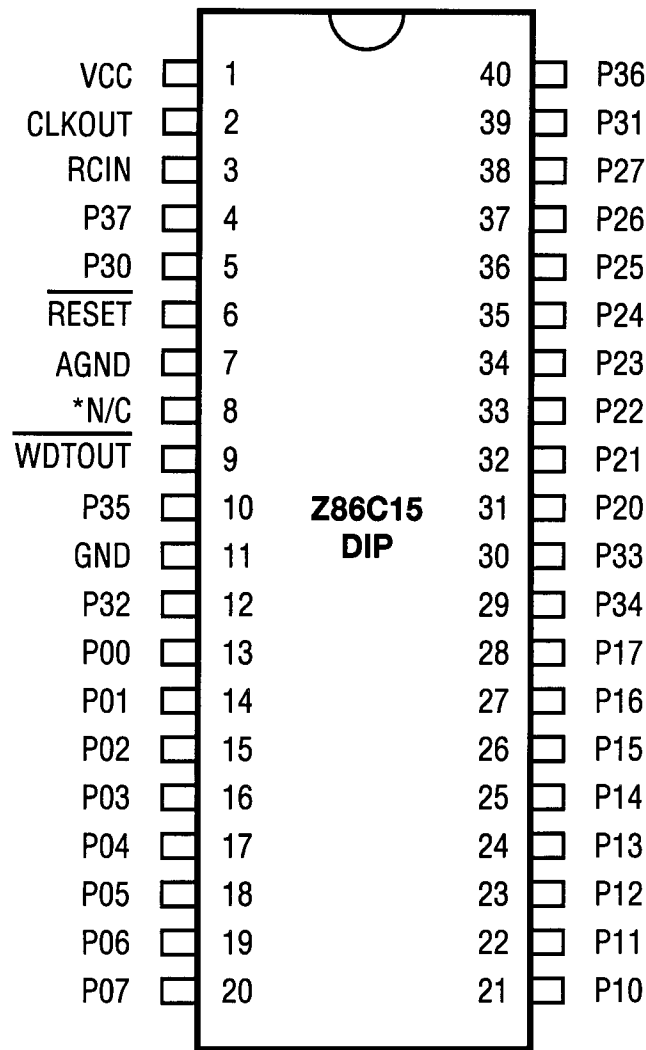


Figure 1. Z86C15 Functional Block Diagram

PIN IDENTIFICATION



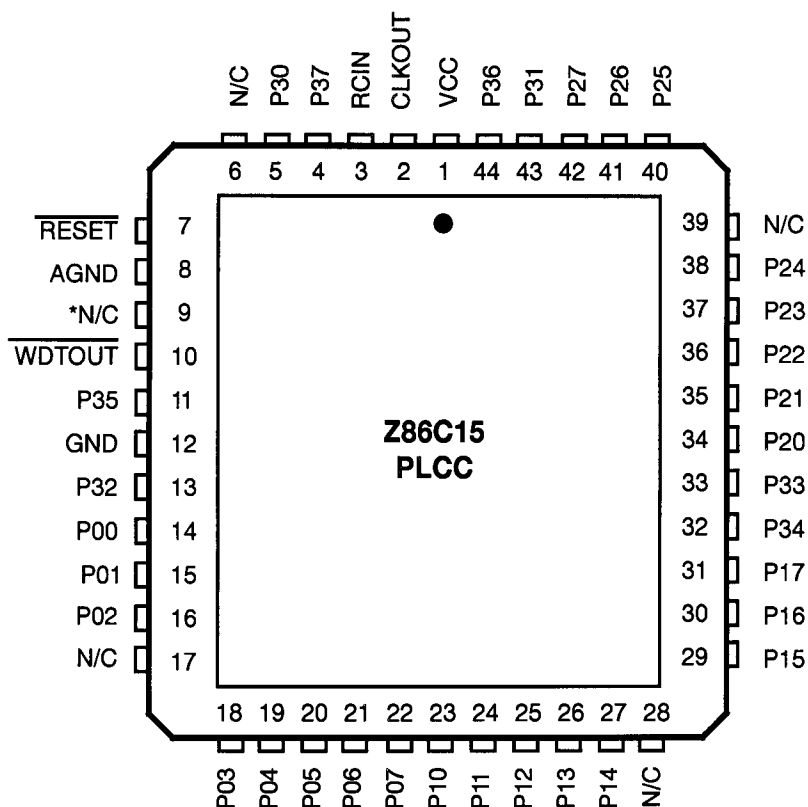
Note: Pin 8 is connected to the chip, although it is used only for testing. This pin **must** float.

Figure 2. 40-Pin DIP Pin Configuration

Table 1. 40-Pin DIP Identification			
Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input
2	CLKOUT	Z8 System Clock	Output
3	RCIN	RC Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	RESET	Reset	Input
7	AGND	Analog Ground	
*8	N/C	Not Connected	
9	WDTOUT	Watch-Dog Timer	Output

Table 1. 40-Pin DIP Identification			
Pin #	Symbol	Function	Direction
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
21-28	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P27-P20	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

PIN IDENTIFICATION (Continued)



***Note:** Pin 9 is connected to the chip, although it is used only for testing. This pin *must* float.

Figure 3. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input
2	CLKOUT	Z8 System Clock	Output
3	RCIN	RC Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	
7	RESET	Reset	Input
8	AGND	Analog Ground	
*9	N/C	Not Connected	
10	WDTOUT	Watch-Dog Timer	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P02/P00	Port 0, Pins 0, 1, 2	In/Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
17	N/C	Not Connected	
18-22	P07-P03	Port 0, Pins 3, 4, 5, 6, 7	In/Output
23-27	P14-P10	Port 1, Pins 0, 1, 2, 3, 4	In/Output
28	N/C	Not Connected	
29-31	P17-P15	Port 1, Pins 5, 6, 7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P24-P20	Port 2, Pins 0, 1, 2, 3, 4	In/Output
39	N/C	Not Connected	
40-42	P27-P25	Port 2, Pins 5, 6, 7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V _{CC}	Supply Voltage*	−0.3	+7.0	V
T _{STG}	Storage Temp	−65	+150	°C
T _A	Oper Ambient Temp	0	+105	°C

* Voltage on all pins with respect to GND.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed here apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).

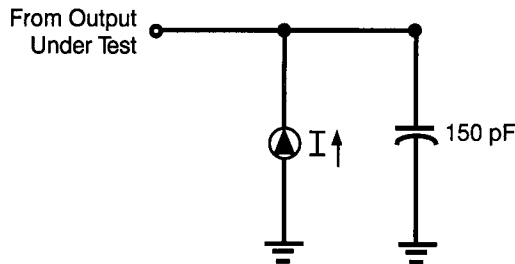


Figure 5. Test Load Diagram

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Max
Input Capacitance	12 pF
Output Capacitance	12 pF
I/O Capacitance	12 pF

FREQUENCY

Frequency 4 MHz – 5 MHz

Tolerance ±10%

Frequency tolerance limit only applies to the packaged device and not die or wafer.

DC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\% @ 0^{\circ}C \text{ to } +70^{\circ}C$

Sym	Parameter	Min	Max	Typical @ 25°C	Unit	Condition	Notes
V_{CH}	Clock Input High Voltage	$0.7 V_{CC}$	$V_{CC} + 0.3V$	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	$GND - 0.3$	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V		
V_{IL}	Input Low Voltage	$GND - 0.3$	$0.2V_{CC}$	1.5	V		
V_{RH}	Reset Input High Voltage	$0.8 V_{CC}$	V_{CC}	2.1	V		
V_{RL}	Reset Input Low Voltage	$GND - 0.3$	$0.2 V_{CC}$	1.7	V		
V_{OH}	Output High Voltage	$V_{CC} - 0.4$		3.1	V	$I_{OH} = -2.0 \text{ mA}$	
V_{OH}	Output High Voltage	$V_{CC} - 0.6$			V	$I_{OH} = -2.0 \text{ mA}$	1
V_{OL}	Output Low Voltage		0.8		V	$I_{OL} = 4 \text{ mA}$	1
V_{OL}	Output Low Voltage		0.4		V	$I_{OL} = 4 \text{ mA}$	
I_{OL}	Output Low	10	20		mA	$V_{OL} = V_{CC} - 2.2 \text{ V}$	1
I_{IL}	Input Leakage	-1	1	<1	μA	$V_{IN} = 0V, 5.25V$	2
I_{OL}	Output Leakage	-1	1	<1	μA	$V_{IN} = 0V, 5.25V$	
I_{CC}	V_{CC} Supply Current		12	6	mA	@ 5.0 MHz	
POR	Power On Reset	80	160	120	ms		
I_{CC1}	Standby Current		4	2.0	mA	HALT Mode $V_{IN} = 0V, V_{CC} @ 5 \text{ MHz}$	
I_{CC2}	Standby Current		20		μA	STOP Mode $V_{IN} = 0V$	
R_P	Pull Up Resistor	6.76	14.04	10.4	Kohm		
R_P	Pull Up Resistor (P26-P27)	1.8	3	2.4	Kohm		
R_P	Pull Up Resistor (Reset)		40	80	60 Kohm		

Notes:

1. Ports P37-P34. These may be used for LEDs or as general-purpose outputs requiring high sink current.
2. Input pin without pull-up resistor.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table

				$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			
				V_{CC}	5 MHz		
No	Symbol	Parameter	Note [4]	Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0V	125	100000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		25	ns	1
3	TwC	Input Clock Width	5.0V	37		ns	1
4	TwTinL	Timer Input Low Width	5.0V	70		ns	1
5	TwTinH	Timer Input High Width	5.0V	2.5TpC			1
6	TpTin	Timer Input Period	5.0V	4TpC			1
7	TrTin	Timer Input Rise & Fall Timer	5.0V		100	ns	1
8A	TwIL	Int. Request Low Time	5.0V	70		ns	1,2
8B	TwIL	Int. Request Low Time	5.0V	3TpC			1,3
9	TwIH	Int. Request Input High Time	5.0V	3TpC			1,2
10	Twsm	STOP Mode Recovery Width Spec	5.0V	20		ns	Reg. SMR - D5=0
			5.0V	5TpC			Reg. SMR- D5=1
11	Tost	Oscillator Startup Time	5.0V		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time	5.0V	2		ms	5
			5.0V	4		ms	6
			5.0V	8		ms	7
			5.0V	32		ms	8
13	POR	Power On Reset Delay	5.0V	84	196	ms	

Notes:

1. Timing Reference uses 0.7 VCC for a logic 1 and 0.2 VCC for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. D1 = 0, D0 = 0.(Reg. WDTMR)
6. D1 = 0, D0 = 1 (Reg. WDTMR)
7. D1 = 1, D0 = 0.(Reg. WDTMR)
8. D1 = 1, D0 = 1.(Reg. WDTMR)

AC ELECTRICAL CHARACTERISTICS

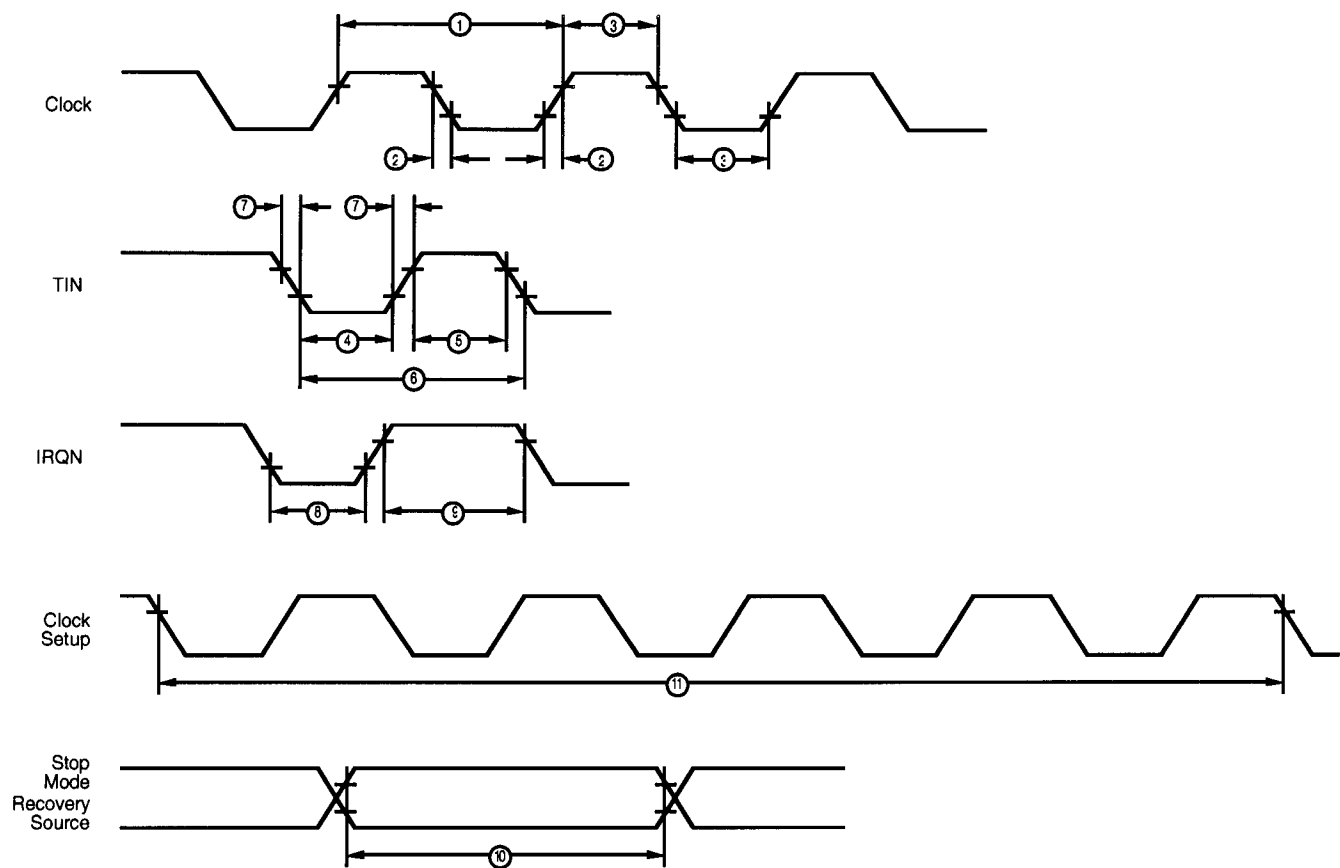


Figure 6. Additional Timing Diagram

PIN FUNCTIONS

RCIN. This pin, connected between a precision resistor and the power supply, forms the precision RC oscillator.

CLKOUT. This pin is the system clock of the Z8® MCU and runs at the frequency of the RC oscillator.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble-programmable, bidirectional, CMOS-compatible I/O port. These eight I/O

lines can be configured under software control as a nibble input port, or as a nibble open-drain output port. Inputs have standard CMOS (Figure 7). Port P00-P03 has

10.4 Kohm ($\pm 35\%$) pull-up resistor when configured as inputs.

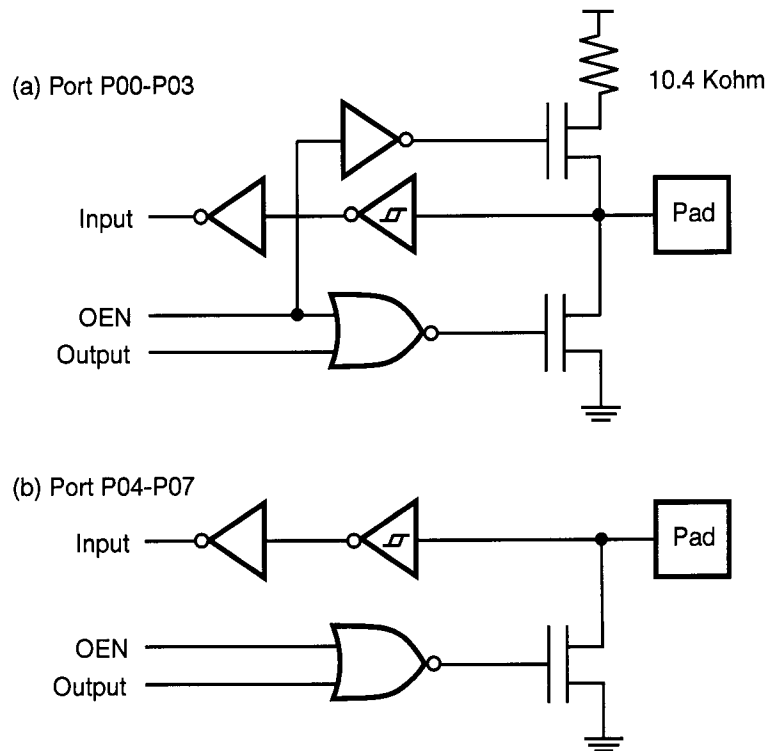
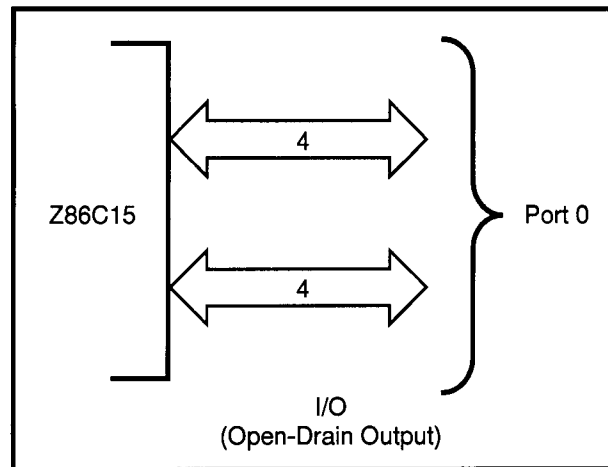


Figure 7. Port 0 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible four-fixed-input (P33-P30) and four-fixed-output (P37-P34) I/O port. Port 3 outputs have 10.4 Kohm pull-up resistances and are capable of directly driving up to four LEDs of output. (Voltage on Port 3 is 2.8V @ 20 mA.)

Port 3 is configured under software control to provide the following control functions: four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (TIN and TOUT - Figure 10).

RESET (input, active Low). When activated, **RESET** initializes the Z86C15. When **RESET** is deactivated, program execution begins from the internal program location at 000CH. Reset pin has a 10.4 Kohm ($\pm 35\%$) pull-up resistor. When this pin is pulled Low, it takes 150 ms for the Z86C15 to initialize (POR).

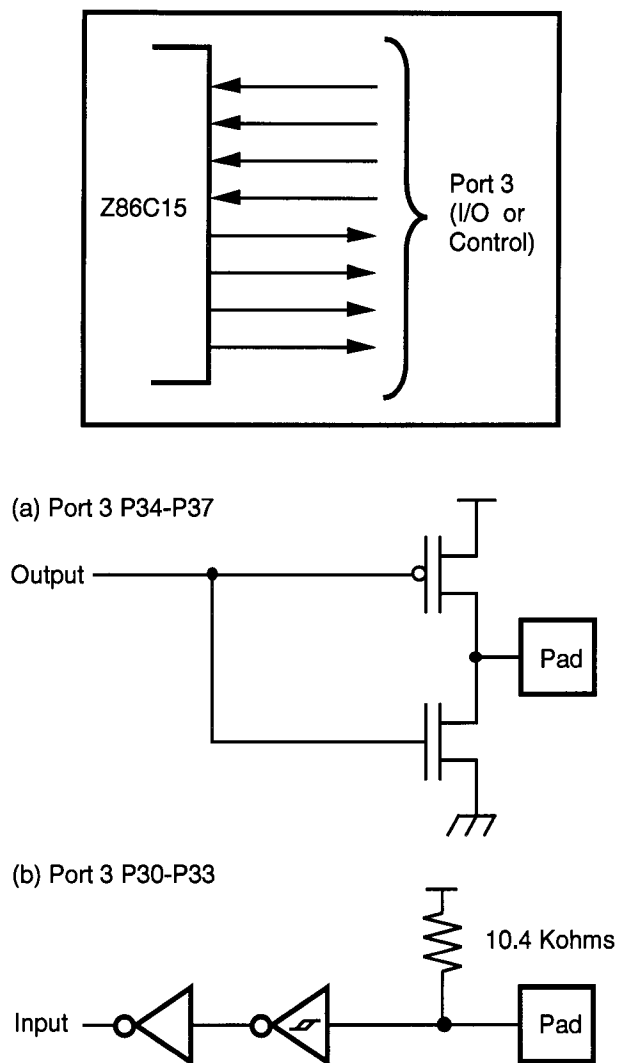


Figure 10. Port 3 Configuration

FUNCTIONAL DESCRIPTION

Program Memory. The 16-bit program counter addresses 4 KB of program memory space at internal locations (Figure 11).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations have six 16-bit vectors that correspond to the six available interrupts.

Byte 12 to byte 4095 consists of on-chip, mask programmed ROM. Addresses 4096 and greater are reserved.

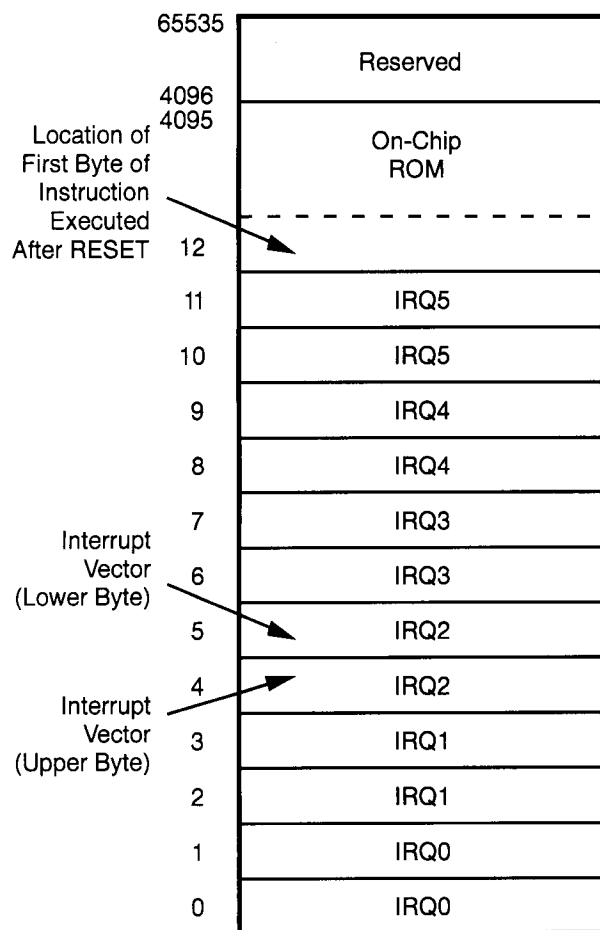


Figure 11. Program Memory Map

Register File. The register file consists of four I/O port registers, 236 general-purpose registers and 15 control and status registers (R0-R3, R4-239 and R240-R255, respectively), plus two system configuration registers in the expanded register group. The instructions access registers directly or indirectly via an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 12). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

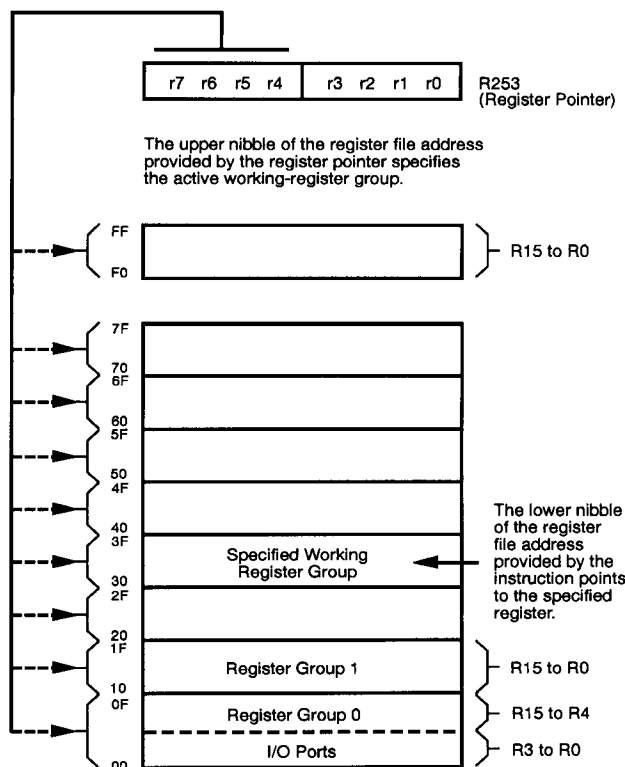


Figure 12. Register Pointer Register

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

The 4 KB program memory is mask programmable. A ROM protect feature prevents “dumping” of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to Program Memory in all modes.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group (Figure 13). These register groups are known as the Expanded Register File (ERF). Bits 7-4 of the RP Register select the working register group. Bits 3-0 of the RP Register select the expanded register group (Figure 13). Two system configuration registers reside in the Expanded Register File at Bank F. The rest of the Expanded Register is not physically implemented and is open for future expansion

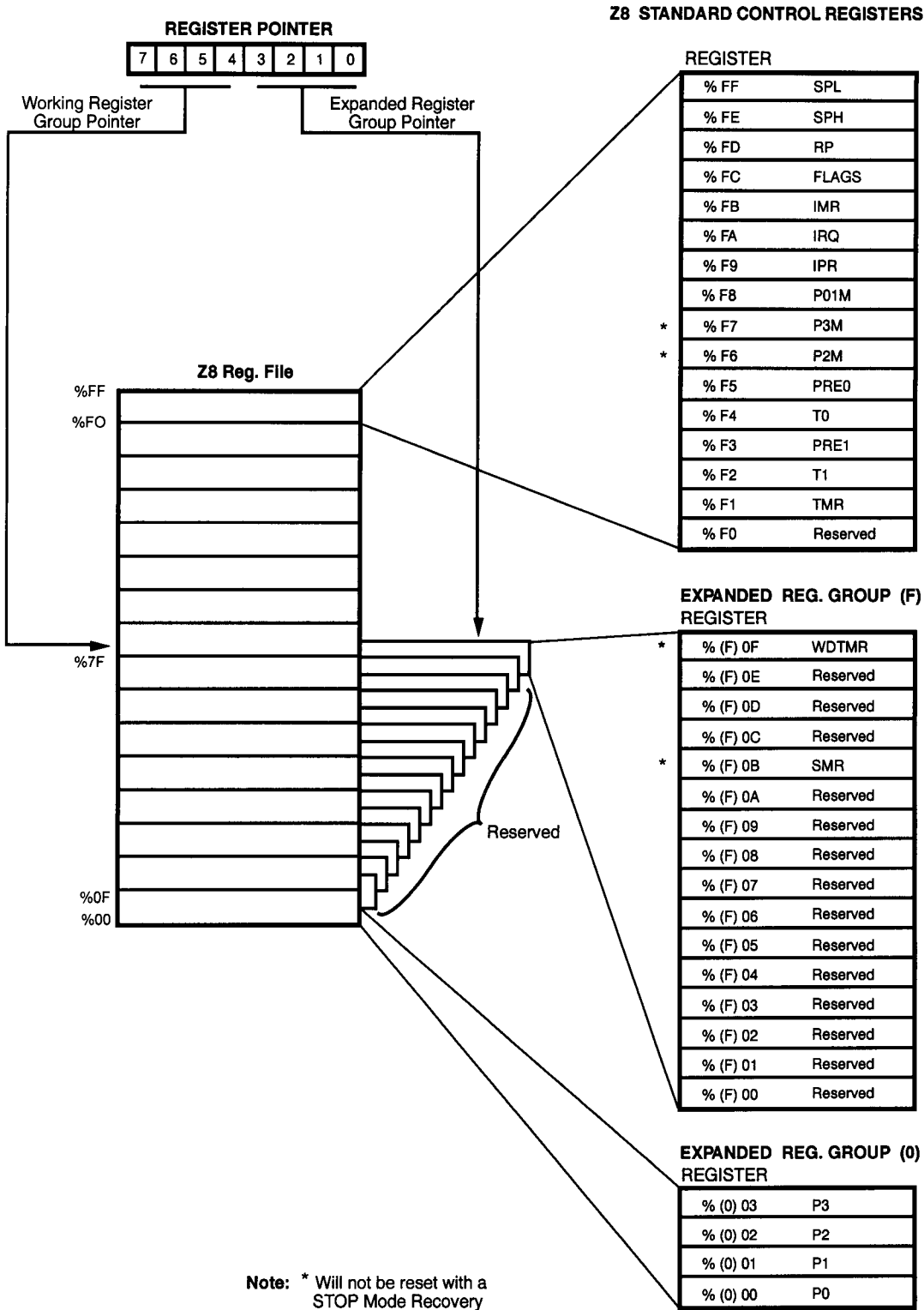


Figure 13. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 14).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its own counter, which decrements the value (1 to 256) that has been loaded into the counter.

When both the counter and prescaler reach the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

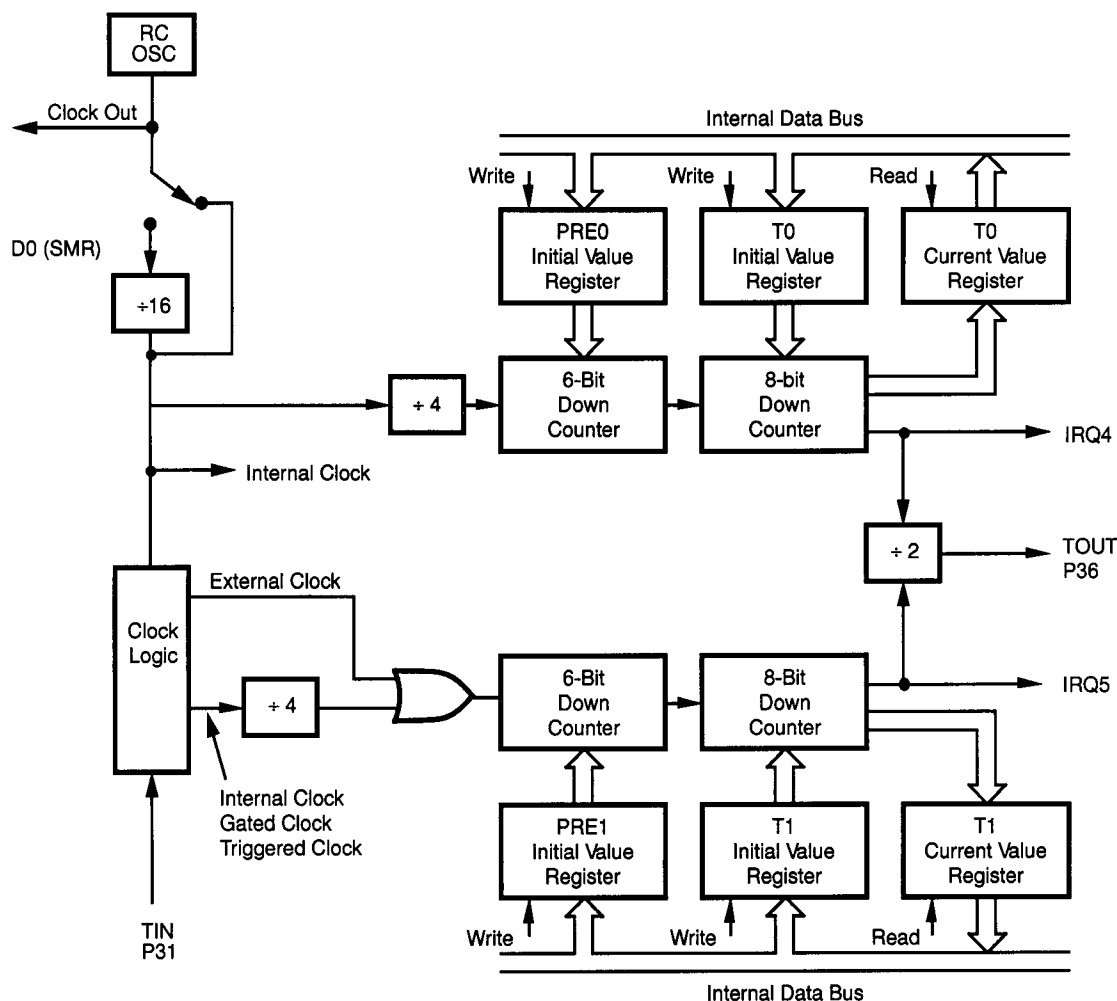


Figure 14. Counter/Timers Block Diagram

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input as an external clock, a trigger input that can be retriggerable or non-triggerable, or as a gate input for the internal clock. The counter/timers can be programmable cascaded by connecting the T0 output to the input of T1. Port 3 lines P36 also serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock are output.

Interrupts. The Z86C15 has six different interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two are claimed by the counter/timers. The Interrupt Masked Register globally or individually enables or disables the six interrupts requests.

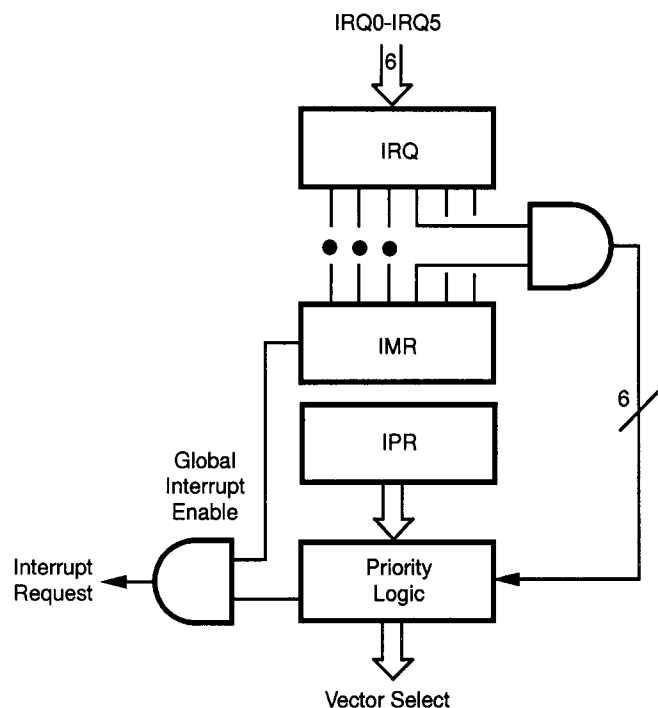


Figure 15. Interrupt Block Diagram

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When

an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and status flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt request needs service.

EMI. Lower EMI on the Z86C15 is achieved through circuit modifications. The internal divide-by-two circuit has been removed to further reduce EMI.

RC Oscillator. The Z86C15 provides an internal capacitor to accommodate an RC oscillator configuration. A 1% precision resistor is necessary to achieve 10% accurate frequency oscillation.

The Z86C15 also accepts external clock from Pin 3 and Pin 7.

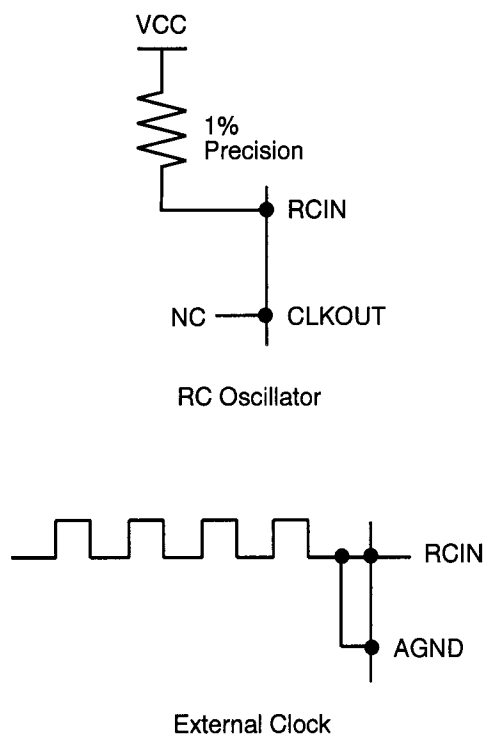


Figure 16. RC Oscillator Configuration

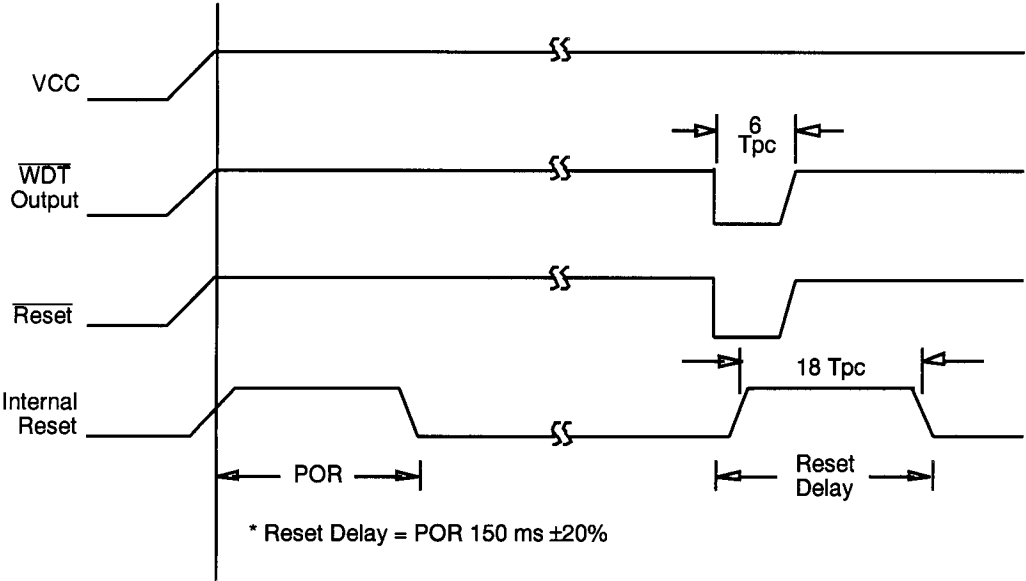


Figure 18. WDT Turn-On Timing After Reset

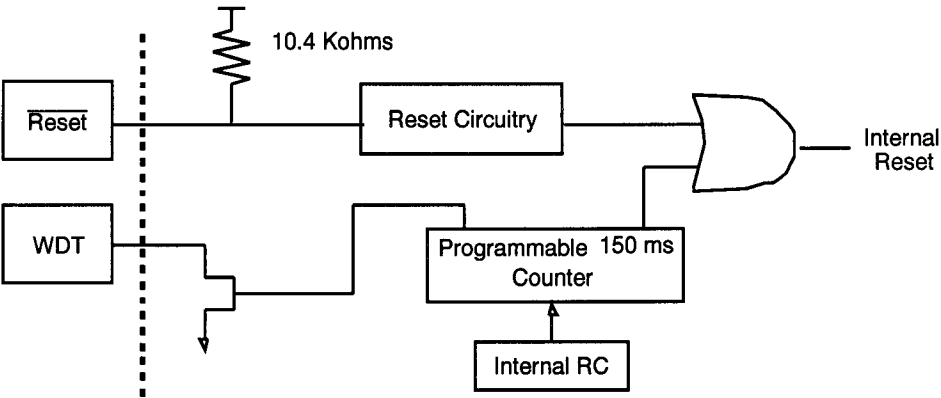


Figure 19. WDT Block Diagram

Stop-Mode Recovery Source (D2, D3, and D4). Bits 2, 3, and 4 of the SMR register specify the wake-up source of the Stop-Mode Recovery signal (Table 4 and Figure 21).

Table 4. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or External Reset Recovery
0	0	1	Logical NAND P00-P03,P30-P33,P24-P26
0	1	0	P31 Transition
0	1	1	P32 Transition
1	0	0	P33 Transition
1	0	1	P27 Transition
1	1	0	Logical NOR of P20-P23
1	1	1	Logical NAND of P00-P03, P31, P33, P24, P25, P26

Stop-Mode Recovery Delay Select (D5). Bit 5 controls the reset delay after recovery. The default configuration of this bit is 1, which enables a 150 ms **RESET** delay after Stop-Mode Recovery. If this bit is set to 0, the “fast” wake up is selected and the STOP-Mode Recovery source is kept active for at least 5 TpC.

Stop-Mode Recovery Edge Select (D6). Bit 6 controls whether a low level or a high level is required from the recovery source. The default configuration of this bit is 0. A 1 indicates that a high level on any one of the recovery sources wakes the Z86C15 from STOP Mode. A 0 indicates a low level recovery. The default is 0 on POR.

Cold or Warm Start (D7). This bit is set upon entering STOP Mode. A 0 (cold) indicates that the device is awakened by a POR/WDT RESET. A 1 (warm) indicates that the device is awakened by a SMR source.

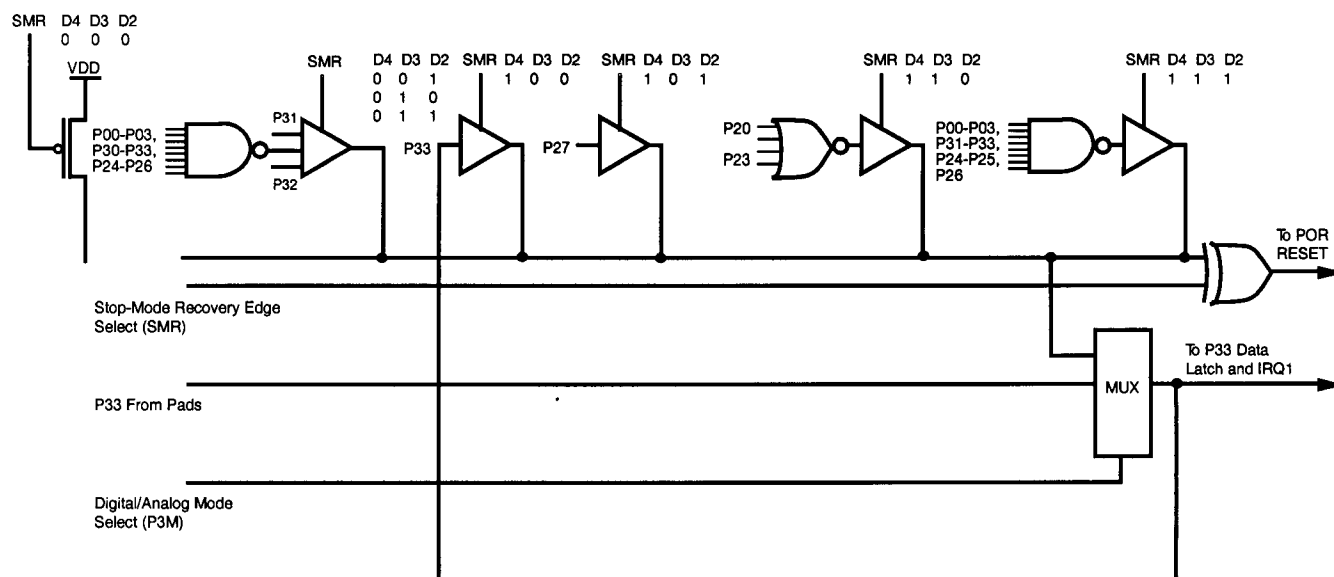
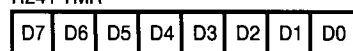


Figure 21. Stop-Mode Recovery Source

Z8 CONTROL REGISTER DIAGRAMS

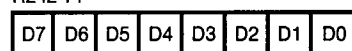
R241 TMR



- 0 = No Function
1 = Load T0
- 0 = Disable T0 Count
1 = Enable T0 Count
- 0 = No Function
1 = Load T1
- 0 = Disable T1 Count
1 = Enable T1 Count
- TIN Modes
00 = External Clock Input
01 = Gate Input
10 = Trigger Input (Non-retriggerable)
11 = Trigger Input (Retriggerable)
- TOUT Mode
00 = Not Used
01 = T0 OUT
10 = T1 OUT
11 = Internal Clock Out

**Figure 22. Timer Mode Register
(F1H: Read/Write)**

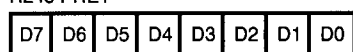
R242 T1



- T1 Initial Value
(When WRITE)
(Range 1-256 Decimal
01-00 HEX)
- T1 Current Value
(When READ)

**Figure 23. Counter Timer 1 Register
(F2H: Read/Write)**

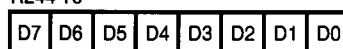
R243 PRE1



- Count Mode
0 = T1 Single Pass
1 = T1 Modulo N
- Clock Source
1 = T0 Internal
0 = T0 External Timing Input
(TIN) Mode
- Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)

**Figure 24. Prescaler 1 Register
(FSH: Write Only)**

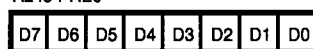
R244 T0



- T0 Initial Value
(When WRITE)
(Range: 1-256 Decimal
01-00 HEX)
- T0 Current Value
(When READ)

**Figure 25. Counter/Timer 0 Register
(F4H: Read/Write)**

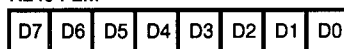
R245 PRE0



- Count Mode
0 = T0 Single Pass
1 = T0 Modulo N
- Reserved (Must be 0)
- Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)

**Figure 26. Prescaler 0 Register
(F5H: Write Only)**

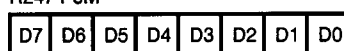
R246 P2M



- P20-P27 I/O Definition
0 Defines Bit as OUTPUT
1 Defines Bit as INPUT

**Figure 27. Port 2 Mode Register
(F6H: Write Only)**

R247 P3M



- 0 Port 2 Pull-Ups Open-Drain
1 Port 2 Pull-Ups Active
- Reserved (Must be 0)

**Figure 28. Port 3 Mode Register
(F7H: Write Only)**

PACKAGE INFORMATION

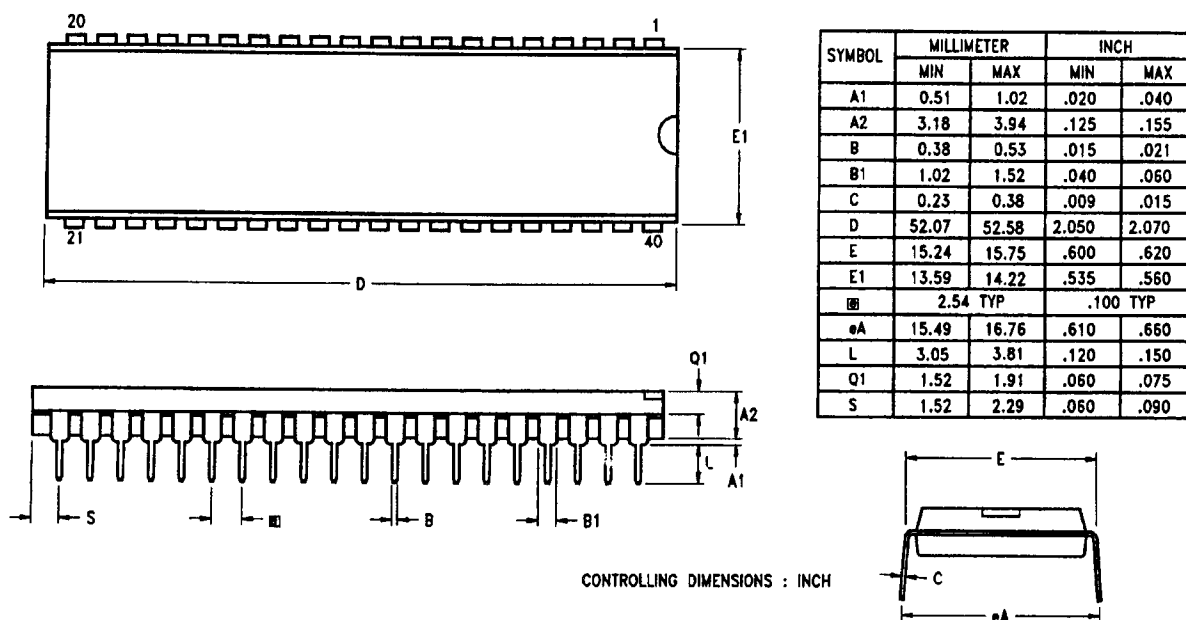


Figure 39. 40-Pin DIP Package Diagram

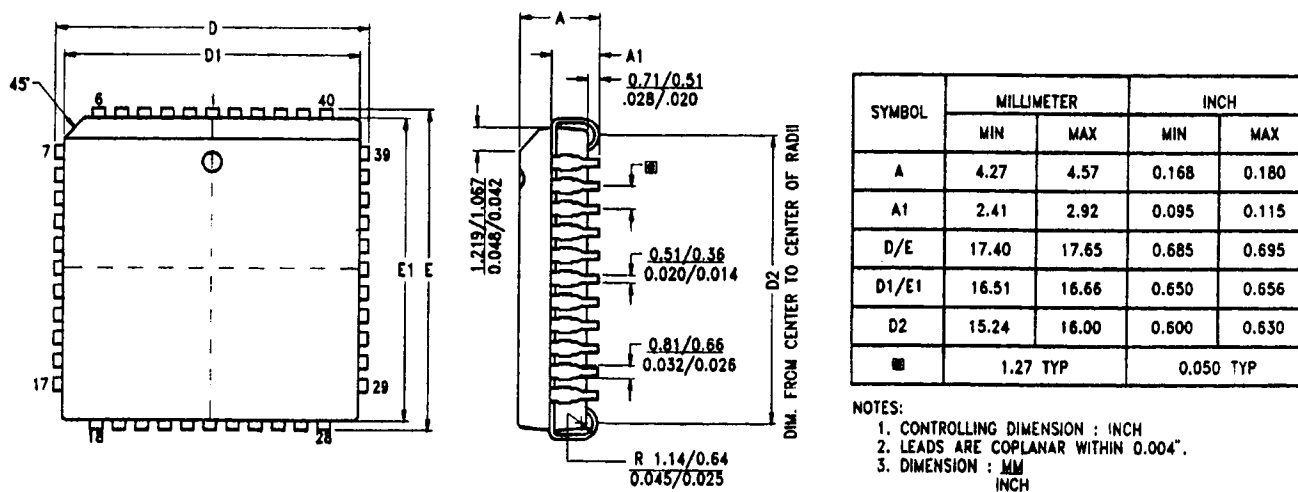
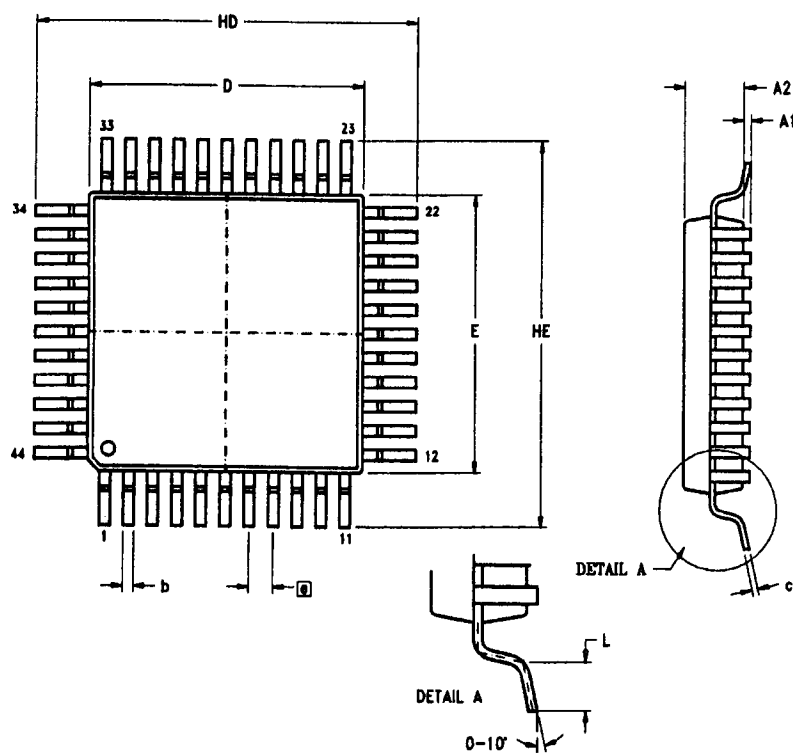


Figure 40. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
Ⓢ	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
 1. CONTROLLING DIMENSIONS : MILLIMETER
 2. LEAD COPLANARITY : MAX $\frac{.10}{.004}$

Figure 41. 44-Pin QFP Package Diagram

ORDERING INFORMATION

5 MHz	5 MHz	5 MHz
40-Pin DIP	44-Pin PLCC	44-Pin QFP
Z86C1505PSC	Z86C1505VSC	Z86C1505FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES**Package**

P = Plastic DIP

V = Plastic Leaded Chip Carrier

F = Quad Flat Pack

Environmental

C = Plastic Standard

Temperature

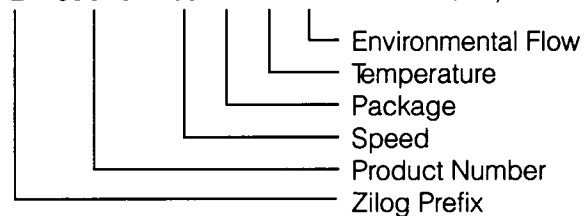
S = 0°C to +70°C

Speed

05 = 5 MHz

Example:

Z 86C15 05 P S C is a Z86C15, 5 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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