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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	125MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	150
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.064M x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5645sf1vlt

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS. The INTC provides the following features:

- Unique 9-bit vector for each of the possible 128 separate interrupt sources
- Eight software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources
- External non maskable interrupt directly accessing the main CPU critical interrupt mechanism
- 32 external interrupts

1.4.6 QuadSPI serial flash memory controller

The QuadSPI module enables use of external serial flash memories supporting single, dual, and quad modes of operation. It features the following:

- Maximum serial clock frequency 80 MHz
- Memory mapped read access for AHB crossbar switch masters
- Automatic serial flash read command generation by CPU, eDMA, DCU, or DCULite read access on AHB bus
- Supports single, dual, and quad serial flash read commands
- Simultaneous mode:
  - Supports concurrent read of two external serial flashes
  - The quad data streams from the two flashes can be recombined in the QuadSPI to achieve up to 80 MB/s read bandwidth with 80 MHz serial flash
- 16×64-bit buffer with speculative fetch and buffer flush mechanisms to maximize read bandwidth of serial flash
- DMA support
- All Serial Flash program, erase, read, and configuration commands available via IP bus interface

1.4.7 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.

The GPIO features the following:

- Up to four levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package
- Centralized general purpose input output (GPIO) control
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs
- Direct readback of the pin value supported on all digital output pins through the SIU
- Configurable digital input filter that can be applied to up to 24 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset

1.4.18 Video Input Unit (VIU2)

The VIU2 is a crossbar master module accepting an ITU656 compatible video input stream on a parallel interface, converting the pixel data to RGB or YUV format and transferring the video image to internal frame buffer memory or external DRAM if available.

- Supports 8-bit/10-bit ITU656 video input
- Output formats:
  - RGB888
  - RGB565
  - 8-bit monochrome
  - YCrCb 4:2:2
- Video downscaling
- Contrast and Brightness adjustment
- De-interlace for interlaced video image
- Internal DMA engine for data transfer to memory

1.4.19 Boot Assist Module (BAM)

The BAM is a block of read-only memory that is programmed once by Freescale. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via FlexCAN or LINFlex and then executed)
- Booting from external memory

Additionally the BAM:

- Enables and manages the transition of the MCU from reset to user code execution
- Configures device for serial bootload
- Enables multiple bootcode starting locations out of reset through implementation of search for valid Reset Configuration Halfword

1.4.20 Enhanced Modular Input/Output System (eMIOS)

This device has two eMIOS modules, each with 16 channels supporting a range of 16-bit Input Capture, Output Compare, Pulse Width Modulation, and Quadrature Decode functions.

- Selectable clock source from primary FMPLL, secondary FMPLL, external 4 - 16 MHz oscillator or 16 MHz Internal RC oscillator on a per module basis
- Timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges
- Edge aligned output pulse width modulation
  - Programmable pulse period and duty cycle
  - Supports 0% and 100% duty cycle
  - Shared or independent time bases
- Programmable phase shift between channels
- 4 channels of Quadrature Decode
- DMA transfer support

- Selectable clock sources from external 32 KHz crystal, external 4–16 MHz crystal, internal 128 kHz RC oscillator or divided internal 16 MHz RC oscillator

1.4.29 System Timer Module (STM)

The STM is a 32-bit timer designed to support commonly required system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel. The counter is driven by the system clock divided by an 8-bit prescale value (1 to 256).

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.4.30 Software Watchdog Timer (SWT)

The SWT features the following:

- Watchdog supporting software activation or enabled out of Reset
- Supports normal or windowed mode
- Watchdog timer value writable once after reset
- Watchdog supports optional halting during low power modes
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Clock source: 128 kHz RC oscillator

1.4.31 Stepper Motor Controller (SMC)

The SMC module is a PWM motor controller suitable to drive instruments in a cluster configuration or any other loads requiring a PWM signal. The motor controller has twelve PWM channels associated with two pins each (24 pins in total) driving up to 6 stepper motors.

The SMC module includes the following features:

- 10/11-bit PWM counter
- 11-bit resolution with selectable PWM dithering function
- Left, right, or center aligned PWM
- Output slew rate control
- Output Short Circuit Detection

This module is suited for, but not limited to, driving small stepper and air core motors used in instrumentation applications. This module can be used for other motor control or PWM applications that match the frequency, resolution, and output drive capabilities of the module.

1.4.32 Stepper Stall Detect (SSD)

The SSD module provides a circuit to measure and integrate the induced voltage on the non-driven coil of a stepper motor using full steps when the gauge pointer is returning to zero (RTZ).

The SSD module features the following:

- Programmable full step state
- Programmable integration polarity
- Blanking (recirculation) state
- 16-bit integration accumulator register

2.4 Signal description

The following sections provide signal descriptions and related information about the signals' functionality and configuration.

2.4.1 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are floating with the following exceptions:

- PB[5] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash memory.
- RESET pad is driven low. This is released only after PHASE2 reset completion.
- Fast (4-16 MHz) external oscillator pads (EXTAL, XTAL) are tristate.
- The following pads are pull-up:
  - PB[6]
  - PH[0]
  - PH[1]
  - PH[3]

NOTE

TCK pin must have an external pull-down resistor of 4.7 K.

2.4.2 Voltage supply pins

Voltage supply pins are used to provide power to the device. Two dedicated pins are used for 1.2 V regulator stabilization.

Table 4. System pin descriptions (continued)

System pin	Function	I/O direction	Pad type	RESET configuration[1]	Pin number		
					176 LQFP	208 LQFP	416 TEPBGA
NMI	Non-Maskable Interrupt	I/O	S	Input, none	45	53	AC7
VRC_CTRL	Voltage Regulator external NPN Ballast base control pin		Analog	—	29	29	AA3
VREF_RSDS[2]	RSDS interface reference voltage		Analog	—	—	145, 165	J24,D24
VREG_BYPASS[3]	Pin used for factory testing	I	—	—	26	26	AA2

1 Reset configuration is given as I/O direction and pull direction (for example, “Input, pullup”).

2 Although this signal is not a supply for RSDS pads, it needs to be terminated in an external capacitor with a value of 47 pF.

3 VREG_BYPASS should be connected to ground during normal operation.

2.4.4 Nexus pins

On the 176 LQFP and the 208 LQFP package options a reduced set of Nexus pins are optionally available, multiplexed with GPIO pins.

On the 416 TEPBGA package option all Nexus pins are dedicated to Nexus only.

Table 5. Nexus pins

System pin	Function	Pad type	PCR	Pin number[1]		
				176 LQFP	208 LQFP	416 TEPBGA
EVTI	Nexus Event In	M	PCR[80]	169	201	A17
EVTO	Nexus Event Out	M	PCR[70]	157	189	C20
MCKO	Nexus Msg Clock Out	F	PCR[85]	174	206	B18
MSEO[0]	Nexus Msg Start/End Out	M	PCR[71]	158	190	B20
MSEO[2]	Nexus Msg Start/End Out	M	PCR[73]	159	191	A20
MDO[0]	Nexus Msg Data Out	M	PCR[81]	170	202	D16
MDO[1]	Nexus Msg Data Out	M	PCR[82]	171	203	C16
MDO[2]	Nexus Msg Data Out	M	PCR[83]	172	204	B16
MDO[3]	Nexus Msg Data Out	M	PCR[84]	173	205	A16
EVTI	Nexus Event In	M	PCR[197]	n/a	n/a	AD8
EVTO	Nexus Event Out	M	PCR[198]	n/a	n/a	AE8
MCKO	Nexus Msg Clock Out	F	PCR[200]	n/a	n/a	AC17
MSEO[0]	Nexus Msg Start/End Out	M	PCR[199]	n/a	n/a	AD9
MSEO[2]	Nexus Msg Start/End Out	M	PCR[201]	n/a	n/a	AD17
MDO[0]	Nexus Msg Data Out	M	PCR[185]	n/a	n/a	AC20

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PC[4]	PCR[34]	Option 0 Option 1 Option 2 Option 3	GPIO[34] — — —	ANS[4]	SIUL — — —	I/O	J	None, none	84	100	AD24
PC[5]	PCR[35]	Option 0 Option 1 Option 2 Option 3	GPIO[35] — — —	ANS[5]	SIUL — — —	I/O	J	None, none	83	99	AD26
PC[6]	PCR[36]	Option 0 Option 1 Option 2 Option 3	GPIO[36] — — —	ANS[6]	SIUL — — —	I/O	J	None, none	82	98	AD21
PC[7]	PCR[37]	Option 0 Option 1 Option 2 Option 3	GPIO[37] — — —	ANS[7]	SIUL — — —	I/O	J	None, none	81	97	AD25
PC[8]	PCR[38]	Option 0 Option 1 Option 2 Option 3	GPIO[38] — — —	ANS[8]	SIUL — — —	I/O	J	None, none	76	92	AE26
PC[9]	PCR[39]	Option 0 Option 1 Option 2 Option 3	GPIO[39] — — —	ANS[9]	SIUL — — —	I/O	J	None, none	75	91	AE25
PC[10]	PCR[40]	Option 0 Option 1 Option 2 Option 3	GPIO[40] — I2S_DO/PWMO —	ANS[10]	SIUL — SGM —	I/O	J	None, none	74	90	AE23
PC[11]	PCR[41]	Option 0 Option 1 Option 2 Option 3	GPIO[41] — MA0 CS2_1	ANS[11]	SIUL — ADC DSPI_1	I/O	J	None, None	73	89	AE24
PC[12]	PCR[42]	Option 0 Option 1 Option 2 Option 3	GPIO[42] — MA1 CS1_1	ANS[12]	SIUL — ADC DSPI_1	I/O	J	None, None	72	88	AF26

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PC[13]	PCR[43]	Option 0 Option 1 Option 2 Option 3	GPIO[43] — MA2 CS0_1	ANS[13]	SIUL — ADC DSPI_1	I/O	J	None, None	71	87	AF25
PC[14]	PCR[44]	Option 0 Option 1 Option 2 Option 3	GPIO[44] — — —	ANS[14] EXTAL32	SIUL — — —	I/O	J	None, None	70	86	AF24
PC[15]	PCR[45]	Option 0 Option 1 Option 2 Option 3	GPIO[45] — — —	ANS[15] XTAL32	SIUL — — —	I/O	J	None, None	69	85	AF23
PORT D											
PD[0]	PCR[46]	Option 0 Option 1 Option 2 Option 3	GPIO[46] M0C0M SSD0_0 eMIOS1[8]	—	SIUL SMD SSD PWM/Timer	I/O	SMD	None, None	90	106	AB26
PD[1]	PCR[47]	Option 0 Option 1 Option 2 Option 3	GPIO[47] M0C0P SSD0_1 eMIOS1[16]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	91	107	AB25
PD[2]	PCR[48]	Option 0 Option 1 Option 2 Option 3	GPIO[48] M0C1M SSD0_2 eMIOS1[23]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	92	108	AB24
PD[3]	PCR[49]	Option 0 Option 1 Option 2 Option 3	GPIO[49] M0C1P SSD0_3 eMIOS0[9]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	93	109	AB23
PD[4]	PCR[50]	Option 0 Option 1 Option 2 Option 3	GPIO[50] M1C0M SSD1_0 eMIOS0[8]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	96	112	AA26
PD[5]	PCR[51]	Option 0 Option 1 Option 2 Option 3	GPIO[51] M1C0P SSD1_1 eMIOS0[16]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	97	113	AA23

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PF[9]	PCR[79]	Option 0 Option 1 Option 2 Option 3	GPIO[79] SCL_0 CS1_1 TXD_1	—	SIUL I^{2}C_0 DSPI_1 LINFlex_1	I/O	S	None, None	165	197	D17
PF[10]	PCR[80]	Option 0 Option 1 Option 2 Option 3	GPIO[80] QUADSPI_PCS_A — EVTI	—	SIUL QuadSPI — NEXUS	I/O	M	None, None	169	201	A17
PF[11]	PCR[81]	Option 0 Option 1 Option 2 Option 3	GPIO[81] QUADSPI_IO2_A — MDO0	—	SIUL QuadSPI — NEXUS	I/O	M	None, None	170	202	D16
PF[12]	PCR[82]	Option 0 Option 1 Option 2 Option 3	GPIO[82] QUADSPI_IO3_A — MDO1	—	SIUL QuadSPI — NEXUS	I/O	M	None, None	171	203	C16
PF[13]	PCR[83]	Option 0 Option 1 Option 2 Option 3	GPIO[83] QUADSPI_IO0_A — MDO2	—	SIUL QuadSPI — NEXUS	I/O	M	None, None	172	204	B16
PF[14]	PCR[84]	Option 0 Option 1 Option 2 Option 3	GPIO[84] QUADSPI_IO1_A — MDO3	—	SIUL QuadSPI — NEXUS	I/O	M	None, None	173	205	A16
PF[15]	PCR[85]	Option 0 Option 1 Option 2 Option 3	GPIO[85] QUADSPI_CLK_A CLKOUT MCKO	—	SIUL QuadSPI Control NEXUS	I/O	F	None, None	174	206	B18
PORT G											
PG[0]	PCR[86]	Option 0 Option 1 Option 2 Option 3	GPIO[86] DCU_B0 SCL_3 eMIOS0[21]	RSDS8P	SIUL DCU3 I^{2}C_3 PWM/Timer	I/O	M	None, None	136	160	E26
PG[1]	PCR[87]	Option 0 Option 1 Option 2 Option 3	GPIO[87] DCU_B1 SDA_3 eMIOS0[22]	RSDS8M	SIUL DCU3 I^{2}C_3 PWM/Timer	I/O	M	None, None	137	161	D26

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PK[7]	PCR[128]	Option 0 Option 1 Option 2 Option 3	GPIO[128] RXD_2 DCULITE_R2 TCON[8]	—	SIUL LINFlex_2 DCULite TCON	I/O	M	None, None	—	44	AD5
PK[8]	PCR[129]	Option 0 Option 1 Option 2 Option 3	GPIO[129] TXD_2 DCULITE_R3 TCON[9]	—	SIUL LINFlex_2 DCULite TCON	I/O	M	None, None	—	45	AE5
PK[9]	PCR[130]	Option 0 Option 1 Option 2 Option 3	GPIO[130] I2S_DO / PWMO DCULITE_R4 TCON[10]	—	SIUL SGM DCULite TCON	I/O	M	None, None	—	46	AF5
PK[10]	PCR[131]	Option 0 Option 1 Option 2 Option 3	GPIO[131] SDA_1 eMIOS1[12] DCULITE_TAG	—	SIUL I^2C_1 PWM/Timer DCULite	I/O	S	None, None	51	59	AF8
PK[11]	PCR[132]	Option 0 Option 1 Option 2 Option 3	GPIO[132] SCL_1 eMIOS1[13] DCU_TAG	—	SIUL I^2C_1 PWM/Timer DCU3	I/O	S	None, None	52	60	AC9
PK[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PORT L											
PL[0]	PCR[133]	Option 0 Option 1 Option 2 Option 3	GPIO[133] — CANRX_1 SDA_1	ANS[19]	SIUL — FlexCAN_1 I2C1	I/O	M / ANALOG	None, None	—	81	AE22
PL[1]	PCR[134]	Option 0 Option 1 Option 2 Option 3	GPIO[134] — CANTX_1 SCL_1	ANS[18]	SIUL — FlexCAN_1 I2C1	I/O	M / ANALOG	None, None	—	82	AE21

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PL[2]	PCR[135]	Option 0 Option 1 Option 2 Option 3	GPIO[135] — CANRX_0 eMIOS1[22]	ANS[17]	SIUL — FlexCAN_0 PWM/Timer	I/O	S / ANALOG	None, None	—	83	AF22
PL[3]	PCR[136]	Option 0 Option 1 Option 2 Option 3	GPIO[136] — CANTX_0 eMIOS1[23]	ANS[16]	SIUL — FlexCAN_0 PWM/Timer	I/O	S / ANALOG	None, None	—	84	AF21
PL[4]	PCR[137]	Option 0 Option 1 Option 2 Option 3	GPIO[137] CS2_2 VIU5_PDI13 TCON[6]	—	SIUL DSPI_2 VIU2/PDI TCON	I/O	M	None, None	—	31	AB2
PL[5]	PCR[138]	Option 0 Option 1 Option 2 Option 3	GPIO[138] CS1_2 VIU6_PDI14 TCON[7]	—	SIUL DSPI_2 VIU2/PDI TCON	I/O	M	None, None	—	32	AC2
PL[6]	PCR[139]	Option 0 Option 1 Option 2 Option 3	GPIO[139] CS0_2 VIU7_PDI15 eMIOS1[18]	—	SIUL DSPI_2 VIU2/PDI PWM/Timer	I/O	S	None, None	—	33	AD1
PL[7]	PCR[140]	Option 0 Option 1 Option 2 Option 3	GPIO[140] SIN_2 VIU8_PDI16 eMIOS1[19]	—	SIUL DSPI_2 VIU2/PDI PWM/Timer	I/O	S	None, None	—	34	AE1
PL[8]	PCR[141]	Option 0 Option 1 Option 2 Option 3	GPIO[141] SOUT_2 VIU9_PDI17 eMIOS1[20]	—	SIUL DSPI_2 VIU2/PDI PWM/Timer	I/O	S	None, None	—	35	AF1
PL[9]	PCR[142]	Option 0 Option 1 Option 2 Option 3	GPIO[142] SCK_2 PDI_PCLK eMIOS1[21]	—	SIUL DSPI_2 PDI PWM/Timer	I/O	S	None, None	—	36	AF2
PL[10]	PCR[143]	Option 0 Option 1 Option 2 Option 3	GPIO[143] eMIOS1[10] DCULITE_G2 —	—	SIUL PWM/Timer DCULite —	I/O	M	None, None	—	174	C24

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PM[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PORT N											
PN[0]	PCR[161]	Option 0 Option 1 Option 2 Option 3	GPIO[161] DCULITE_HSYNC — TCON[4]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AC3
PN[1]	PCR[162]	Option 0 Option 1 Option 2 Option 3	GPIO[162] DCULITE_VSYNC — TCON[5]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AD3
PN[2]	PCR[163]	Option 0 Option 1 Option 2 Option 3	GPIO[163] DCULITE_R0 RXD_2 VIU0_PDI8	—	SIUL DCULite LINFlex_2 VIU2/PDI	I/O	M	None, None	—	—	AC10
PN[3]	PCR[164]	Option 0 Option 1 Option 2 Option 3	GPIO[164] DCULITE_R1 TXD_2 VIU1_PDI9	—	SIUL DCULite LINFlex_2 VIU2/PDI	I/O	M	None, None	—	—	AF10
PN[4]	PCR[165]	Option 0 Option 1 Option 2 Option 3	GPIO[165] DCULITE_R2 — TCON[6]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AC11
PN[5]	PCR[166]	Option 0 Option 1 Option 2 Option 3	GPIO[166] DCULITE_R3 — TCON[7]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AD11
PN[6]	PCR[167]	Option 0 Option 1 Option 2 Option 3	GPIO[167] DCULITE_R4 — TCON[8]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AE11
PN[7]	PCR[168]	Option 0 Option 1 Option 2 Option 3	GPIO[168] DCULITE_R5 — TCON[9]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AF11

The following pad types are available for system pins and functional port pins:

Table 9. Pad Types

Pad	Function
S	Slow (pad_ssr, pad_ssr_hv)
M	Medium (pad_msr, pad_msr_hv)
F	Fast (pad_fc)
J	Input/output with analog features (pad_tgate, pad_tgate_hv)
Analog	Input only with analog features (pad_ae, pad_ae_hv)
SMD	Stepper Motor Detector
DDR	DDR pads
RSDS	RSDS pads

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D) \qquad \textit{Eqn. 2}$$

where:

T_B= board temperature for the package perimeter (^oC)

$R_{\theta JB}$= junction-to-board thermal resistance ($^oC/W$) per JESD51-8S

P_D= power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$= junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$= case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ s device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

[6] Flash in Low Power. RC-osc128KHz & RC-OSC 16MHzon. 10MHz XTAL clock.FlexCAN: instances: 0, 1ON (clocked but no reception or transmission), LINFLEX: instances 0, 1, 2 ON (clocked but no reception or transmission). eMIOS: instance: 0, 1 ON - 16 channels on with PWM20KHz. DSPI: instance: 0 (clocked but no communication). DCUs, TCON, VIU, GPU clock gated, RTC/API ON.PIT ON. STM ON. ADC ON but not converting.

[7] For Tj > 105 ^{0}C , HPvreg needs to be kept ON. The consumption increases beyond this temperature and to handle the extra current, HPvreg should be ON.

[8] No clock, RC 16MHz off, RCI 128KHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

[9] ULPreg ON, HP/LPVreg off, 64KB RAM on, device configured for minimum consumption, all possible modules switched-off.

[10] ULPreg ON, HP/LPVreg off, 8KB RAM on, device configured for minimum consumption, all possible modules switched-off.

4.8 DC electrical specifications

4.8.1 DC specification for CMOS090LP2 library @ VDDE = 3.3 V

NOTE

These pad specifications are applicable for pads in the Digital segment Only. See the "GPIO power bank supplies and functionality" table in the "Voltage Regulators and Power Supplies" chapter of the reference manual for details.

Table 23. DC electrical specifications

Symbol		C	Parameter	Condition	Value		Unit	SpecID
					Min	Max		
Vdd	SR	P	Core supply voltage	—	1.08	1.32	V	D9.1
Vdde	SR	P	I/O supply voltage	—	3.0	3.6	V	D9.2
Vdd33	SR	P	I/O pre-driver supply voltage	—	3.0	3.6	V	D9.3
Vih_c	SR	P	CMOS input buffer high voltage	With hysteresis enabled	0.65×Vdde	Vdde+0.3	V	D9.4
				With hysteresis disabled	0.55×Vdde	Vdde+0.3		
Vil_c	SR	P	CMOS input buffer low voltage	With hysteresis enabled	Vss–0.3	0.35×Vdde	V	D9.5
				With hysteresis disabled	Vss–0.3	0.40×Vdde		
Vhys_c	SR	T	CMOS input buffer hysteresis	—	0.1×Vdde	—	V	D9.6
Vih_fod_h	SR	P	5 V tolerant CMOS input buffer high voltage	With hysteresis enabled	0.65×Vdd33	Vdd33+0.3	V	D9.7
Vil_fod_h	SR	P	5 V tolerant CMOS input buffer low voltage	With hysteresis enabled	Vss–0.3	0.35×Vdd33	V	D9.8
Iact_s	SR	T	Selectable weak pullup/pulldown current	—	25	150	µA	D9.9
Iinact_d	SR	P	Digital pad input leakage current	Weak pull inactive	–2.5	2.5	µA	D9.10

Table 28. Supply leakage

Pad	VDD		VDDE		VDD33	
	Typ	Max	Typ	Max	Typ	Max
pad_msr_hv	0.818 nA	83.7 nA	0.81 nA	118 nA	—	—
pad ssr_hv	0.818 nA	83.7 nA	0.858 nA	88.7 nA	—	—
pad_i_hv	0.307 nA	48.4 nA	88.2 pA	30 nA	—	—
biasref_hv	—	—	—	—	—	—
core_v_det_hv	0	0	—	—	0	0
core_v_det_lp_hv	0	0	—	—	—	—
corner_esdpadcell_hv	—	—	—	—	—	—
corner_esdpadcell_id00_hv	—	—	—	—	—	—
corner_esdpadcell_id11_hv	—	—	—	—	—	—
corner_esdpadcell_lp_hv	—	—	—	—	—	—
esd_term_35_84_hv	—	—	—	—	—	—
pad_9v_hv	0	0	—	—	—	—
pad_ae_hv	—	—	—	—	—	—
pad_esdspacer_hv	—	—	—	—	—	—
pad_tgate_hv	—	—	—	—	—	—
pad_vdd33_hv	—	—	—	—	—	—
pad_vdde_hv	0	0	—	—	0	0
pad_vddint3v_hv	0	0	—	—	0	0
pad_vddint_hv	0	0	—	—	—	—
pad_vss_hv	0	0	—	—	—	—
pad_vsse_hv	0	0	—	—	—	—
pad_vssint3v_hv	0	0	—	—	—	—
pad_vssint_hv	0	0	—	—	—	—
spcr_17_82_hv	—	—	—	—	—	—
spcr_35_84_hv	—	—	—	—	—	—
spcr_71_88_hv	—	—	—	—	—	—
spcr_143_38_hv	—	—	—	—	—	—
spcr_vdde_lvl_hv	—	—	—	—	—	—

4.18.6 AC specification for CMOS090_ddr library @ VDDE = 1.8 V

Table 55. AC electrical specifications at 1.8 V VDD

Name	C	Prop. delay (ns) L>H / H>L		Rise/fall edge (ns)		Drive load (pF)	Drive/slew rate select	Libraries
		Min	Max	Min	Max		MSB, LSB	
pad_st_acc	C	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000	6MDDR
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20		
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001	
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20		
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010	
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20		
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110	
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20		
pad_st_dq	C	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000	6MDDR
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20		
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001	
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20		
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010	
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20		
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110	
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20		
pad_st_clk	C	1.4/1.4	2.4/2.4	0.4/0.6	2.7/2.7	5	000	6MDDR
		1.6/1.6	2.7/2.7	0.7/0.9	1.8/3.4	20		
		1.4/1.4	2.4/2.4	1.1/1.1	3.0/2.8	5	001	
		1.7/1.7	2.7/2.7	0.3/0.4	1.0/1.1	20		
		1.4/1.4	2.4/2.4	0.9/1.1	3.0/2.8	5	010	
		1.6/1.6	2.7/2.7	0.3/0.4	0.9/1.0	20		
		1.4/1.5	2.5/2.5	1.5/1.2	3.2/2.6	5	110	
		1.7/1.8	2.7/2.7	0.4/0.4	1.1/1.2	20		

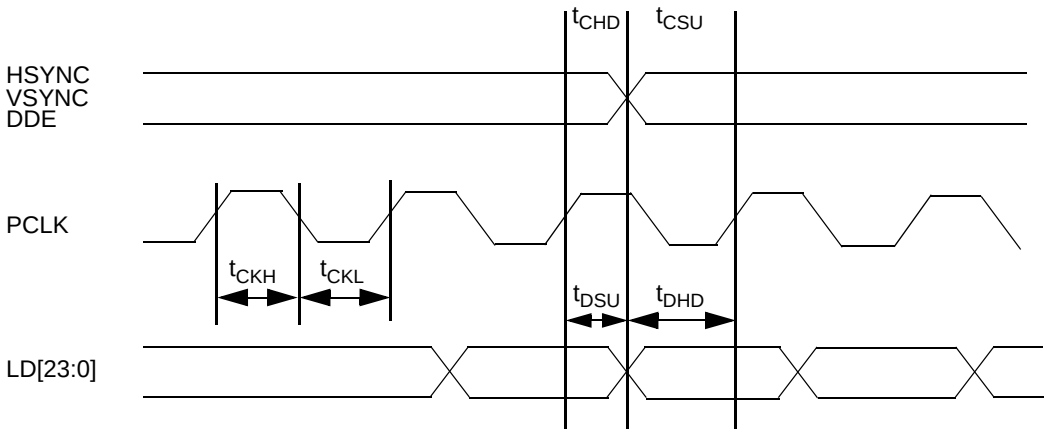


Figure 26. LCD Interface Timing Parameters—Access Level

4.19.11 I²C timing

Table 72. I²C Input Timing Specifications—SCL and SDA

Num	Symbol		C	Characteristic	Min. Value	Max. Value	Unit	SpecID
1	—	CC[1]	D	Start condition hold time	2	—	IP-Bus Cycle[2]	A12.1
2	—	CC[1]	D	Clock low time	8	—	IP-Bus Cycle[2]	A12.2
4	—	CC[1]	D	Data hold time	0.0	—	ns	A12.3
6	—	CC[1]	D	Clock high time	4	—	IP-Bus Cycle[2]	A12.4
7	—	CC[1]	D	Data setup time	0.0	—	ns	A12.5
8	—	CC[1]	D	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[2]	A12.6
9	—	CC[1]	D	Stop condition setup time	2	—	IP-Bus Cycle[2]	A12.7

1 Parameter values guaranteed by design.

2 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

Table 73. I²C Output Timing Specifications—SCL and SDA

Num	Symbol		C	Characteristic	Min. Value	Max. Value	Unit	SpecID
1[1]	—	CC[2]	D	Start condition hold time	6	—	IP-Bus Cycle[3]	A12.8
2[1]	—	CC[2]	D	Clock low time	10	—	IP-Bus Cycle[2]	A12.9
3[4]	—	CC[2]	D	SCL/SDA rise time	—	99.6	ns	A12.10
4[1]	—	CC[2]	D	Data hold time	7	—	IP-Bus Cycle[2]	A12.11
5[1]	—	CC[2]	D	SCL/SDA fall time	—	99.5	ns	A12.12
6[1]	—	CC[2]	D	Clock high time	10	—	IP-Bus Cycle[2]	A12.13
7[1]	—	CC[2]	D	Data setup time	2	—	IP-Bus Cycle[2]	A12.14
8[1]	—	CC[2]	D	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[2]	A12.15
9[1]	—	CC[2]	D	Stop condition setup time	10	—	IP-Bus Cycle[2]	A12.16

1 Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Parameter values guaranteed by design.

3 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

4 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

Table 75. QuadSPI timing events

Number	Event
1	Last address out
2	Address captured at flash memory
3	Data out from flash memory
4	Ideal data capture edge
5	Delayed data capture edge with QSPI_SMPR=0x0000_000X
6	Delayed data capture edge with QSPI_SMPR=0x0000_002X
7	Delayed data capture edge with QSPI_SMPR=0x0000_004X
8	Delayed data capture edge with QSPI_SMPR=0x0000_006X

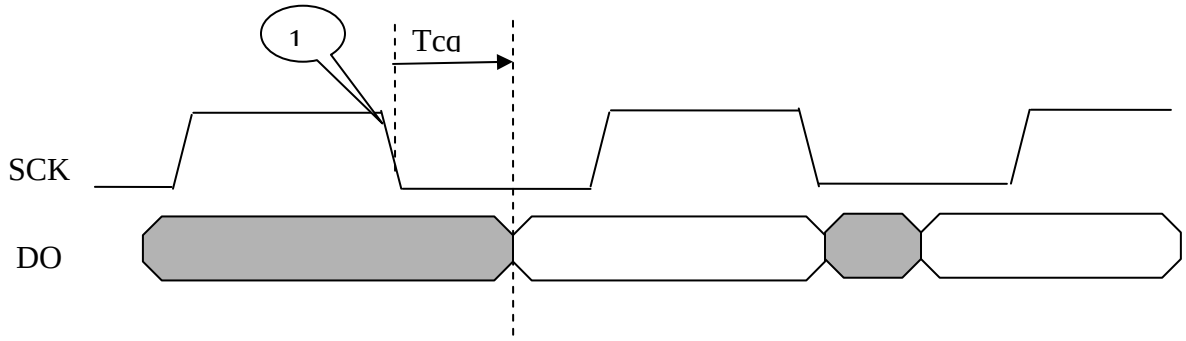
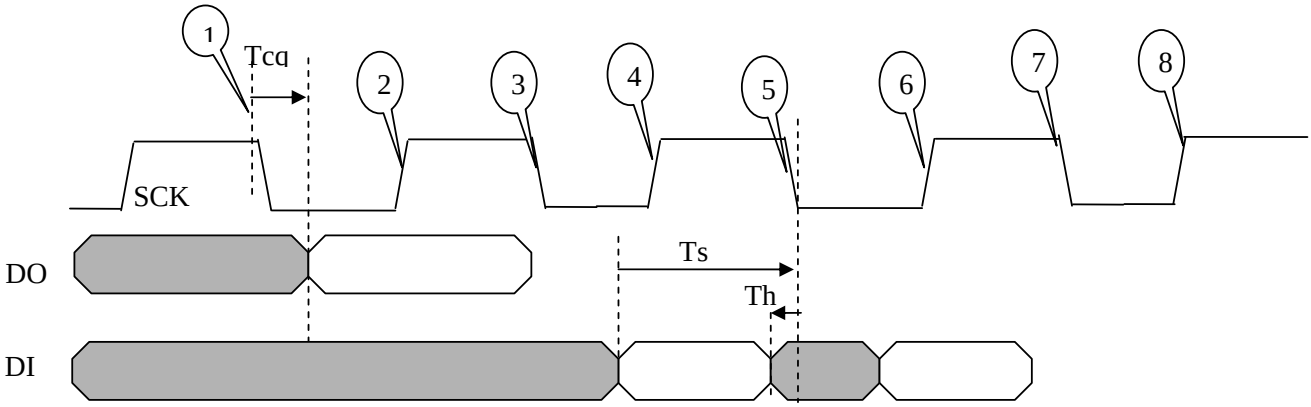
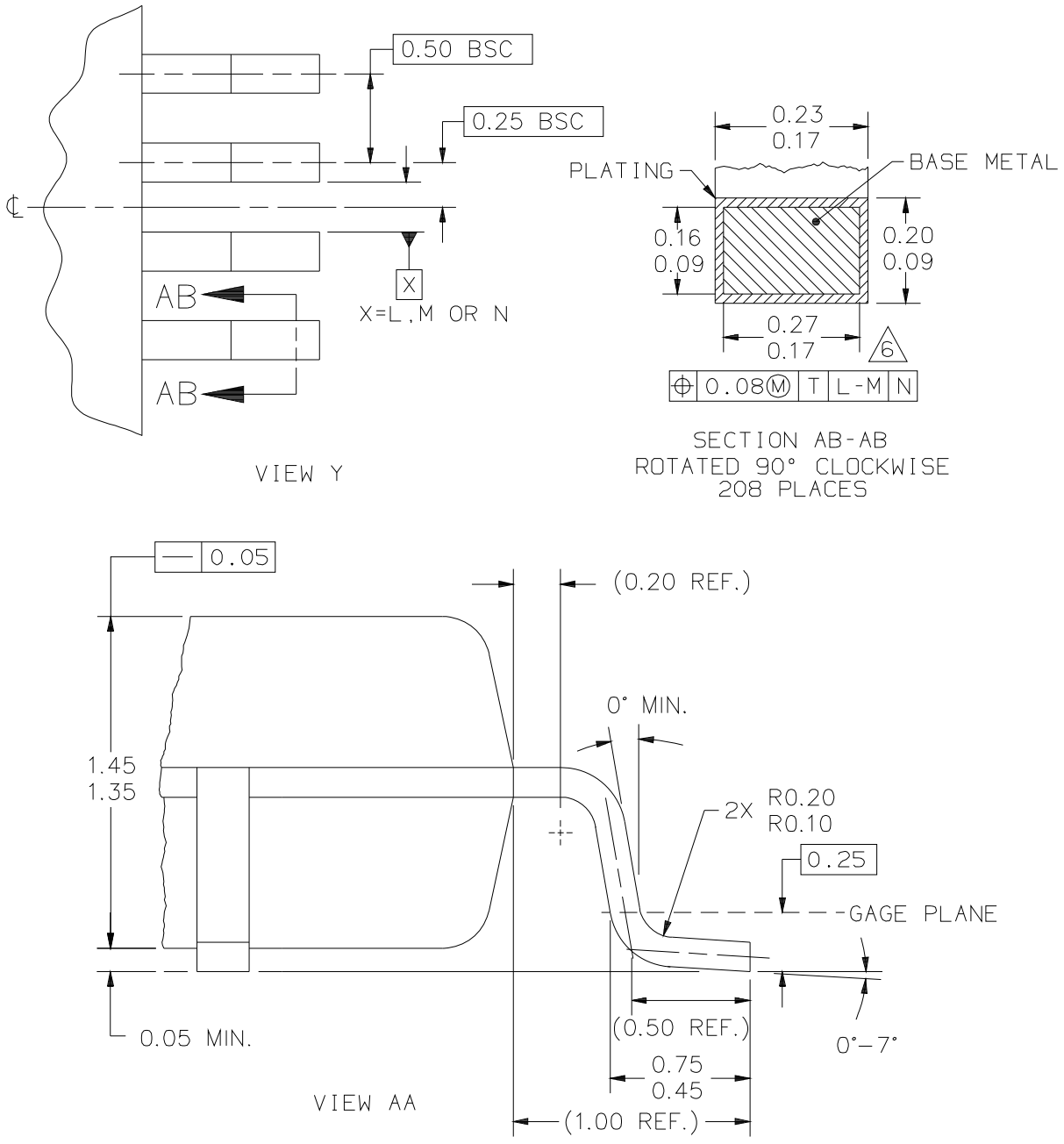


Figure 45. QuadSPI output timing



Note: Ts and Th correspond to QSPI_SMPR = 0x0000_000X.

Figure 46. QuadSPI input timing



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	CASE NUMBER: 998-01	20 MAY 2005
	STANDARD: JEDEC MS-026 BJB	

Figure 55. LQFP208 Mechanical Drawing (Part 2 of 3)