Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	125MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	128
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.064M x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5645sf1vlu

— Low-Power and Ultra-Low-Power regulators support operation when in STOP and STANDBY modes, respectively, to minimize power consumption
— Startup on-chip regulators in <350µs for rapid exit of STOP and STANDBY modes
— Low voltage detection on main supply and 1.2 V regulated supplies

1.4.2 e200z4d core

The e200z4d Power Architecture® core provides the following features:

- Dual issue, 32-bit *Power Architecture Book E* compliant CPU
- Implements the VLE APU for reduced code footprint
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  — Dedicated branch address calculation adder
  — Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and Flash memory via independent Instruction and Data BIUs.
- Load/store unit
  — 2 cycle load latency
  — Fully pipelined
  — Big and Little endian support
  — Misaligned access support
- 64-bit General Purpose Register file
- Dual AHB 2.v6 64-bit System buses
- Memory Management Unit (MMU) with 16-entry fully-associative TLB and multiple page size support
- 4 KB, 2/4-Way Set Associative Instruction Cache
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Nexus Class 3 real-time Development Unit
- Dynamic power management of execution units, cache and MMU

1.4.3 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between seven master ports and eight slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows concurrent transactions to occur from any master port to any slave port but one of those transfers must be an instruction fetch from internal flash. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters having equal priority are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- Seven master ports:
  — e200z4d core instruction port
  — e200z4d core complex load/store data port

The source system clock frequency can be changed via an on-chip programmable clock divider (÷1 to ÷32). An additional programmable peripheral bus clock divider (ratios ÷1 to ÷15) is also available.

The MPC5645S has two on-chip FMPLLs (primary and secondary). Each features the following:

- Input clock frequency from 4 MHz to 16 MHz
- Lock detect circuitry continuously monitors lock status
- Loss Of Clock (LOC) detection for reference and feedback clocks
- On-chip loop filter (for improved electromagnetic interference performance and reduction of number of external components required)
- Support for frequency ramping from PLL

The primary FMPLL module is for use as a system clock source. The secondary FMPLL is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules and as alternate clock to the DCU for pixel clock generation.

The fast external oscillator provides the following features:

- Input frequency range 4–16 MHz
- Square-wave input mode
- Oscillator input mode 3.3 V (5.0 V)
- Automatic level control
- Low power consumption
- PLL reference

The MPC5645S also includes the following oscillators:

- 32 KHz low power external oscillator for slow execution, low power, and RTC
- Dedicated internal 128 kHz RC oscillator for low power mode operation and self wake-up
  - ±10% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support improved accuracy with in-application calibration
- Dedicated 16 MHz internal RC oscillator
  - Used as default clock source out of reset
  - Provides a clock for rapid start-up from low power modes
  - Provides a back-up clock in the event of PLL or External Oscillator clock failure
  - Offers an independent clock source for the SWT
  - ±5% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support frequency adjustment with in-application calibration

1.4.27 Periodic Interrupt Timer (PIT)

The PIT features the following:

- Eight general purpose interrupt timers
- Two dedicated interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency

1.4.28 Real Time Counter (RTC)

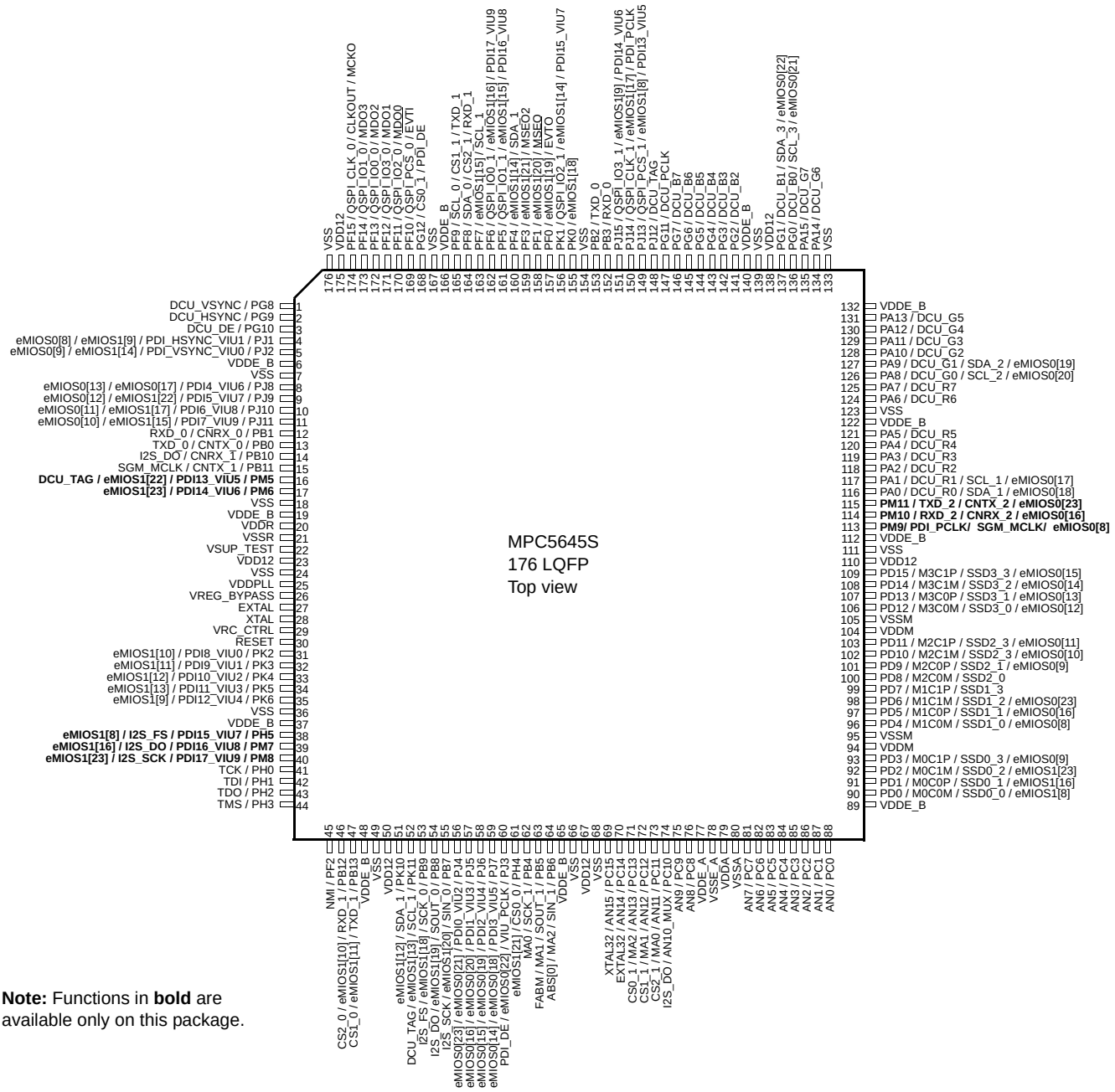
The Real Timer Counter supports wake-up from Low Power modes or Real Time Clock generation

- Configurable resolution for different timeout periods
  - 1 s resolution for >1 hour period
  - 1 ms resolution for 2 second period

2 Pinout and signal descriptions

2.1 176 LQFP package pinout

Figure 2 shows the pinout for the 176-pin LQFP package.



Note: Functions in **bold** are available only on this package.

Figure 2. 176-pin LQFP pinout

2.3 416 TEPBGA package pinout

Figure 4 shows the pinout for the 416 TEPBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	ddr_dq[26]	ddr_dq[27]	ddr_dq[28]	ddr_dq[29]	30]	31]	ddr_ba[0]	ddr_ba[1]	ddr_ba[2]	ddr_address[0]	ddr_address[4]	ddr_address[6]	ddr_address[8]	ddr_address[12]	PG12	PF14	PF10	PF8	PF5	PF3	PK0	PB3	PJ12	PL11	PG7	PG6	A
B	ddr_dq[25]	VSS	ddr_dqs[3]	ddr_dm[3]	VSS	ddr_cas	ddr_ras	VSS	ddr_web	ddr_address[1]	VSS	ddr_address[7]	ddr_address[9]	VSS	ddr_address[15]	PF13	VDDE	PF15	VSS	PF1	VDDE	PJ15	PL13	VDDE	VSS	PG5	B
C	ddr_dq[23]]	VDDE_DDR	VSS	ddr_dq[24]	VDDE_DDR	VSS	ddr_dram_clk	VDDE_DDR	VSS	ddr_address[2]	VDDE_DDR	VSS	ddr_address[10]	VDDE_DDR	VSS	PF12	VSS	PF7	VDDE	PF0	VSS	PJ14	PL12	PL10	PG3	PG4	C
D	ddr_dq[19]	ddr_dq[20]	ddr_dq[21]	ddr_dq[22]	ddr_odt	VDD33_DDR	ddr_dram_clkb	ddr_cke	ddr_cs	ddr_address[3]	ddr_address[5]	VDD33_DDR	ddr_address[11]	ddr_address[13]	ddr_address[14]	PF11	PF9	PF6	PF4	PK1	PB2	PJ13	PM2	**VREF_RSDS2**	PG2	PG1	D
E	ddr_dq[17]	VSS	VDDE_DDR	ddr_dq[18]																			PG11	VSS	VDDE	PG0	E
F	ddr_dq[16]	**MVTT3**	VSS	VDD33_DDR																			PA15	PA14	PA13	PA12	F
G	ddr_dq[15]	ddr_dqs[2]	ddr_dm[2]	ddr_dq[14]																			PA11	PA9	PA8	PA7	G
H	ddr_dq[13]	VSS	VDDE_DDR	ddr_dq[12]																			PA10	VDDE	VSS	VA6	H
J	ddr_dq[11]	**MVTT2**	VSS	MVREF																			PA3	**VREF_RSDS1**	PA5	PA4	J
K	ddr_dq[9]	ddr_dqs[1]	ddr_dm[1]	ddr_dq[10]						VDD12	VSS	VDD12	VSS	VDD12	VSS	VDD12	VSS						PA2	VSS	PA1	PA0	K
L	ddr_dq[8]	VSS	VDDE_DDR	ddr_dq[7]						VSS	VDD12	VSS	VDD12	VSS	VDD12	VSS	VDD12						PM13	PM12	VDDE	PJ0	L
M	ddr_dq[5]	**MVTT1**	VSS	ddr_dq[6]						VDD12	VSS	VSS	VSS	VSS	VSS	VDD12	VSS						PO7	PO6	PO5	PO4	M
N	ddr_dq[3]	ddr_dqs[0]	VDDE_DDR	ddr_dq[4]						VSS	VDD12	VSS	VSS	VSS	VSS	VSS	VDD12						PO3	VDDE	PO2	PO1	N
P	ddr_dq[1]	VSS	ddr_dm[0]	ddr_dq[2]						VDD12	VSS	VSS	VSS	VSS	VSS	VDD12	VSS						PO0	PN15	VSS	PN14	P
R	ddr_dq[0]	**MVTT0**	VSS	VDD33_DDR						VSS	VDD12	VSS	VSS	VSS	VSS	VSS	VDD12						PE7	PE6	PN13	PN12	R
T	PG10	PG9	VDDE_DDR	PG8						VDD12	VSS	VDD12	VSS	VDD12	VSS	VDD12	VSS						PE5	PE4	PE3	PE2	T
U	PJ9	PJ8	PJ2	PJ1						VSS	VDD12	VSS	VDD12	VSS	VDD12	VSS	VDD12						PE1	VSSM	VDDM	PE0	U
V	PB1	VSS	PJ11	PJ10																			PD15	PD14	PD13	PD12	V
W	**RESET**	PB10	VDDE	PB0																			PD11	VDDM	VSSM	PD10	W
Y	VSS	PM4	PM3	PB11																			PD9	PD8	PD7	PD6	Y
AA	**XTAL**	**VREG_BYPASS**	**VRC_CTRL**	**VDDREG**																			PD5	VSSM	VDDM	PD4	AA
AB	**EXTAL**	PL4	VSS	**VDDPLL**																			PD3	PD2	PD1	PD0	AB
AC	**VSUP_TEST**	PL5	**PN0**	**PK4**	**PK6**	**PH0**	PF2	PB13	PK11	PN2	PN4	PN8	PB9	PB7	PJ7	PB5	MCKO	MDO6	MDO10	MVO0	PC0	VDDA	VSSEH_ADC	PC3	PC1	PC2	AC
AD	**PL6**	VDDE	**PN1**	VSS	**PK7**	PH1	VDDE	EVTI	MSEO	VSS	PN5	PN9	VDDE	PJ4	PJ3	VSS	MSEO2	MDO7	VDDE	MDO1	PC6	VSSA	VDDEH_ADC	PC4	PC7	PC5	AD
AE	**PL7**	VSS	**PK2**	VDDE	**PK8**	PH2	VSS	EVTO	PM0	VDDE	PN6	PN10	VSS	PJ5	PH4	VDDE	MDO4	MDO8	VSS	MDO2	PL1	PL0	PC10	PC11	PC9	PC8	AE
AF	**PL8**	**PL9**	**PK3**	**PK5**	**PK9**	**PH3**	PB12	PK10	PM1	PN3	PN7	PN11	PB8	PJ6	PB4	PB6	MDO5	MDO9	MDO11	MDO3	PL3	PL2	**PC15**	**PC14**	PC13	PC12	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

416 TEPBGA pinout

Figure 4. 416 TEPBGA package pinout

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PB[1]	PCR[17]	Option 0 Option 1 Option 2 Option 3	GPIO[17] CANRX_0 RXD_0 —	—	SIUL FlexCAN_0 LINFlex_0 —	I/O	S	None, none	12	12	V1
PB[2]	PCR[18]	Option 0 Option 1 Option 2 Option 3	GPIO[18] TXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, none	153	183	D21
PB[3]	PCR[19]	Option 0 Option 1 Option 2 Option 3	GPIO[19] RXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, none	152	182	A22
PB[4]	PCR[20]	Option 0 Option 1 Option 2 Option 3	GPIO[20] SCK_1 MA0 —	—	SIUL DSPI_1 ADC —	I/O	S	None, none	62	74	AF15
PB[5]	PCR[21]	Option 0 Option 1 Option 2 Option 3	GPIO[21] SOUT_1 MA1 FABM	—	SIUL DSPI_1 ADC Control	I/O	S	Input, pull-down	63	75	AC16
PB[6]	PCR[22]	Option 0 Option 1 Option 2 Option 3	GPIO[22] SIN_1 MA2 ABS[0]	—	SIUL DSPI_1 ADC Control	I/O	S	Input, pull-up	64	76	AF16
PB[7]	PCR[23]	Option 0 Option 1 Option 2 Option 3	GPIO[23] SIN_0 eMIOS1[20] I2S_SCK/PWMO	—	SIUL DSPI_0 PWM/Timer SGM	I/O	S	None, none	55	67	AC14
PB[8]	PCR[24]	Option 0 Option 1 Option 2 Option 3	GPIO[24] SOUT_0 eMIOS1[19] I2S_DO/PWMOA	—	SIUL DSPI_0 PWM/Timer SGM	I/O	S	None, none	54	66	AF13
PB[9]	PCR[25]	Option 0 Option 1 Option 2 Option 3	GPIO[25] SCK_0 eMIOS1[18] I2S_FS	—	SIUL DSPI_0 PWM/Timer SGM	I/O	M	None, none	53	65	AC13

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PB[10]	PCR[26]	Option 0 Option 1 Option 2 Option 3	GPIO[26] CANRX_1 I2S_DO/PWMOA —	—	SIUL FlexCAN_1 SGM —	I/O	S	None, none	14	14	W2
PB[11]	PCR[27]	Option 0 Option 1 Option 2 Option 3	GPIO[27] CANTX_1 SGM_MCLK —	—	SIUL FlexCAN_1 SGM —	I/O	S	None, none	15	15	Y4
PB[12]	PCR[28]	Option 0 Option 1 Option 2 Option 3	GPIO[28] RXD_1 eMIOS1[10] CS2_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, none	46	54	AF7
PB[13]	PCR[29]	Option 0 Option 1 Option 2 Option 3	GPIO[29] TXD_1 eMIOS1[11] CS1_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, none	47	55	AC8
PB[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PB[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PORT C											
PC[0]	PCR[30]	Option 0 Option 1 Option 2 Option 3	GPIO[30] — — —	ANS[0]	SIUL — — —	I/O	J	None, none	88	104	AC21
PC[1]	PCR[31]	Option 0 Option 1 Option 2 Option 3	GPIO[31] — — —	ANS[1]	SIUL — — —	I/O	J	None, none	87	103	AC25
PC[2]	PCR[32]	Option 0 Option 1 Option 2 Option 3	GPIO[32] — — —	ANS[2]	SIUL — — —	I/O	J	None, none	86	102	AC26
PC[3]	PCR[33]	Option 0 Option 1 Option 2 Option 3	GPIO[33] — — —	ANS[3]	SIUL — — —	I/O	J	None, none	85	101	AC24

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PD[6]	PCR[52]	Option 0 Option 1 Option 2 Option 3	GPIO[52] M1C1M SSD1_2 eMIOS0[23]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	98	114	Y26
PD[7]	PCR[53]	Option 0 Option 1 Option 2 Option 3	GPIO[53] M1C1P SSD1_3 —	—	SIUL SMC SSD —	I/O	SMD	None, None	99	115	Y25
PD[8]	PCR[54]	Option 0 Option 1 Option 2 Option 3	GPIO[54] M2C0M SSD2_0 —	—	SIUL SMC SSD —	I/O	SMD	None, None	100	116	Y24
PD[9]	PCR[55]	Option 0 Option 1 Option 2 Option 3	GPIO[55] M2C0P SSD2_1 eMIOS0[9]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	101	117	Y23
PD[10]	PCR[56]	Option 0 Option 1 Option 2 Option 3	GPIO[56] M2C1M SSD2_2 eMIOS0[10]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	102	118	W26
PD[11]	PCR[57]	Option 0 Option 1 Option 2 Option 3	GPIO[57] M2C1P SSD2_3 eMIOS0[11]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	103	119	W23
PD[12]	PCR[58]	Option 0 Option 1 Option 2 Option 3	GPIO[58] M3C0M SSD3_0 eMIOS0[12]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	106	122	V26
PD[13]	PCR[59]	Option 0 Option 1 Option 2 Option 3	GPIO[59] M3C0P SSD3_1 eMIOS0[13]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	107	123	V25
PD[14]	PCR[60]	Option 0 Option 1 Option 2 Option 3	GPIO[60] M3C1M SSD3_2 eMIOS0[14]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	108	124	V24

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PORT F											
PF[0]	PCR[70]	Option 0 Option 1 Option 2 Option 3	GPIO[70] eMIOS1[19] EVTO DCULITE_B2	—	SIUL PWM/Timer NEXUS DCULite	I/O	M	None, None	157	189	C20
PF[1]	PCR[71]	Option 0 Option 1 Option 2 Option 3	GPIO[71] eMIOS1[20] MSEO DCULITE_B3	—	SIUL PWM/Timer NEXUS DCULite	I/O	M	None, None	158	190	B20
PF[2]	PCR[72]	Option 0 Option 1 Option 2 Option 3	GPIO[72] NMI — —	—	SIUL NMI — —	I/O	S	None, None	45	53	AC7
PF[3]	PCR[73]	Option 0 Option 1 Option 2 Option 3	GPIO[73] eMIOS1[21] MSEO DCULITE_B4	—	SIUL PWM/Timer NEXUS DCULite	I/O	M	None, None	159	191	A20
PF[4]	PCR[74]	Option 0 Option 1 Option 2 Option 3	GPIO[74] eMIOS1[14] SDA_1 DCULITE_B5	—	SIUL PWM/Timer I^2C_1 DCULite	I/O	M	None, None	160	192	D19
PF[5]	PCR[75]	Option 0 Option 1 Option 2 Option 3	GPIO[75] QUADSPI_IO1_B eMIOS1[15] VIU8_PDI16	—	SIUL QuadSPI PWM/Timer VIU2/PDI	I/O	M	None, None	161	193	A19
PF[6]	PCR[76]	Option 0 Option 1 Option 2 Option 3	GPIO[76] QUADSPI_IO0_B eMIOS1[16] VIU9_PDI17	—	SIUL QuadSPI PWM/Timer VIU2/PDI	I/O	M	None, None	162	194	D18
PF[7]	PCR[77]	Option 0 Option 1 Option 2 Option 3	GPIO[77] eMIOS1[15] SCL_1 DCULITE_B6	—	SIUL PWM/Timer I^2C_1 DCULite	I/O	M	None, None	163	195	C18
PF[8]	PCR[78]	Option 0 Option 1 Option 2 Option 3	GPIO[78] SDA_0 CS2_1 RXD_1	—	SIUL I^2C_0 DSPI_1 LINFlex_1	I/O	S	None, None	164	196	A18

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PH[6]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[7]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[8]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[9]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[10]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[11]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PORT J											
PJ[0]	PCR[105]	Option 0 Option 1 Option 2 Option 3	GPIO[105] DCULITE_B6 — I2S_DO / PWMO	—	SIUL DCULite — SGM	I/O	M	None, None	—	—	L26
PJ[1]	PCR[106]	Option 0 Option 1 Option 2 Option 3	GPIO[106] VIU1_PDI_HSYNC eMIOS1[9] eMIOS0[8]	—	SIUL VIU2/PDI PWM/Timer PWM/Timer	I/O	S	None, None	4	4	U4
PJ[2]	PCR[107]	Option 0 Option 1 Option 2 Option 3	GPIO[107] VIU0_PDI_VSYNC eMIOS1[14] eMIOS0[9]	—	SIUL VIU2/PDI PWM/Timer PWM/Timer	I/O	S	None, None	5	5	U3
PJ[3]	PCR[108]	Option 0 Option 1 Option 2 Option 3	GPIO[108] VIU_PCLK eMIOS0[22] PDI_DE	—	SIUL VIU2 PWM/Timer PDI	I/O	S	None, None	60	72	AD15
PJ[4]	PCR[109]	Option 0 Option 1 Option 2 Option 3	GPIO[109] VIU2_PDI0 eMIOS0[21] eMIOS0[23]	—	SIUL VIU2/PDI PWM/Timer PWM/Timer	I/O	S	None, None	56	68	AD14

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PK[7]	PCR[128]	Option 0 Option 1 Option 2 Option 3	GPIO[128] RXD_2 DCULITE_R2 TCON[8]	—	SIUL LINFlex_2 DCULite TCON	I/O	M	None, None	—	44	AD5
PK[8]	PCR[129]	Option 0 Option 1 Option 2 Option 3	GPIO[129] TXD_2 DCULITE_R3 TCON[9]	—	SIUL LINFlex_2 DCULite TCON	I/O	M	None, None	—	45	AE5
PK[9]	PCR[130]	Option 0 Option 1 Option 2 Option 3	GPIO[130] I2S_DO / PWMO DCULITE_R4 TCON[10]	—	SIUL SGM DCULite TCON	I/O	M	None, None	—	46	AF5
PK[10]	PCR[131]	Option 0 Option 1 Option 2 Option 3	GPIO[131] SDA_1 eMIOS1[12] DCULITE_TAG	—	SIUL I^2C_1 PWM/Timer DCULite	I/O	S	None, None	51	59	AF8
PK[11]	PCR[132]	Option 0 Option 1 Option 2 Option 3	GPIO[132] SCL_1 eMIOS1[13] DCU_TAG	—	SIUL I^2C_1 PWM/Timer DCU3	I/O	S	None, None	52	60	AC9
PK[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PORT L											
PL[0]	PCR[133]	Option 0 Option 1 Option 2 Option 3	GPIO[133] — CANRX_1 SDA_1	ANS[19]	SIUL — FlexCAN_1 I2C1	I/O	M / ANALOG	None, None	—	81	AE22
PL[1]	PCR[134]	Option 0 Option 1 Option 2 Option 3	GPIO[134] — CANTX_1 SCL_1	ANS[18]	SIUL — FlexCAN_1 I2C1	I/O	M / ANALOG	None, None	—	82	AE21

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PL[11]	PCR[144]	Option 0 Option 1 Option 2 Option 3	GPIO[144] eMIOS1[11] DCULITE_G3 —	—	SIUL PWM/Timer DCULite —	I/O	M	None, None	—	175	A24
PL[12]	PCR[145]	Option 0 Option 1 Option 2 Option 3	GPIO[145] eMIOS1[12] DCULITE_G4 —	—	SIUL PWM/Timer DCULite —	I/O	M	None, None	—	176	C23
PL[13]	PCR[146]	Option 0 Option 1 Option 2 Option 3	GPIO[146] eMIOS1[13] DCULITE_G5 —	—	SIUL PWM/Timer DCULite —	I/O	M	None, None	—	177	B23
PL[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PL[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PORT M											
PM[0]	PCR[147]	Option 0 Option 1 Option 2 Option 3	GPIO[147] I2S_SCK / PWMO DCULITE_R5 TCON[11]	—	SIUL SGM DCULite TCON	I/O	M	None, None	—	61	AE9
PM[1]	PCR[148]	Option 0 Option 1 Option 2 Option 3	GPIO[148] I2S_FS DCULITE_R6 —	—	SIUL SGM DCULite —	I/O	M	None, None	—	62	AF9
PM[2]	PCR[149]	Option 0 Option 1 Option 2 Option 3	GPIO[149] eMIOS1[17] DCULITE_R7 DCULITE_DE	RSDSCLKM	SIUL PWM/Timer DCULite DCULite	I/O	M	None, None	—	173	D23
PM[3]	PCR[150]	Option 0 Option 1 Option 2 Option 3	GPIO[150] CANRX_2 RXD_3 TCON[4]	—	SIUL FlexCAN_2 LINFlex_3 TCON	I/O	M	None, None	—	16	Y3
PM[4]	PCR[151]	Option 0 Option 1 Option 2 Option 3	GPIO[151] CANTX_2 TXD_3 TCON[5]	—	SIUL FlexCAN_2 LINFlex_3 TCON	I/O	M	None, None	—	17	Y2

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PM[5]	PCR[152]	Option 0 Option 1 Option 2 Option 3	GPIO[152] VIU5_PDI13 eMIOS1[22] DCU_TAG	—	SIUL VIU2/PDI PWM/Timer DCU3	I/O	M	None, None	16	—	—
PM[6]	PCR[153]	Option 0 Option 1 Option 2 Option 3	GPIO[153] VIU6_PDI14 eMIOS1[23] DCULITE_TAG	—	SIUL VIU2/PDI PWM/Timer DCULite	I/O	M	None, None	17	—	—
PM[7]	PCR[154]	Option 0 Option 1 Option 2 Option 3	GPIO[154] VIU8_PDI16 I2S_DO / PWMOA eMIOS1[16]	—	SIUL VIU2/PDI SGM PWM/Timer	I/O	S	None, None	39	—	—
PM[8]	PCR[155]	Option 0 Option 1 Option 2 Option 3	GPIO[155] VIU9_PDI17 I2S_SCK / PWMO eMIOS1[23]	—	SIUL VIU2/PDI SGM PWM/Timer	I/O	S	None, None	40	—	—
PM[9]	PCR[156]	Option 0 Option 1 Option 2 Option 3	GPIO[156] PDI_PCLK SGM_MCLK eMIOS0[8]	—	SIUL PDI SGM PWM/Timer	I/O	M	None, None	113	—	—
PM[10]	PCR[157]	Option 0 Option 1 Option 2 Option 3	GPIO[157] RXD_2 CANRX_2 eMIOS0[16]	—	SIUL LINFlex_2 FlexCAN_2 PWM/Timer	I/O	S	None, None	114	—	—
PM[11]	PCR[158]	Option 0 Option 1 Option 2 Option 3	GPIO[158] TXD_2 CANTX_2 eMIOS0[23]	—	SIUL LINFlex_2 FlexCAN_2 PWM/Timer	I/O	S	None, None	115	—	—
PM[12]	PCR[159]	Option 0 Option 1 Option 2 Option 3	GPIO[159] DCULITE_B7 — I2S_SCK / PWMO	—	SIUL DCULite — SGM	I/O	M	None, None	—	—	L24
PM[13]	PCR[160]	Option 0 Option 1 Option 2 Option 3	GPIO[160] DCULITE_PCLK — SGM_MCLK	—	SIUL DCULite — SGM	I/O	F	None, None	—	—	L23
PM[14]	—	—	Reserved	—	—	—	—	—	—	—	—

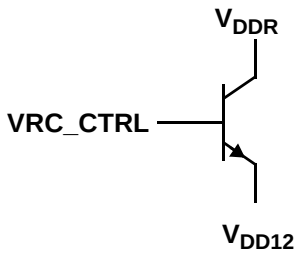


Figure 6. External NPN ballast connections

Table 18. Voltage regulator electrical characteristics

Symbol		C	Parameter		Conditions	Min	Max	Unit	SpecID
V_{DDR}	SR	P	Power supply		—	3.0	5.5	V	D5.1
T_J	SR	D	Junction temperature		—	-40	140	°C	D5.2
I_{REG}	CC	T	Current consumption		Reference included, @ 55 °C No load @ Full load	—	 2 11	mA	D5.3
I_L	CC	T	Output current capacity		DC load current	—	450	mA	D5.4
V_{DD12}	CC	D	Output voltage (value @ I_L = 0 @ 27°C)		Pre-trimming sigma < 7 mV	—	1.330	V	D5.5
		P			Post-trimming	1.145	1.32		
		T	Output voltage (value @ I_L = Imax)		Post-trimming	1.145	—		
	SR	D	External decoupling/stability capacitor		4 capacitances of 10 µF each	10 * 4		µF	D5.6
		D			ESR of external cap	0.05	0.2	Ω	
		D			1 bond wire R + 1 pad R	0.2	1	Ω	
L_{BOND}	CC	D	Bonding Inductance for Bipolar Base Control pad		—	0	15	nH	D5.7
	CC	D	Power supply rejection	@ DC @ no load	Cload = 10 µF * 4	—	–30	dB	D5.8
		D		@ 200 kHz @ no load			–100		
		D		@ DC @ 400 mA			–30		
		D		@ 200 kHz @ 400 mA			–30		
	CC	D	Load current transient		Cload = 10 µF * 4	—	10% to 90% of I_L (max) in 100 ns		D5.9
t_{SU}	CC	T	Start-up time after input supply stabilizes[1]		Cload = 10 µF * 4	—	500	µs	D5.10

[1] Time after the input supply to the voltage regulator has ramped up (VDDR) and the voltage regulator has asserted the Power OK signal.

Table 22. DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
$I_{DDSTDBY2}$	CC	D	STANDBY2 mode current[9] (64K SRAM on)	SXOSC (32KHz) ON and RTC running	$T_A = –40^oC$	—	470	—	µA
		D			$T_A = 0^oC$	—	480	—	
		P			$T_A = 25^oC$	—	481	490	
		D			$T_A = 55^oC$	—	525	—	
		D			$T_A = 85^oC$	—	650	—	
		P			$T_A = 105^oC$	—	870	910	
	CC	D		SXOSC (32KHz) and RTC OFF	$T_A = –40^oC$	—	63	—	µA
		D			$T_A = 0^oC$	—	85	—	
		P			$T_A = 25^oC$	—	93	100	
		D			$T_A = 55^oC$	—	95	—	
		D			$T_A = 85^oC$	—	190	—	
		P			$T_A = 105^oC$	—	390	430	
$I_{DDSTDBY1}$	CC	D	STANDBY1 mode current (8K SRAM on)[10]	SXOSC (32KHz) ON and RTC running	$T_A = –40^oC$	—	415	—	µA
		D			$T_A = 0^oC$	—	422	—	
		P			$T_A = 25^oC$	—	426	430	
		D			$T_A = 55^oC$	—	575	—	
		D			$T_A = 85^oC$	—	680	—	
		P			$T_A = 105^oC$	—	810	915	
	CC	D		SXOSC (32 KHz) and RTC OFF	$T_A = –40^oC$	—	20	—	µA
		D			$T_A = 0^oC$	—	22	—	
		P			$T_A = 25^oC$	—	29	75	
		D			$T_A = 55^oC$	—	47	—	
		D			$T_A = 85^oC$	—	118	—	
		P			$T_A = 105^oC$	—	236	410	

1 V_{DD} = 3.0V to 5.5V, T_A = -40 to 105 °C, unless otherwise specified.

2 I_{DDMAX} is composed of the current consumption on all supplies (V_{DD12}, V_{DDE_A}, V_{DDE_B}, V_{DDA}, V_{DDR}, V_{DDM}, V_{DDPLL}, V_{DD_DR}). It does not include current consumption linked to I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application; switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

3 Higher current may be sinked by device during power-up and standby exit. Please refer to inrush current in Table 23.

4 RUN current measured with typical application and accesses on both flash and RAM.

5 Data and Code Flash in Normal Power. Code fetched from RAM: DCUs running with 20MHz pixel clock, QuadSPI fetching data at 80MHz, GPU accessing internal SRAM and external DRAM, DMA, RLE, and VIU active, Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/ADC/SMD/SSD/SGM) and running at max frequency, periodic SW/WDG timer reset enabled.

Table 29. AVG IDDE specifications

Cell	Period (ns)	Load (pF)[1]	VDDE (V)	Drive/slew select	IDDE (mA)
pad_msr_hv[2]	24	50	5.5	11	14
	62	50	5.5	01	5.3
	317	50	5.5	00	1.1
	425	200	5.5	00	3
pad_ssr_hv[2]	37	50	5.5	11	9
	130	50	5.5	01	2.5
	650	50	5.5	00	0.5
	840	200	5.5	00	1.5

1 All loads are lumped loads.

2 Average current is for pad configured as output only. Use pad_i current for input.

4.8.3 DC specification for CMOS090_ddr library @ VDDE = 3.3 V

Table 30. DC electrical specifications at 3.3 V VDDE

Symbol		Parameter	Value		Unit	SpecID
			Min	Max		
Vdd	SR	Core supply voltage	1.08	1.32	V	D9.71
Vdde	SR	I/O supply voltage	3.0	3.6	V	D9.72
Vdd33	SR	I/O pre-driver supply voltage	3.0	3.6	V	D9.73
Vref	SR	Input reference voltage	1.3	1.7	V	D9.74
Vtt	SR	Termination voltage	Vref–0.05	Vref+0.05	V	D9.75
Vih	SR	Input high voltage	Vref+0.20	—	V	D9.76
Vil	SR	Input low voltage	—	Vref–0.2	V	D9.77
Voh	SR	Output high voltage	Vtt+0.8	—	V	D9.78
Vol	SR	Output low voltage	—	Vtt–0.8	V	D9.79

Table 31. Output drive current @ VDDE = 3.3 V (+/-10%)

Pad	C	Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)
pad_st_acc	D	111	–16	16
pad_st_dq	D	111	–16	16

4.19.2 Nexus Debug Interface

Table 57. Nexus Debug Port Timing[1]

Num	Symbol		C	Characteristic	Min	Max	Unit	SpecID
1	t_{MCYC}	CC[2]	D	MCKO Cycle Time	15	—	ns	A2.1
2	t_{MDC}	CC[2]	D	MCKO Duty Cycle	40	60	%	A2.2
3	t_{MDOV}	CC[2]	D	MCKO Low to MDO Data Valid[3]	0.1	0.2	t_{MCYC}	A2.3
4	t_{MSEOV}	CC[2]	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[3]	0.1	0.2	t_{MCYC}	A2.4
5	t_{EVTOV}	CC[2]	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[3]	0.1	0.2	t_{MCYC}	A2.5
6	t_{EVTIPW}	CC[2]	D	$\overline{\text{EVTI}}$ Pulse Width	4	—	t_{TCYC}	A2.6
7	t_{EVTOPW}	CC[2]	D	$\overline{\text{EVTO}}$ Pulse Width	1	—	t_{MCYC}	A2.7
8	t_{TCYC}	CC[2]	D	TCK Cycle Time[4]	100	—	ns	A2.8
9	t_{TDC}	CC[2]	D	TCK Duty Cycle	40	60	%	A2.9
10	t_{NTDIS}, t_{NTMSS}	CC[2]	D	TDI, TMS Data Setup Time	25	—	ns	A2.10
11	t_{NTDIH}, t_{NTMSH}	CC[2]	D	TDI, TMS Data Hold Time	5	—	ns	A2.11
12	t_{JOV}	CC[2]	D	TCK Low to TDO Data Valid	0	35	ns	A2.12

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 3.0 V to 3.6 V, T_A = -40 to 105 °C, and CL = 50 pF (Cl=30 pF on MCKO), with SRC = 0b10 for MCKO and 0b11 for others.

2 Parameter values guaranteed by design.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

4 The system clock frequency needs to be three times faster that the TCK frequency.

NOTE

Nexus Dual Data Rate is not supported. The timings are mentioned for dedicated pins on 416BGA. The max value for #2, 3 and 4 above, are 0.3 of tMCYC for shared nexus ports.

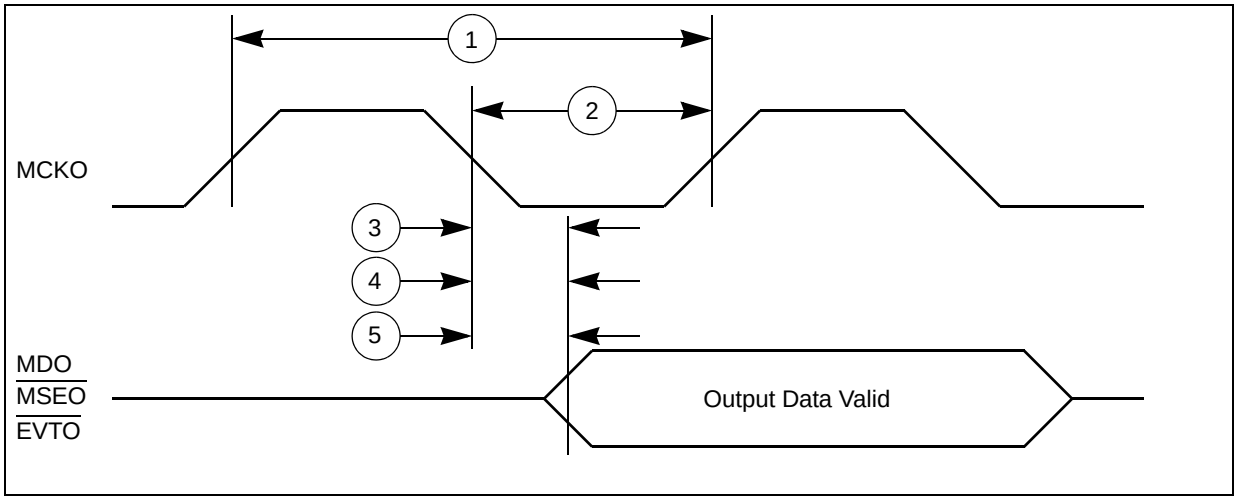


Figure 20. Nexus Output Timing

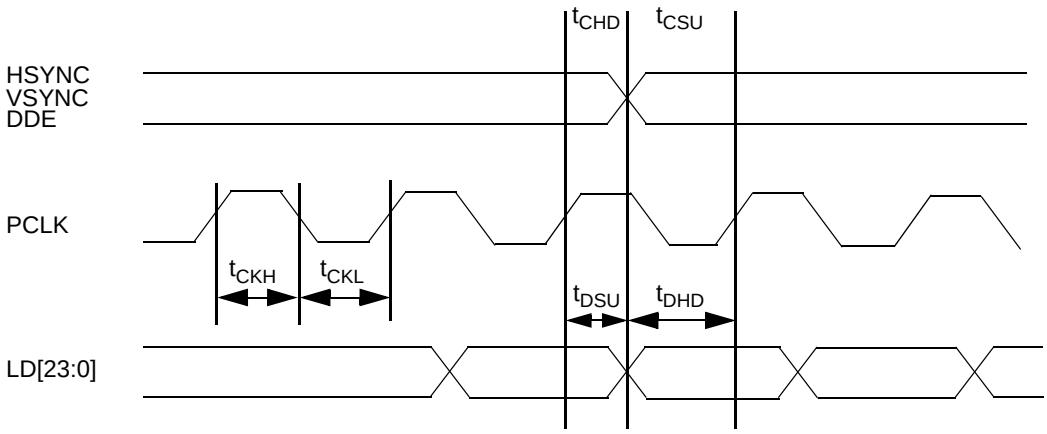


Figure 26. LCD Interface Timing Parameters—Access Level

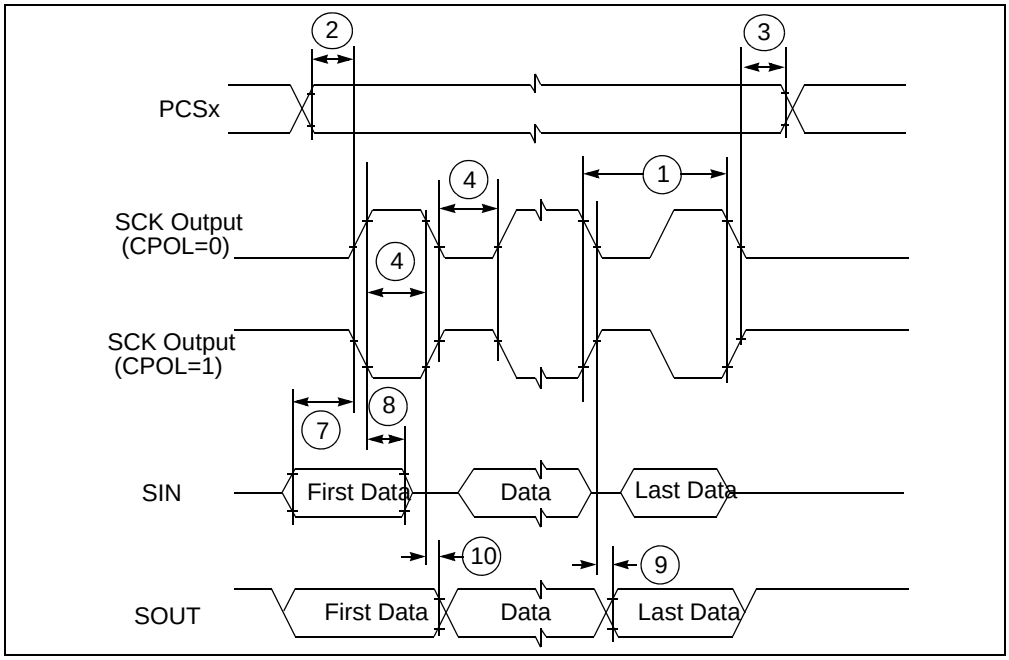


Figure 36. DSPI Classic SPI Timing — Master, CPHA = 0

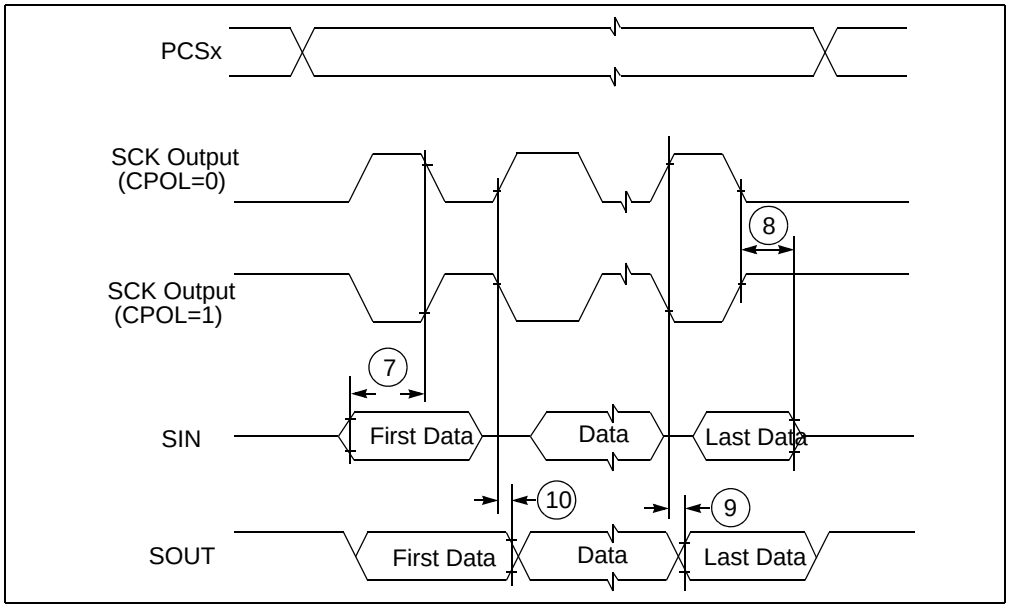


Figure 37. DSPI Classic SPI Timing — Master, CPHA = 1

Table 75. QuadSPI timing events

Number	Event
1	Last address out
2	Address captured at flash memory
3	Data out from flash memory
4	Ideal data capture edge
5	Delayed data capture edge with QSPI_SMPR=0x0000_000X
6	Delayed data capture edge with QSPI_SMPR=0x0000_002X
7	Delayed data capture edge with QSPI_SMPR=0x0000_004X
8	Delayed data capture edge with QSPI_SMPR=0x0000_006X

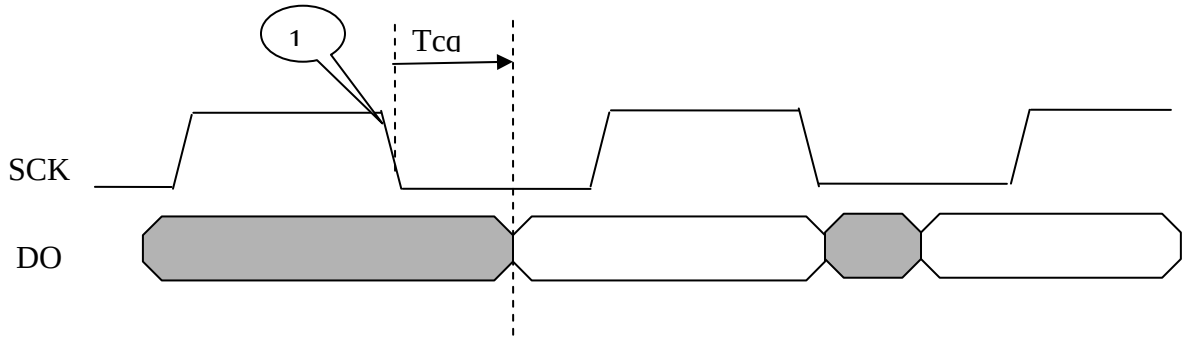
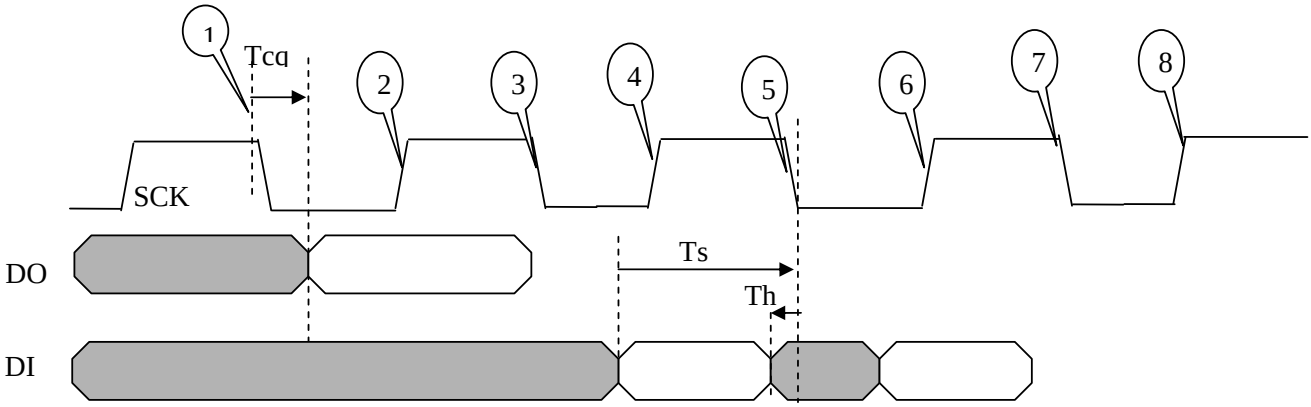


Figure 45. QuadSPI output timing



Note: Ts and Th correspond to QSPI_SMPR = 0x0000_000X.

Figure 46. QuadSPI input timing

Table 78. Revision history (continued)

Revision (Date)	Description
12 (30 Oct 2014)	In Figure 3. "208-pin LQFP pinout": • “DCU_LITE_TAG” added and “DCU_TAG” removed for PK10. • “DCU_TAG” added and “DCULITE_TAG” removed for PK11. • “SDA_1” added for PL0. • “SCL_1” added for PL1. In Section 1.4.13, "Display Control Unit (DCU3)", added a feature “Support displays up to 800 x 480 pixel resolutions”. In Figure 4. "416 TEPBGA package pinout", added MSEO2 pin in added in column 17, 3rd last row. In Table 7. "Port pin summary": • Updated “Function” and “Peripheral” entries for PL[0] and PL[1]. • For PB[7], PM[0], PM[8], and PM[12], changed PWMOA to PWMO. • For PB[8], PB[10], and PM[7], changed PWMO to PWMOA. In Section 3.1, "Power-up sequencing", added a note “Vreg bypass mode is for factory testing only”. Removed “Pad AC specifications (3.3 V, PAD3V5V = 1)” table and “Pad AC specifications (3.3 V, PAD3V5V = 1)” section. Updated values of V_{DDR} in Table 13. "Recommended operating conditions (5.0 V)" to 4.5-5.5 V. Updated temperature in table note 7 of Table 22. "DC electrical characteristics", from 110 ^{0}C to 105 ^{0}C. Updated Table 47. "Program and erase specifications" with following modifications: • Added rows for 64KB and 256KB programming timings • Updated timings for 16KB and 128KB programming timings • Removed row for 32KB programming timings Updated Figure 57. “416 TEPBGA Mechanical Drawing (Part 1 of 2)“ and Figure 58. “416 TEPBGA Mechanical Drawing (Part 2 of 2)“.
13 (13 Apr 2015)	Added a note in Section 2.4.1, "Pad configuration during reset phases". In Table 67. "VIU2 timing parameters", updated the max value of VIU2 pixel clock frequency. Added a table note for this entry. In Section 1.3, "Feature list", updated from "Interrupt Controller (INTC) with 181 peripheral interrupt sources and eight software interrupts" to "Interrupt Controller (INTC) with 163 peripheral interrupt sources and eight software interrupts". In Figure 59. “Commercial product code structure“, updated the temperature range for “C” as -40 C to 85 C and for “V” as -40 C to 85/105 C. Updated Table 77. "Orderable part number summary". Following changes were made in Rev 12 of DS but were not captured in Rev 12’s revision history: • In Figure 2. "176-pin LQFP pinout", changed “MCK0” to “MCKO” for pin 174 and added “MSEO2” to pin 159 • In Table 7. "Port pin summary", added SDA_1 function and I2C1 peripheral for PL[0] port pin and added SCL_1 function and I2C1 peripheral for PL[1] port pin.