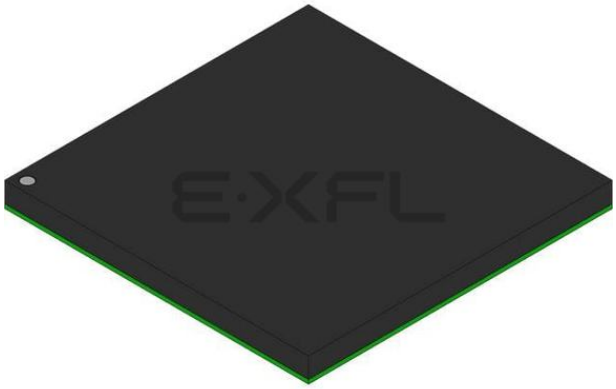

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	125MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	177
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.064M x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5645sf1vvu

- 16-bit modulus down counter with interrupt

1.4.33 Sound Generator Module (SGM)

The SGM features the following:

- 4-channel audio mixer
- Each channel capable of independent Tone generation or Wave playback
- Individual channel volume control (8-bit resolution)
- Tone Mode:
  - Programmable Tone frequency
  - Programmable amplitude envelope: attack, duration, and decay
  - Programmable number of tone pulses and inter-tone duration
- Wave Mode:
  - One FIFO per channel working in conjunction with eDMA
  - Supports standard audio sampling rates (4 kHz, 8 kHz, 11.025 kHz, 16 kHz, 22.050 kHz, 32 kHz, 44.100 kHz, 48 kHz)
  - Same sample rate applies to all channels
  - 8-bit, 12-bit, 16-bit input data formats
  - Programmable wave duration and inter-wave duration
  - Repeat mode with programmable number of wave playbacks
- SGM Output:
  - 16-bit PWM channel
  - Integrated I^2S master interface for connection to external audio DAC

1.4.34 IEEE 1149.1 JTAG controller (JTAGC)

JTAGC features the following:

- Backward compatible to standard JTAG IEEE 1149.1-2001 test access port (TAP) interface
- Support for boundary scan testing

1.4.35 Nexus Development Interface (NDI)

The Nexus 3 module is compliant with Class 3 of the IEEE-ISTO 5001-2008 standard, with additional Class 4 features available. The following features are implemented:

- Program Trace via Branch Trace Messaging (BTM). Branch trace messaging displays program flow discontinuities (direct and indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus static code may be traced.
- Data Trace via Data Write Messaging (DWM) and Data Read Messaging (DRM). This provides the capability for the development tool to trace reads and/or writes to selected internal memory resources.
- Ownership Trace via Ownership Trace Messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An Ownership Trace Message is transmitted when a new process/task is activated, allowing the development tool to trace ownership flow.
- Run-time access to embedded processor memory map via the JTAG port. This allows for enhanced download/upload capabilities.
- Watchpoint Messaging via the auxiliary pins provides visibility when debugging.
- Watchpoint Trigger enablement of Program and/or Data Trace Messaging enhances debug capability.

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PB[1]	PCR[17]	Option 0 Option 1 Option 2 Option 3	GPIO[17] CANRX_0 RXD_0 —	—	SIUL FlexCAN_0 LINFlex_0 —	I/O	S	None, none	12	12	V1
PB[2]	PCR[18]	Option 0 Option 1 Option 2 Option 3	GPIO[18] TXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, none	153	183	D21
PB[3]	PCR[19]	Option 0 Option 1 Option 2 Option 3	GPIO[19] RXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, none	152	182	A22
PB[4]	PCR[20]	Option 0 Option 1 Option 2 Option 3	GPIO[20] SCK_1 MA0 —	—	SIUL DSPI_1 ADC —	I/O	S	None, none	62	74	AF15
PB[5]	PCR[21]	Option 0 Option 1 Option 2 Option 3	GPIO[21] SOUT_1 MA1 FABM	—	SIUL DSPI_1 ADC Control	I/O	S	Input, pull-down	63	75	AC16
PB[6]	PCR[22]	Option 0 Option 1 Option 2 Option 3	GPIO[22] SIN_1 MA2 ABS[0]	—	SIUL DSPI_1 ADC Control	I/O	S	Input, pull-up	64	76	AF16
PB[7]	PCR[23]	Option 0 Option 1 Option 2 Option 3	GPIO[23] SIN_0 eMIOS1[20] I2S_SCK/PWMO	—	SIUL DSPI_0 PWM/Timer SGM	I/O	S	None, none	55	67	AC14
PB[8]	PCR[24]	Option 0 Option 1 Option 2 Option 3	GPIO[24] SOUT_0 eMIOS1[19] I2S_DO/PWMOA	—	SIUL DSPI_0 PWM/Timer SGM	I/O	S	None, none	54	66	AF13
PB[9]	PCR[25]	Option 0 Option 1 Option 2 Option 3	GPIO[25] SCK_0 eMIOS1[18] I2S_FS	—	SIUL DSPI_0 PWM/Timer SGM	I/O	M	None, none	53	65	AC13

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PORT F											
PF[0]	PCR[70]	Option 0 Option 1 Option 2 Option 3	GPIO[70] eMIOS1[19] EVTO DCULITE_B2	—	SIUL PWM/Timer NEXUS DCULite	I/O	M	None, None	157	189	C20
PF[1]	PCR[71]	Option 0 Option 1 Option 2 Option 3	GPIO[71] eMIOS1[20] MSEO DCULITE_B3	—	SIUL PWM/Timer NEXUS DCULite	I/O	M	None, None	158	190	B20
PF[2]	PCR[72]	Option 0 Option 1 Option 2 Option 3	GPIO[72] NMI — —	—	SIUL NMI — —	I/O	S	None, None	45	53	AC7
PF[3]	PCR[73]	Option 0 Option 1 Option 2 Option 3	GPIO[73] eMIOS1[21] MSEO DCULITE_B4	—	SIUL PWM/Timer NEXUS DCULite	I/O	M	None, None	159	191	A20
PF[4]	PCR[74]	Option 0 Option 1 Option 2 Option 3	GPIO[74] eMIOS1[14] SDA_1 DCULITE_B5	—	SIUL PWM/Timer I^2C_1 DCULite	I/O	M	None, None	160	192	D19
PF[5]	PCR[75]	Option 0 Option 1 Option 2 Option 3	GPIO[75] QUADSPI_IO1_B eMIOS1[15] VIU8_PDI16	—	SIUL QuadSPI PWM/Timer VIU2/PDI	I/O	M	None, None	161	193	A19
PF[6]	PCR[76]	Option 0 Option 1 Option 2 Option 3	GPIO[76] QUADSPI_IO0_B eMIOS1[16] VIU9_PDI17	—	SIUL QuadSPI PWM/Timer VIU2/PDI	I/O	M	None, None	162	194	D18
PF[7]	PCR[77]	Option 0 Option 1 Option 2 Option 3	GPIO[77] eMIOS1[15] SCL_1 DCULITE_B6	—	SIUL PWM/Timer I^2C_1 DCULite	I/O	M	None, None	163	195	C18
PF[8]	PCR[78]	Option 0 Option 1 Option 2 Option 3	GPIO[78] SDA_0 CS2_1 RXD_1	—	SIUL I^2C_0 DSPI_1 LINFlex_1	I/O	S	None, None	164	196	A18

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PK[7]	PCR[128]	Option 0 Option 1 Option 2 Option 3	GPIO[128] RXD_2 DCULITE_R2 TCON[8]	—	SIUL LINFlex_2 DCULite TCON	I/O	M	None, None	—	44	AD5
PK[8]	PCR[129]	Option 0 Option 1 Option 2 Option 3	GPIO[129] TXD_2 DCULITE_R3 TCON[9]	—	SIUL LINFlex_2 DCULite TCON	I/O	M	None, None	—	45	AE5
PK[9]	PCR[130]	Option 0 Option 1 Option 2 Option 3	GPIO[130] I2S_DO / PWMO DCULITE_R4 TCON[10]	—	SIUL SGM DCULite TCON	I/O	M	None, None	—	46	AF5
PK[10]	PCR[131]	Option 0 Option 1 Option 2 Option 3	GPIO[131] SDA_1 eMIOS1[12] DCULITE_TAG	—	SIUL I^2C_1 PWM/Timer DCULite	I/O	S	None, None	51	59	AF8
PK[11]	PCR[132]	Option 0 Option 1 Option 2 Option 3	GPIO[132] SCL_1 eMIOS1[13] DCU_TAG	—	SIUL I^2C_1 PWM/Timer DCU3	I/O	S	None, None	52	60	AC9
PK[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PK[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PORT L											
PL[0]	PCR[133]	Option 0 Option 1 Option 2 Option 3	GPIO[133] — CANRX_1 SDA_1	ANS[19]	SIUL — FlexCAN_1 I2C1	I/O	M / ANALOG	None, None	—	81	AE22
PL[1]	PCR[134]	Option 0 Option 1 Option 2 Option 3	GPIO[134] — CANTX_1 SCL_1	ANS[18]	SIUL — FlexCAN_1 I2C1	I/O	M / ANALOG	None, None	—	82	AE21

The following pad types are available for system pins and functional port pins:

Table 9. Pad Types

Pad	Function
S	Slow (pad_ssr, pad_ssr_hv)
M	Medium (pad_msr, pad_msr_hv)
F	Fast (pad_fc)
J	Input/output with analog features (pad_tgate, pad_tgate_hv)
Analog	Input only with analog features (pad_ae, pad_ae_hv)
SMD	Stepper Motor Detector
DDR	DDR pads
RSDS	RSDS pads

4.5 Thermal characteristics

Table 13. Recommended operating conditions (5.0 V)

Symbol		C	Parameter	Conditions	Value		Unit	SpecID
					Min	Max		
V_{DDA}[1]	SR	P	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	+4.5	+5.5	V	D2.19
		D		Voltage drop[2]	+3.0	+5.5		
		D		Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1		
V_{SSA}	SR	D	Voltage on VSSA (ADC reference) pin with respect V_{SS}	—	V_{SS}–0.1	V_{SS}+0.1	V	D2.20
V_{DDPLL}	CC	P	Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground (V_{SSPLL})	—	1.08	1.32	V	D2.21
V_{DDR}[3]	SR	P	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	+4.5	+5.5	V	D2.22
		D		Voltage drop[2]	+4.5	+5.5		
		D		Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1		
V_{SSR}	SR	D	Voltage on VSSR (regulator ground) pin with respect to V_{SS}	—	V_{SS}–0.1	V_{SS}+0.1	V	D2.23
V_{DD12}[4,5]	CC	P	Voltage on VDD12 pin with respect to ground (V_{SS12})	—	1.08	1.4	V	D2.24
V_{SS12}	CC	D	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS}–0.1	V_{SS}+0.1	V	D2.25
V_{DD}[6,7]	SR	P	Voltage on VDD pins (VDDE_A, VDDE_B, VDD_DR, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})	Voltage drop[2]	V_{DDmin}[6]	V_{DDmax}[6]	V	D2.26
V_{SS}[8]	SR	D	I/O supply ground	—	0	0	V	D2.27
V_{DDE_A}[9]	SR	P	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})	—	+4.5	+5.5	V	D2.28
V_{DDE_B}[10]	SR	P	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})	—	+3.0	+3.6	V	D2.29
V_{DDM}	SR	P	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})	—	+4.5	+5.5	V	D2.30
V_{DD_DR}[11]		P	Voltage on V_{DD_DR} with respect to V_{SS}	—	+1.62	+3.6	V	D2.31
V_{SS_DR}		D	Voltage on V_{SSRSDS} with respect to V_{SS}	—	+1.62	+3.6	V	D2.32
V_{RSDS}		P	Voltage on V_{DD_DR} with respect to V_{SS}	—	+3.0	+3.6	V	D2.33
TV_{DD}	SR	D	V_{DD} slope to ensure correct power up[12]	—	—	12	V/ms	D2.34
T_A	SR	P	Ambient temperature under bias	—	–40	+105	°C	D2.35
					–40	+105		
T_J	SR	D	Junction temperature under bias	—	–40	+140	—	D2.36

1 100 nF capacitance needs to be provided between V_{DDA}/V_{SSA} pair.

2 Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, I/O DC and ADC electrical characteristics may not be guaranteed below 4.5 V during the voltage drop sequence.

3 10 µF capacitance must be connected between V_{DDR} and V_{SS12}. It is recommended that this cap should be placed, as close as possible to the DUT pin on board.

Table 15. Thermal characteristics for 208-pin LQFP[1] (continued)

Symbol		C	Parameter	Conditions	Value	Unit	SpecID
Ψ_{JT}	CC	D	Junction to Package Top Natural Convection[5]	—	2	°C/W	D3.14

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 16. Thermal characteristics for 416-pin TEPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit	SpecID
$R_{\theta JA}$	CC	D	Junction to Ambient Natural Convection[2]	Single layer board - 1s	26	°C/W	D3.15
$R_{\theta JA}$	CC	D	Junction to Ambient Natural Convection[2]	Four layer board - 2s2p	18	°C/W	D3.16
$R_{\theta JMA}$	CC	D	Junction to Ambient[2]	@200 ft./min., single layer board - 1s	20	°C/W	D3.17
$R_{\theta JMA}$	CC	D	Junction to Ambient[2]	@200 ft./min., Four layer board - 2s2p	15	°C/W	D3.18
$R_{\theta JB}$	CC	D	Junction to Board[3]	—	10	°C/W	D3.19
$R_{\theta JCtop}$	CC	D	Junction to Case (Top)[4]	—	6	°C/W	D3.20
Ψ_{JT}	CC	D	Junction to Package Top Natural Convection[5]	—	2	°C/W	D3.21

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.5.1 General notes for specifications at maximum junction temperature

An estimate of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \qquad \textit{Eqn. 1}$$

where:

T_A= ambient temperature for the package (^oC)

$R_{\theta JA}$= junction to ambient thermal resistance ($^oC/W$)

P_D= power dissipation in the package (W)

Table 21. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit	SpecID
					Min	Typ	Max		
V_{PORH}	CC	C	Power-on reset threshold	—	1.5	—	2.7	V	D5.11
$V_{LVDHV3H}$	CC	C	LVDHV3 low voltage detector high threshold	—	—	—	2.9		D5.12
$V_{LVDHV3L}$	CC	C	LVDHV3 low voltage detector low threshold	—	2.5	—	—		D5.13
$V_{LVDHV5H}$	CC	C	LVDHV5 low voltage detector high threshold	—	—	—	4.4		D5.14
$V_{LVDHV5L}$	CC	C	LVDHV5 low voltage detector low threshold	—	3.9	—	—		D5.15
$V_{LVDLVCORH}$	CC	C	LVDLVCOR low voltage detector high threshold	T_A = 25°C, after trimming	—	—	1.185		D5.16
$V_{LVDLVCORL}$	CC	C	LVDLVCOR low voltage detector low threshold		1.095	—	—		D5.17

1 V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = -40 / +105°C, unless otherwise specified

2 All values need to be confirmed during device validation.

4.7.3 Low voltage domain power consumption

Table 22 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 22. DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—	—	—	295	375[3]	mA
I_{DDRUN}[4]	CC	P	RUN mode typical average current[5]	f_{CPU} = 125MHz, Dual Display Drive with external DRAM, 416 TEPBGA package option only	—	—	275	—	mA
				f_{CPU} = 125MHz, Single Display Drive, no external DRAM, 176 LQFP / 208 LQFP package options	—	—	240	—	
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128KHz) running	T_A = 25 °C	—	17.5	23.5	mA
		P			T_A = 105 °C	—	35	45.5	
I_{DDSTOP}	CC	D	STOP mode current[7] [8]	Slow internal RC oscillator (128KHz) running	T_A = –40°C	—	645	—	µA
		D			T_A = 0°C	—	1100	—	
		P			T_A = 25°C	—	1531	5500	
		D			T_A = 55°C	—	3.8	—	mA
		D			T_A = 85°C	—	9.7	—	
		C			T_A = 105°C	—	17.67	36.5	

[6] Flash in Low Power. RC-osc128KHz & RC-OSC 16MHzon. 10MHz XTAL clock.FlexCAN: instances: 0, 1ON (clocked but no reception or transmission), LINFLEX: instances 0, 1, 2 ON (clocked but no reception or transmission). eMIOS: instance: 0, 1 ON - 16 channels on with PWM20KHz. DSPI: instance: 0 (clocked but no communication). DCUs, TCON, VIU, GPU clock gated, RTC/API ON.PIT ON. STM ON. ADC ON but not converting.

[7] For Tj > 105 ^{0}C , HPvreg needs to be kept ON. The consumption increases beyond this temperature and to handle the extra current, HPvreg should be ON.

[8] No clock, RC 16MHz off, RCI 128KHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

[9] ULPreg ON, HP/LPVreg off, 64KB RAM on, device configured for minimum consumption, all possible modules switched-off.

[10] ULPreg ON, HP/LPVreg off, 8KB RAM on, device configured for minimum consumption, all possible modules switched-off.

4.8 DC electrical specifications

4.8.1 DC specification for CMOS090LP2 library @ VDDE = 3.3 V

NOTE

These pad specifications are applicable for pads in the Digital segment Only. See the "GPIO power bank supplies and functionality" table in the "Voltage Regulators and Power Supplies" chapter of the reference manual for details.

Table 23. DC electrical specifications

Symbol		C	Parameter	Condition	Value		Unit	SpecID
					Min	Max		
Vdd	SR	P	Core supply voltage	—	1.08	1.32	V	D9.1
Vdde	SR	P	I/O supply voltage	—	3.0	3.6	V	D9.2
Vdd33	SR	P	I/O pre-driver supply voltage	—	3.0	3.6	V	D9.3
Vih_c	SR	P	CMOS input buffer high voltage	With hysteresis enabled	0.65×Vdde	Vdde+0.3	V	D9.4
				With hysteresis disabled	0.55×Vdde	Vdde+0.3		
Vil_c	SR	P	CMOS input buffer low voltage	With hysteresis enabled	Vss–0.3	0.35×Vdde	V	D9.5
				With hysteresis disabled	Vss–0.3	0.40×Vdde		
Vhys_c	SR	T	CMOS input buffer hysteresis	—	0.1×Vdde	—	V	D9.6
Vih_fod_h	SR	P	5 V tolerant CMOS input buffer high voltage	With hysteresis enabled	0.65×Vdd33	Vdd33+0.3	V	D9.7
Vil_fod_h	SR	P	5 V tolerant CMOS input buffer low voltage	With hysteresis enabled	Vss–0.3	0.35×Vdd33	V	D9.8
Iact_s	SR	T	Selectable weak pullup/pulldown current	—	25	150	µA	D9.9
Iinact_d	SR	P	Digital pad input leakage current	Weak pull inactive	–2.5	2.5	µA	D9.10

4.8.2 DC specification for CMOS090LP2fg library @ VDDE = 5.0 V

NOTE

These pad specifications are applicable for pads in the Analog segment Only. See the "GPIO power bank supplies and functionality" table in the "Voltage Regulators and Power Supplies" chapter of the reference manual for details.

Table 26. DC electrical specifications

Symbol		C	Parameter	Condition	Value		Unit	SpecID
					Min	Max		
Vdd	SR	P	Core supply voltage	—	1.08	1.32	V	D9.17
Vdde	SR	P	I/O supply voltage	—	4.5	5.5	V	D9.18
Vdd33	SR	P	I/O pre-driver supply voltage	—	3.0	3.6	V	D9.19
Vih_hys	SR	P	CMOS input buffer high voltage	With hysteresis enabled	0.65×Vdde	Vdde+0.3	V	D9.20
Vil_hys	SR	P	CMOS input buffer low voltage	With hysteresis enabled	Vss–0.3	0.35×Vdde	V	D9.21
Vih	SR	P	CMOS input buffer high voltage	With hysteresis disabled	0.55×Vdde	Vdde+0.3	V	D9.22
Vil	SR	P	CMOS input buffer low voltage	With hysteresis disabled	Vss–0.3	0.40×Vdde	V	D9.23
Vhys	SR	T	CMOS input buffer hysteresis	—	0.1×Vdde	—	V	D9.24
Pull_Ioh	SR	P	Weak pullup current	—	35	135	µA	D9.25
Pull_Iol	SR	P	Weak pulldown current	—	35	200	µA	D9.26
Iinact_d	SR	P	Digital pad input leakage current	Weak pull inactive	–2.5	2.5	µA	D9.27
Iinact_a	SR	P	Analog pad input leakage current	Weak pull inactive	–150	150	nA	D9.28
Voh	SR	P	Slew rate controlled output high voltage	—	0.8×Vdde	—	V	D9.29
Vol	SR	P	Slew rate controlled output low voltage	—	—	0.2×Vdde	V	D9.30
Voh_ls	SR	C	Low swing output pad output high voltage	—	2.64	—	V	D9.31
Ioh_msr	SR	C	pad_msr_hv Ioh	—	11.6	40.7	mA	D9.32
Iol_msr	SR	C	pad_msr_hv Iol	—	17.7	68.2	mA	D9.33
Ioh_ssr	SR	C	pad_ssr_hv Ioh	—	6.0	21.3	mA	D9.34
Iol_ssr	SR	C	pad_ssr_hv Iol	—	9.2	36.3	mA	D9.35
Rtgate	SR	D	Pad_tgate_hv input resistance	—	250	800	Ω	D9.39

Table 31. Output drive current @ VDDE = 3.3 V (+/-10%) (continued)

Pad	C	Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)
pad_st_clk	D	111	–16	16
pad_st	D	111	–16	16
pad_st_odt	D	111	–16	16
pad_st_ck	D	111	–16	16

4.8.4 DC specification for CMOS090_ddr library @ VDDE = 2.5 V

Table 32. DC electrical specifications at 2.5 V VDDE

Symbol		C	Parameter	Value		Unit	SpecID
				Min	Max		
Vdd	SR	P	Core supply voltage	1.08	1.32	V	D9.80
Vdde	SR	P	I/O supply voltage	2.3	2.7	V	D9.81
Vdd33	SR	P	I/O pre-driver supply voltage	3.0	3.6	V	D9.82
Vref	SR	P	Input reference voltage	0.49×Vdde	0.51×Vdde	V	D9.83
Vtt	SR	P	Termination voltage	Vref–0.04	Vref+0.04	V	D9.84
Vih	SR	P	Input high voltage	Vref+0.15	—	V	D9.85
Vil	SR	P	Input low voltage	—	Vref–0.15	V	D9.86
Voh	SR	P	Output high voltage	Vtt+0.81	—	V	D9.87
Vol	SR	P	Output low voltage	—	Vtt–0.81	V	D9.88

Table 33. Output drive current @ VDDE = 2.5 V (+/-200mV)

Pad	C	Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)	Libraries
pad_st_acc	D	011	–16.2	16.2	6MDDR
pad_st_dq	D	011	–16.2	16.2	6MDDR
pad_st_ck	D	011	–16.2	16.2	6MDDR

4.8.5 DC specification for CMOS090_ddr library @ VDDE = 1.8 V

Table 34. DC electrical specifications for 1.8 V VDDE

Symbol		C	Parameter	Value		Unit	SpecID
				Min	Max		
Vdd	SR	P	Core supply voltage	1.08	1.32	V	D9.89
Vdde	SR	P	I/O supply voltage	1.7	1.9	V	D9.90
Vdd33	SR	P	I/O pre-driver supply voltage	3.0	3.6	V	D9.91
Vref	SR	P	Input reference voltage	0.49×Vdde	0.51×Vdde	V	D9.92
Vtt	SR	P	Termination voltage	Vref–0.04	Vref+0.04	V	D9.93
Vih	SR	P	Input high voltage	Vref+0.125	—	V	D9.94
Vil	SR	P	Input low voltage	—	Vref–0.125	V	D9.95
Voh	SR	P	Output high voltage	Vtt+0.81	—	V	D9.96
Vol	SR	P	Output low voltage	—	Vtt–0.81	V	D9.97

Table 35. Output drive current @ VDDE = 1.8 V (+/-100mV)

Pad		Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)	Libraries
pad_st_acc	D	000	–3.57	3.57	6MDDR
		001	–7.84	7.84	
		010	–5.36	5.36	
		110	–13.4	13.4	
pad_st_dq	D	000	–3.57	3.57	6MDDR
		001	–7.84	7.84	
		010	–5.36	5.36	
		110	–13.4	13.4	
pad_st_clk	D	000	–3.57	3.57	6MDDR
		001	–7.84	7.84	
		010	–5.36	5.36	
		110	–13.4	13.4	

4 Data based on device simulation.

5 2x sys clock required for generation of DDR timing.

6 f_{CPU} of 125 MHz can be achieved only at temperatures up to 105 °C with a maximum FM depth of 2%.

7 Data based on characterization results, not tested in production

4.14 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 45. Fast internal oscillator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit	SpecID
					Min	Typ	Max		
f_{RCM}	CC[3]	P	RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz	O12.1
I_{RCMRUN}	CC[3]	D	RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA	O12.2
I_{RCMPWD}	CC[3]	D	RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	10	µA	O12.3
ΔRCMVAR	CC[4]	C	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high-frequency configuration	—	–5	—	+5	%	O12.5

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to +105 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 Guaranteed by device simulation, not tested in production.

4 Guaranteed by device characterization, not tested in production.

4.15 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

Table 46. Slow internal RC oscillator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit	SpecID
					Min	Typ	Max		
f_{RCL}	CC[3]	P	RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz	O13.1
I_{RCL}	CC[3]	D	RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA	O13.2
ΔRCLVAR[3]	CC[3]	C	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	+10	%	O13.4

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to +105 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 Guaranteed by device simulation, not tested in production

Table 49. ADC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit	SpecID
					Min	Typ	Max		
V_{SSA}	SR	D	Voltage on VSSA (ADC reference) pin with respect to ground (V_{SS})[3]	—	-0.1	—	0.1	V	D15.1
V_{DDA}	SR	D	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	V_{DDE_A}–0.1	—	V_{DDE_A}+0.1	V	D15.2
V_{AINx}	SR	D	Analog input voltage[4]	—	V_{SSA}-0.1	—	V_{DDA}+0.1	V	D15.3
f_{ADC}	SR	D	ADC analog frequency	—	6	—	32	MHz	D15.4
t_{ADC_PU}	SR	D	ADC power up delay	—	—	—	1.5	µs	D15.5
t_{ADC_S}	CC[5]	T	Sample time[6]	f_{ADC} = 32 MHz, ADC_conf_sample_input = 17	0.5	—	—	µs	D15.6
				f_{ADC} = 6 MHz, ADC_conf_sample_input = 127	—	—	21		
t_{ADC_C}	CC[5]	T	Conversion time[7]	f_{ADC} = 32 MHz, ADC_conf_comp = 2	0.625	—	—	µs	D15.7
C_S	CC[5]	D	ADC input sampling capacitance	—	—	—	3	pF	D15.8
C_{P1}	CC[5]	D	ADC input pin capacitance 1	—	—	—	3	pF	D15.9
C_{P2}	CC[5]	D	ADC input pin capacitance 2	—	—	—	1	pF	D15.10
C_{P3}	CC[5]	D	ADC input pin capacitance 3	—	—	—	1	pF	D15.11
R_{SW1}	CC[5]	D	Internal resistance of analog source	—	—	—	3	kΩ	D15.12
R_{SW2}	CC[5]	D	Internal resistance of analog source	—	—	—	2	kΩ	D15.13
R_{AD}	CC[5]	D	Internal resistance of analog source	—	—	—	0.1	kΩ	D15.14
I_{INJ}	SR	T	Input current Injection	Current injection on one ADC input, different from the converted one	-10	—	10	mA	D15.15
INL	CC[5]	P	Integral Non Linearity	No overload	-1.5	—	1.5	LSB	D15.16
DNL	CC[5]	P	Differential Non Linearity	No overload	-1.0	—	1.0	LSB	D15.17
OFS	CC[5]	T	Offset error	After offset cancellation	—	0.5	—	LSB	D15.18
GNE	CC[5]	T	Gain error	—	—	0.6	—	LSB	D15.19

Table 52. Functional pad AC type specifications (continued)

Name	Prop. delay (ns) L>H / H>L		Rise/fall edge (ns)		Drive load (pF)	Drive/slew rate select
	Min	Max	Min	Max		MSB, LSB
pad_ssr_hv	9.2 / 6.9	27 / 28	5.5 / 4.1	15 / 17	50	11
	30 / 23	81 / 87	21 / 16	57 / 63	200	
	N/A					10
	31 / 31	80 / 90	15.4 / 15.4	38 / 42	50	01
	58 / 52	144 / 155	32 / 26	82 / 85	200	
	162 / 168	415 / 415	80 / 82	190 / 190	50	00
	216 / 205	533 / 540	106 / 95	250 / 250	200	
pad_i_hv	0.5 / 0.5	3 / 3	0.4 / 0.4	1.5 / 1.5	0.5	N/A

4.18.4 AC specification for CMOS090_ddr library @ VDDE = 3.3 V

Table 53. AC specifications at 3.3 V VDDE

Name	C	Prop. delay (ns) L>H / H>L		Rise/fall edge (ns)		Drive load (pF)	Drive/slew rate select	Libraries
		Min	Max	Min	Max		MSB, LSB	
pad_st_acc	C	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111	6MDDR
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20		
pad_st_dq	C	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111	6MDDR
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20		
pad_st_clk	C	1.4/1.4	2.4/2.4	3.1/2.5	5.7/5.7	5	111	6MDDR
		1.6/1.6	2.6/2.6	1.1/1.3	2.3/2.3	20		

4.18.5 AC specification for CMOS090_ddr library @ VDDE = 2.5 V

Table 54. AC specifications at 2.5 V VDDE

Name	C	Prop. delay (ns) L>H / H>L		Rise/fall edge (ns)		Drive load (pF)	Drive/slew rate select	Libraries
		Min	Max	Min	Max		MSB, LSB	
pad_st_acc	C	1.4/1.5	2.5/2.4	2.1/2.1	4.3/4.1	5	011	6MDDR
		1.7/1.7	2.8/2.7	0.6/0.7	1.1/1.3	20		
pad_st_dq	C	1.4/1.5	2.5/2.4	2.1/2.1	4.3/4.1	5	011	6MDDR
		1.7/1.7	2.8/2.7	0.6/0.7	1.1/1.3	20		
pad_st_clk	C	1.4/1.4	2.4/2.4	2.1/2.1	4.4/4.1	5	011	6MDDR
		1.1/1.6	2.7/2.7	0.6/0.7	1.6/1.8	20		

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 66 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

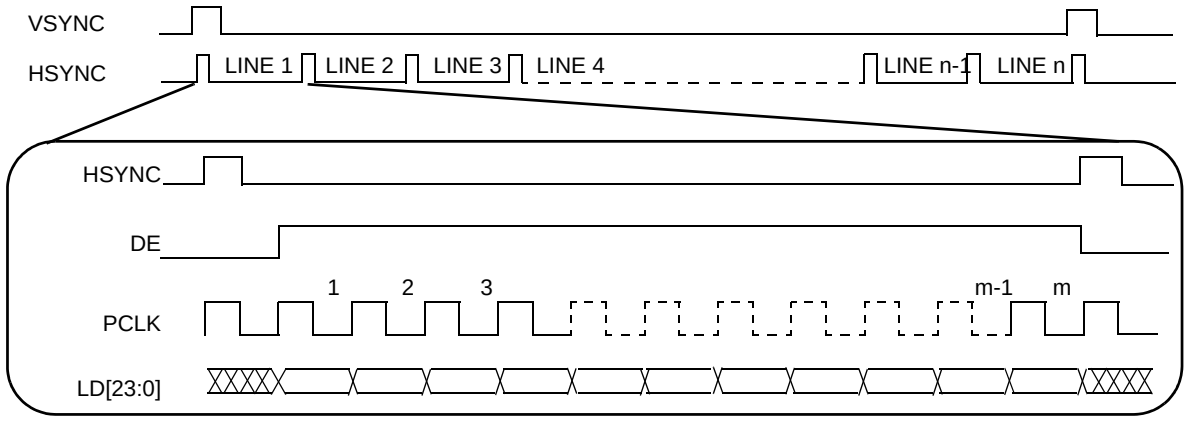


Figure 23. TFT LCD interface timing overview[1]

4.19.3.1 Interface to TFT LCD Panels—Pixel Level Timings

Figure 24 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high.

Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the DCU Clock Confide Register (DCCR) in the system clock module.

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

1. In Figure 23, the “LD[23:0]” signal is “line data,” an aggregation of the DCU’s RGB signals—R[0:7], G[0:7] and B[0:7].

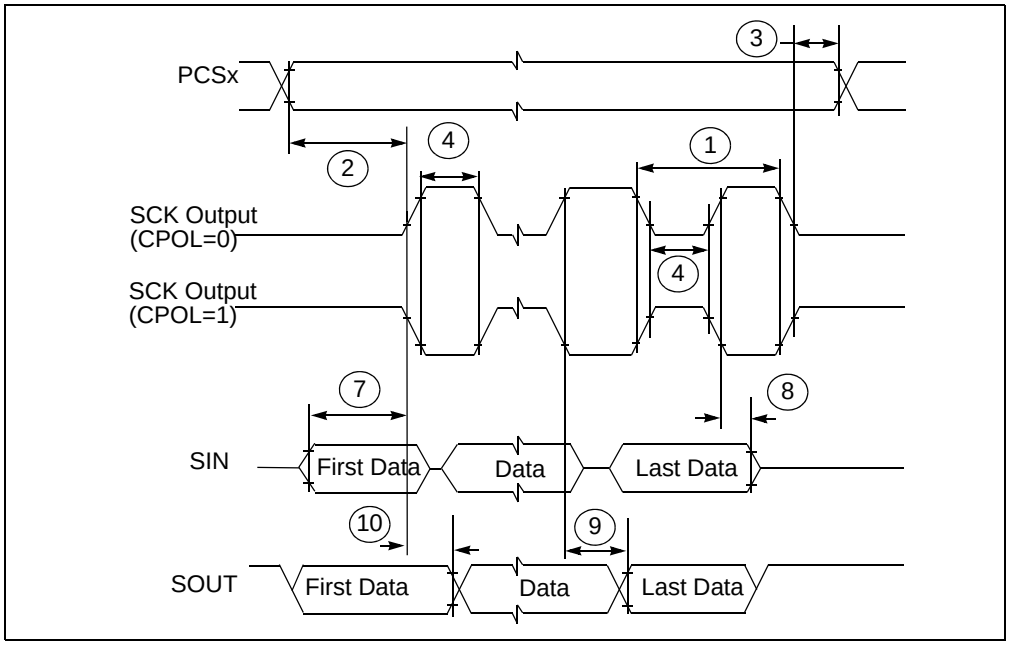


Figure 40. DSPI Modified Transfer Format Timing — Master, CPHA = 0

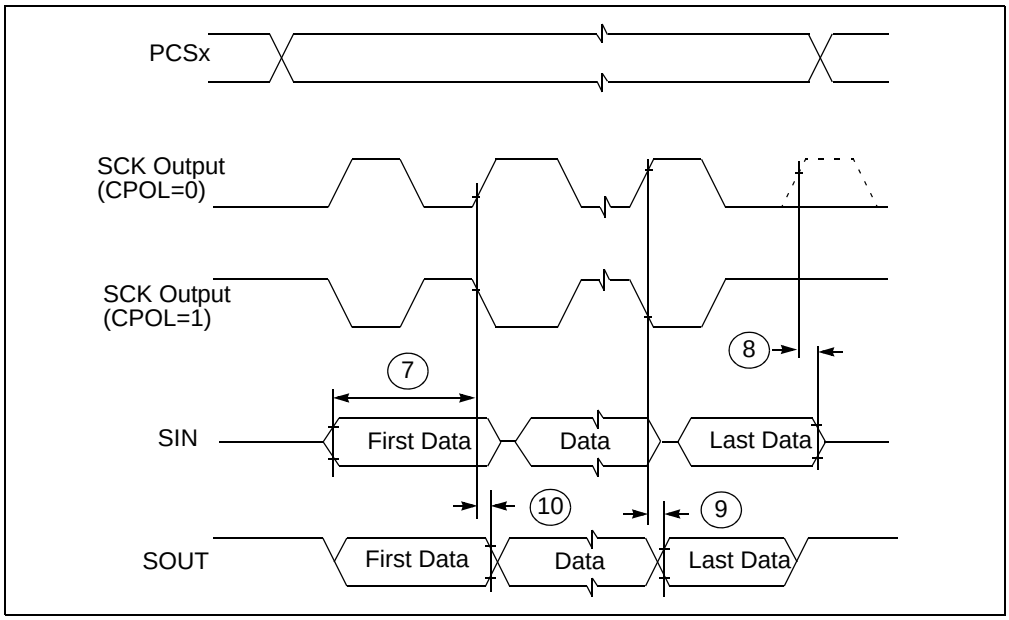
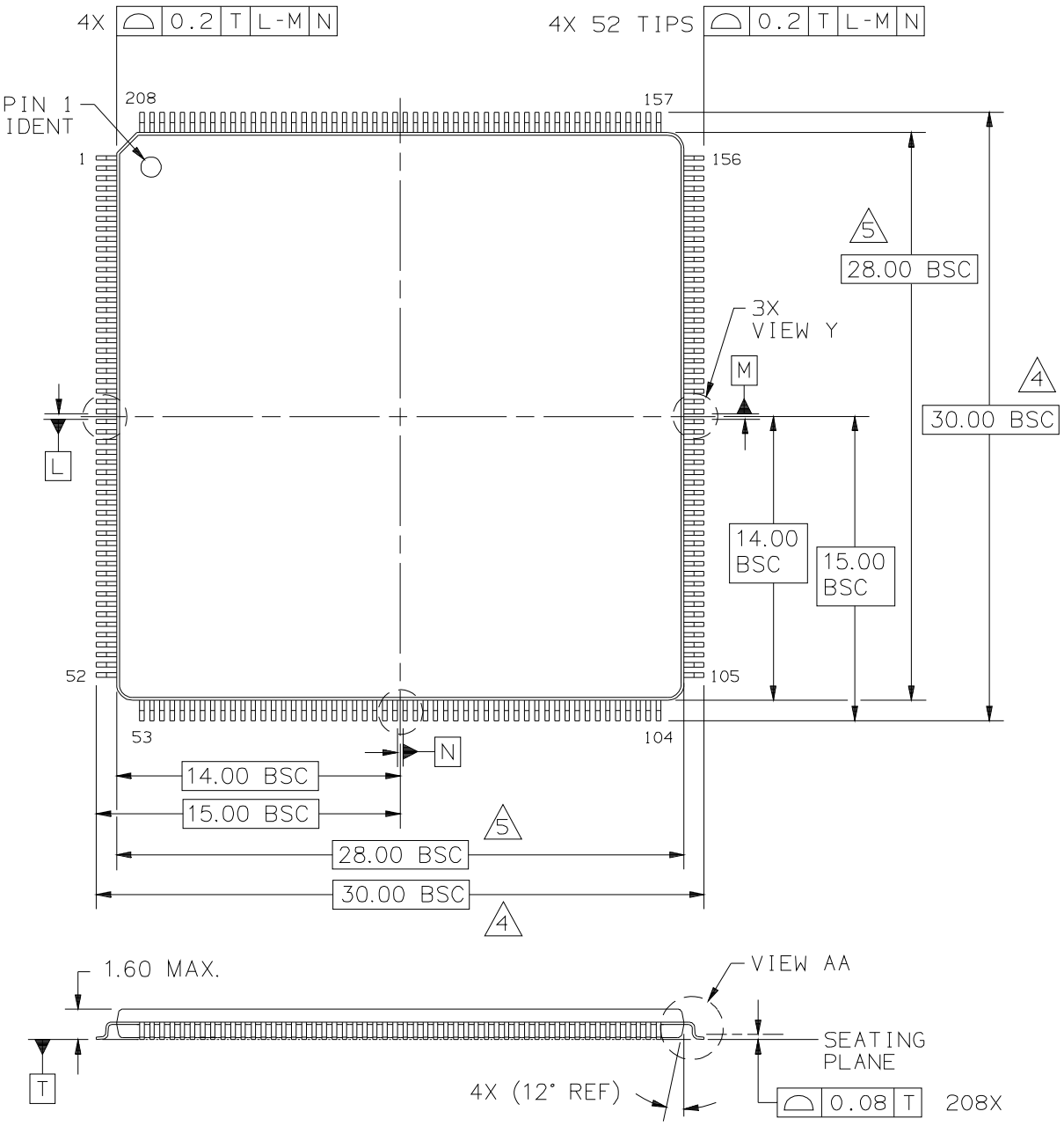


Figure 41. DSPI Modified Transfer Format Timing — Master, CPHA = 1



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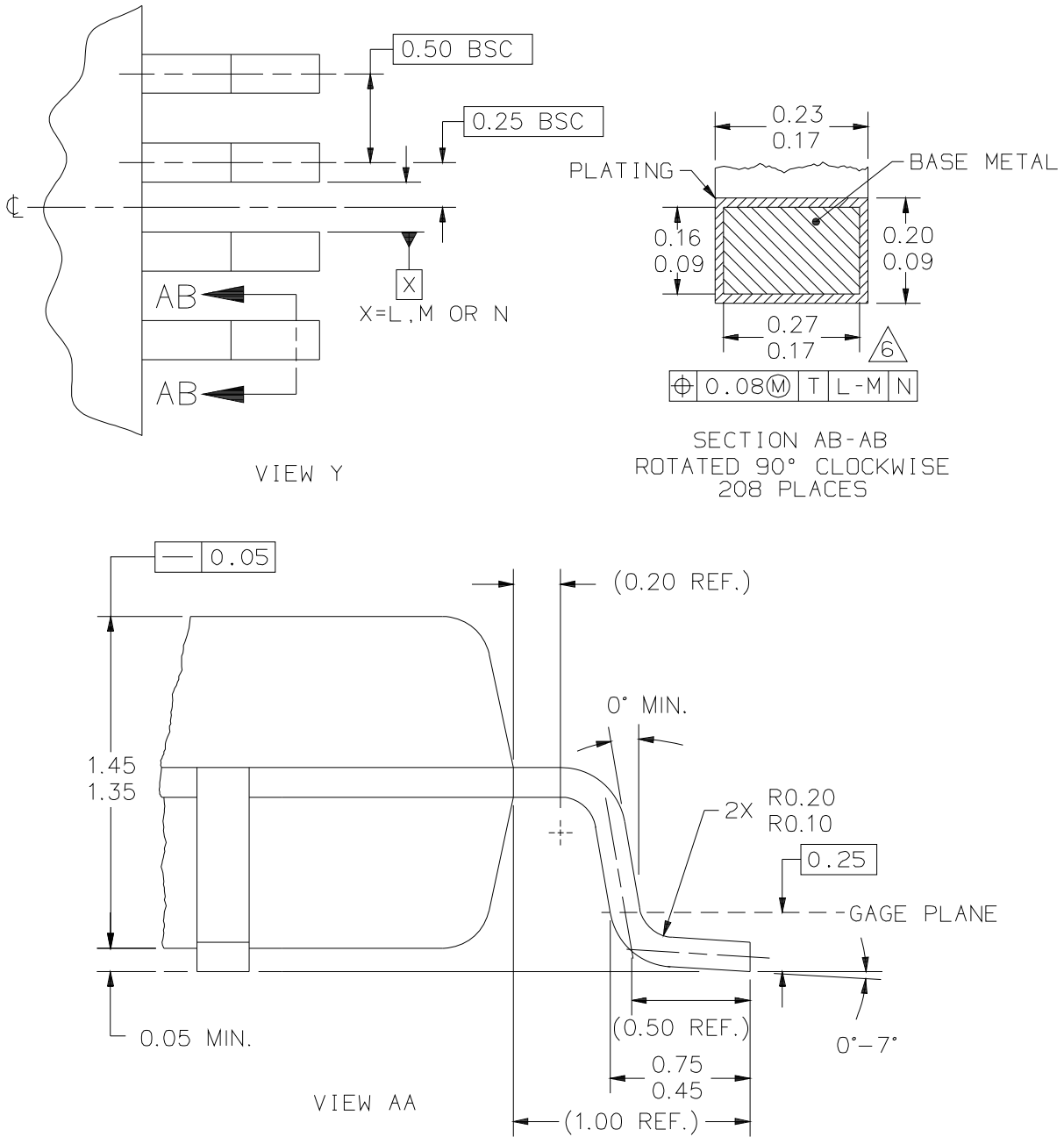
TITLE: 208 LD TQFP, 28 X 28 PKG, 0.50 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23458W	REV: C
	CASE NUMBER: 998-01	20 MAY 2005
	STANDARD: JEDEC MS-026 BJB	

Figure 54. LQFP208 Mechanical Drawing (Part 1 of 3)



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	CASE NUMBER: 998-01	20 MAY 2005
	STANDARD: JEDEC MS-026 BJB	

Figure 55. LQFP208 Mechanical Drawing (Part 2 of 3)

Table 78. Revision history (continued)

Revision (Date)	Description
5 (continued) (25 Feb 2011)	In the “Absolute maximum ratings” table: • Changed max value for V_{DDE_B} from 5.5V to 3.6 V. • Changed max value for V_{DD_DR} from TBD to 3.6 V. • Changed max value for V_{RSDS} from TBD to 3.6 V. • Changed max value for V_{IN} from 5.5V to “V_{DDmax} (VDDE max of that segment)“. • Removed “Relative to V_{DD}“ condition for V_{IN}. In the “Recommended operating conditions (3.3 V)” table: • Changed min value for “V_{DD}“ from 3.0 V to “V_{DDmin}“. • Changed max value for “V_{DD}“ from 3.6 V to “V_{DDmax}“. • Changed V_{DD} entry to include only V_{DDE_A}, V_{DDE_B}, V_{DD_DR}, and V_{DDM}. • Corrected error in V_{DDE_A} entry, changed reference in “parameter” column from V_{DDE_C} to V_{DDE_A}. • Added V_{DD_DR} to the V_{DD} footnote. In the “Recommended operating conditions (5.0 V)” table: • Added footnote for V_{DDE_B} max values. • Added footnote for V_{DD_DR} typ values. • Changed min and max values for V_{DD_DR} from 4.5V and 5.5V to 3.0V and 3.6V, respectively. • Changed max value for V_{DD_DR} (under “voltage drop” conditions) from 5.5V to 3.6V. • Changed min and max values for V_{DD} from 4.5V and 5.5V to V_{DDmin} and V_{DDmax}, also referenced footnote 6. • Removed VDDE_C and VDDE_E from the VDD “parameter” description and footnote, and added VDD_DR. • Changed min and max values for V_{DDE_B} from 4.5V and 5.5V to 3.0V and 3.6V, respectively. Removed the “Libraries” column from the DC specifications “library“ tables. Removed the 75Ω and 50Ω cases and added details on the 150Ω case in the “ODT DC electrical characteristics” table. Changed the “Main oscillator electrical characteristics“ section name to “Fast external crystal oscillator (4-16 MHz) electrical characteristics“ and modified text and table name within the section appropriately. Removed the “Full swing Pierce” condition and the relevant footnotes from the “Fast external crystal oscillator (4-16 MHz) electrical characteristics“ table. Changed the “Low power oscillator electrical characteristics“ section name to “Slow external crystal oscillator (32 KHz) electrical characteristics“ and modified the text, figure, and table names within the section appropriately. Changed “main oscillator” to “fast external oscillator” in the “FMPLL electrical characteristics” table. Updated parameters, conditions, and values in the “FMPLL electrical characteristics“ table. Changed the “Main RC oscillator electrical characteristics“ section name to “Fast Internal RC oscillator (16 MHz) electrical characteristics“ and modified the text and table name within the section appropriately. Changed the “Low power RC oscillator electrical characteristics“ section name to “Slow Internal RC oscillator (128 KHz) electrical characteristics“ and modified the text and table name within the section appropriately. Removed duplicate entry of TUEP in the “ADC electrical characteristics” table. Removed pad_pci and pad_osc48 from the “Functional pad type AC specifications“ table because they are not used. Added new “Pad mode configurations” table to the “DRAM Interface” section. Changed the 324-pin TEPBGA pinout to 416-pin TEPBGA. Changed the 324-pin TEPBGA mechanical drawing to 416-pin TEPBGA.