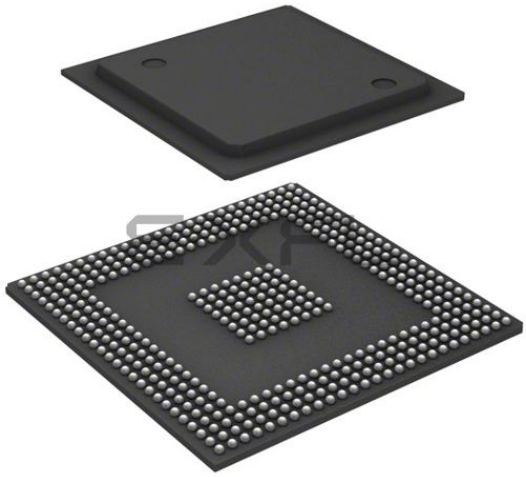

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	125MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	177
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.064M x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5645sf1vvur

1.3 Feature list

- Dual-issue, 32-bit Power Architecture Book E compliant CPU core complex (e200z4d)
  - Memory Management Unit (MMU)
  - 4 KB, 2/4-way instruction cache
- 2 MB on-chip ECC flash memory with:
  - Flash memory controller
  - Prefetch buffers
- 64 KB on-chip ECC SRAM
- 1 MB on-chip non-ECC graphics SRAM with two-port graphics SRAM controller
- Memory Protection Unit (MPU) with up to 16 region descriptors and 32-byte region granularity to provide basic memory access permission and ensure separation between different codes and data
- Interrupt Controller (INTC) with 163 peripheral interrupt sources and eight software interrupts
- Two Frequency-Modulated Phase-Locked Loops (FMPLLs)
  - Primary FMPLL (FMPLL0) provides a system clock up to 125 MHz
  - Auxiliary FMPLL (FMPLL1) is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules, QuadSPI and as alternate clock to the DCU and DCU-Lite for pixel clock generation
- Crossbar switch architecture enables concurrent access of peripherals, flash memory or RAM from multiple bus masters
- 16-channel Enhanced Direct Memory Access controller (eDMA) with multiple transfer request sources using a DMA channel multiplexer
- Boot Assist Module (BAM) with 8 KB dedicated ROM for embedded boot code supports boot options including download of boot code via a serial link (CAN or SCI)
- Two Display Control Units (DCU3 and DCULite) for direct drive of up to two TFT LCD displays up to XGA resolution
- Timing Controller (TCON) and RSDS interface for the DCU3 module
- 2D OpenVG 1.1 and raster graphics accelerator (GFX2D)
- Video Input Unit (VIU2) supporting 8/10-bit ITU656 video input, YUV to RGB conversion, video down-scaling, de-interlacing, contrast adjustment and brightness adjustment.
- DRAM controller supporting DDR1, DDR2, and LPDDR1 DRAMs
- Stepper Motor Controller (SMC)
  - High-current drivers for up to six instrument cluster gauges driven in full dual H-bridge configuration
  - Stepper motor return-to-zero and stall detection module
  - Stepper motor short circuit detection
- Sound Generator Module (SGM)
  - 4-channel mixer
  - Supports PCM wave playback and synthesized tones
  - Optional PWM or I^2S outputs
- Two 16-channel Enhanced Modular Input Output System (eMIOS) modules
  - Support a range of 16-bit Input Capture, Output Compare, Pulse Width Modulation and Quadrature Decode functions
- 10-bit Analog-to-Digital Converter (ADC) with a maximum conversion time of 1 µs
  - Up to 20 internal channels
  - Up to 8 external channels
- Three Deserial Serial Peripheral Interface (DSPI) modules for full-duplex, synchronous, communications with external devices
- QuadSPI serial flash memory controller

- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for 4 concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

1.4.12 2D Graphics Accelerator (GFX2D)

- Native vector graphics rendering
  - Compatible with OpenVG1.1
  - Complete hardware OpenVG 1.1 rendering pipeline
  - Both geometry and pixel processing
  - Adaptive processing of Bezier curves and strokes
- 16-sample edge anti-aliasing
  - High image quality, font scalability, etc.
  - 4× Rotated Grid Supersampling (RGSS) AA for Flash
- 3D perspective texturing, reflections, and shadowing
- Shading (linear or radial gradient)
- Separate 2D engine for BitBlt, fill, and ROP operations
- Significant performance improvement when compared to software or 3D GPU-based OpenVG implementations

1.4.13 Display Control Unit (DCU3)

The DCU3 is a display controller designed to drive TFT LCD displays up to WVGA resolution using direct blit graphics and video.

The DCU3 generates all the necessary signals required to drive the TFT LCD displays: up to 24-bit RGB data bus, Pixel Clock, Data Enable, Horizontal-Sync, and Vertical-Sync.

The flexible architecture of the DCU3 enables the display of OpenVG-rendered frame buffer content and direct blit rendered graphics simultaneously.

An optional Timing Controller (TCON) and RSDS interface is available to directly drive the row and column drivers of a display panel.

Internal memory resource of the device allows to easily handle complex graphics contents (pictures, icons, languages, fonts).

The DCU3 supports 4-plane blending and 16 graphics layers. Control Descriptors (CDs) associated with each of the 16 layers enable effective merging of different resolutions into one plane to optimize use of internal memory buffers. A layer may be constructed from graphic content of various resolutions including indexed colors of 1, 2, 4, and 8 bpp, direct colors of 16, 24, and 32 bpp, and a YUV 4:2:2 color space. The ability of the DCU3 to handle input data in resolutions as low as 1bpp, 2bpp, and 4bpp enables a highly efficient use of internal memory resources of the MPC5645S. A special tiled mode can be enabled on any of the 16 layers to repeat a pattern optimizing graphic memory usage.

A hardware cursor can be managed independently of the layers at blending level increasing the efficient use of the internal DCU3 resources.

To secure the content of all critical information to be displayed, a safety mode can be activated to check the integrity of critical data along the whole system data path from the memory to the TFT pads.

The DCU3 features the following:

- Display color depth: up to 24 bpp
- Generation of all RGB and control signals for TFT
- Four-plane blending

- Maximum number of Input Layers: 16 (fixed priority)
- Dynamic Look-Up-Table (Color and Gamma Look-Up)
- α–blending range: up to 256 levels
- Transparency Mode
- Gamma Correction
- Tiled mode on all the layers
- Hardware Cursor
- Supports YCrCb 4:2:2 input data format
- RLE decode inline supporting direct read of RLE compressed images from system memory
- Critical display content integrity monitoring for Functional Safety support
- Internal Direct Memory Access (DMA) module to transfer data from internal and / or external memory
- Support displays up to 800 x 480 pixel resolutions

The DCU3 also features a Parallel Data Interface (PDI) to receive external digital video or graphic content into the DCU3. The PDI input is directly injected into the DCU3 background plane FIFO. When the PDI is activated, all the DCU3 synchronization is extracted from the external video stream to guarantee the synchronization of the two video sources.

The PDI can be used to:

- Connect a video camera output directly to the PDI
- Connect a secondary display driver as slave with a minimum of extra cost
- Connect a device gathering various Video sources
- Provide flexibility to allow the DCU to be used in slave mode (external synchronization)

The PDI features the following:

- Supported color modes:
  - 8-bit mono
  - 8-bit color multiplexed
  - RGB565
  - 16-bit/18-bit RAW color
- Supported synchronization modes:
  - embedded ITU-R BT.656-4 (RGB565 mode 2)
  - HSYNC, VSYNC
  - Data Enable
- Direct interface with DCU3 background plane FIFO
- Synchronization generation for the DCU3

1.4.14 Display Control Unit Lite (DCULite)

The DCULite is a display controller designed to enable the MPC5645S to drive a second TFT LCD display up to XGA resolution using direct blit graphics and video. The DCULite includes all features of the DCU3, including the PDI with the following exceptions:

- Reduced from 4-plane to 2-plane blending
- Reduced from 16 layers to 4 layers
- Reduced CLUT size

1.4.15 Timing Controller (TCON) and RSDS interface

The TCON enables direct drive of the row and column drivers of display panels enabling emulation of TCON ICs used in display panels.

- 16-bit modulus down counter with interrupt

1.4.33 Sound Generator Module (SGM)

The SGM features the following:

- 4-channel audio mixer
- Each channel capable of independent Tone generation or Wave playback
- Individual channel volume control (8-bit resolution)
- Tone Mode:
  - Programmable Tone frequency
  - Programmable amplitude envelope: attack, duration, and decay
  - Programmable number of tone pulses and inter-tone duration
- Wave Mode:
  - One FIFO per channel working in conjunction with eDMA
  - Supports standard audio sampling rates (4 kHz, 8 kHz, 11.025 kHz, 16 kHz, 22.050 kHz, 32 kHz, 44.100 kHz, 48 kHz)
  - Same sample rate applies to all channels
  - 8-bit, 12-bit, 16-bit input data formats
  - Programmable wave duration and inter-wave duration
  - Repeat mode with programmable number of wave playbacks
- SGM Output:
  - 16-bit PWM channel
  - Integrated I^2S master interface for connection to external audio DAC

1.4.34 IEEE 1149.1 JTAG controller (JTAGC)

JTAGC features the following:

- Backward compatible to standard JTAG IEEE 1149.1-2001 test access port (TAP) interface
- Support for boundary scan testing

1.4.35 Nexus Development Interface (NDI)

The Nexus 3 module is compliant with Class 3 of the IEEE-ISTO 5001-2008 standard, with additional Class 4 features available. The following features are implemented:

- Program Trace via Branch Trace Messaging (BTM). Branch trace messaging displays program flow discontinuities (direct and indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus static code may be traced.
- Data Trace via Data Write Messaging (DWM) and Data Read Messaging (DRM). This provides the capability for the development tool to trace reads and/or writes to selected internal memory resources.
- Ownership Trace via Ownership Trace Messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An Ownership Trace Message is transmitted when a new process/task is activated, allowing the development tool to trace ownership flow.
- Run-time access to embedded processor memory map via the JTAG port. This allows for enhanced download/upload capabilities.
- Watchpoint Messaging via the auxiliary pins provides visibility when debugging.
- Watchpoint Trigger enablement of Program and/or Data Trace Messaging enhances debug capability.

- Data Acquisition Messaging (DQM) allows code to be instrumented to export customized information to the Nexus Auxiliary Output Port.
- Address Translation Messaging via program correlation messages displays updates to the TLB for use by the debugger in correlating virtual and physical address information.
- Auxiliary interface for higher data input/output.
- Registers for Program Trace, Data Trace, Ownership Trace, and Watchpoint Trigger.
- All features are controllable and configurable via the JTAG port.
- Nexus Auxiliary port is supported on the 416BGA package.

Table 6. DRAM interface pin summary (continued)

Port pin[1]	Function	I/O direction	Pad type	PCR	RESET config[2]	Pin number
						416 TEPBGA
DDR_DQ[18]	DRAM Data Bus [18]	I/O	DDR	PCR[250]	None, None	E4
DDR_DQ[17]	DRAM Data Bus [17]	I/O	DDR	PCR[251]	None, None	E1
DDR_DQ[16]	DRAM Data Bus [16]	I/O	DDR	PCR[252]	None, None	F1
DDR_DQ[15]	DRAM Data Bus [15]	I/O	DDR	PCR[253]	None, None	G1
DDR_DQ[14]	DRAM Data Bus [14]	I/O	DDR	PCR[254]	None, None	G4
DDR_DQ[13]	DRAM Data Bus [13]	I/O	DDR	PCR[255]	None, None	H1
DDR_DQ[12]	DRAM Data Bus [12]	I/O	DDR	PCR[256]	None, None	H4
DDR_DQ[11]	DRAM Data Bus [11]	I/O	DDR	PCR[257]	None, None	J1
DDR_DQ[10]	DRAM Data Bus [10]	I/O	DDR	PCR[258]	None, None	K4
DDR_DQ[9]	DRAM Data Bus [9]	I/O	DDR	PCR[259]	None, None	K1
DDR_DQ[8]	DRAM Data Bus [8]	I/O	DDR	PCR[260]	None, None	L1
DDR_DQ[7]	DRAM Data Bus [7]	I/O	DDR	PCR[261]	None, None	L4
DDR_DQ[6]	DRAM Data Bus [6]	I/O	DDR	PCR[262]	None, None	M4
DDR_DQ[5]	DRAM Data Bus [5]	I/O	DDR	PCR[263]	None, None	M1
DDR_DQ[4]	DRAM Data Bus [4]	I/O	DDR	PCR[264]	None, None	N4
DDR_DQ[3]	DRAM Data Bus [3]	I/O	DDR	PCR[265]	None, None	N1
DDR_DQ[2]	DRAM Data Bus [2]	I/O	DDR	PCR[266]	None, None	P4
DDR_DQ[1]	DRAM Data Bus [1]	I/O	DDR	PCR[267]	None, None	P1
DDR_DQ[0]	DRAM Data Bus [0]	I/O	DDR	PCR[268]	None, None	R1
DRAM Data Strobes						
DDR_DQS[3]	DRAM Data Strobe [3]	I/O	DDR	PCR[232]	None, None	B3
DDR_DQS[2]	DRAM Data Strobe [2]	I/O	DDR	PCR[231]	None, None	G2
DDR_DQS[1]	DRAM Data Strobe [1]	I/O	DDR	PCR[230]	None, None	K2
DDR_DQS[0]	DRAM Data Strobe [0]	I/O	DDR	PCR[229]	None, None	N2
DRAM Data Enables						
DDR_DM[3]	DRAM Data Enable [3]	Output	DDR	PCR[236]	Output, None	B4
DDR_DM[2]	DRAM Data Enable [2]	Output	DDR	PCR[235]	Output, None	G3
DDR_DM[1]	DRAM Data Enable [1]	Output	DDR	PCR[234]	Output, None	K3
DDR_DM[0]	DRAM Data Enable [0]	Output	DDR	PCR[233]	Output, None	P3
DRAM Address						

Table 6. DRAM interface pin summary (continued)

Port pin[1]	Function	I/O direction	Pad type	PCR	RESET config[2]	Pin number
						416 TEPBGA
DDR_CAS	$\overline{\text{Column Address Strobe}}$	Output	DDR	PCR[221]	Output, None	B6
DDR_RAS	$\overline{\text{Row Address Strobe}}$	Output	DDR	PCR[227]	Output, None	B7
DDR_WEB	$\overline{\text{Write Enable}}$	Output	DDR	PCR[228]	Output, None	B9
DDR_ODT	DRAM On-die termination	Output	DDR	PCR[226]	Output, Pull Down	D5
DDR_CLK	DRAM Clock	Output	DDR	PCR[225]	Output, None	C7
DDR_CLKB	DRAM Clock bar	Output	DDR	NA	Output, None	D7
DDR_CK	DRAM Clock Enable	Output	DDR	PCR[222]	Output, Pull Down	D8
DDR_CS	DRAM Chip Select	Output	DDR	PCR[223]	Output, None	D9
MVREF	DDR Reference Voltage	Input	—	NA	—	J4
MVTT	DRAM Termination Voltage	Input	—	NA	—	F2,J2,M2,R2

1 These port pins are disabled and unpowered on packages where the DRAM interface is not bonded out.

2 Reset configuration is given as I/O direction and pull direction (for example, “Input, pullup”).

2.4.6 VIU muxing

The DCU3, DCULite and VIU2 modules share the same pins for input video. It is, however, possible to feed independent video streams to VIU2 and DCU3 (operating in narrow mode). Figure 5 explains the pin sharing arrangement.

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PA[8]	PCR[8]	Option 0 Option 1 Option 2 Option 3	GPIO[8] DCU_G0 SCL_2 eMIOS0[20]	RSDS4P	SIUL DCU3 I^2C_2 PWM/Timer	I/O	M / RSDS	None, none	126	150	G25
PA[9]	PCR[9]	Option 0 Option 1 Option 2 Option 3	GPIO[9] DCU_G1 SDA_2 eMIOS0[19]	RSDS4M	SIUL DCU3 I^2C_2 PWM/Timer	I/O	M / RSDS	None, none	127	151	G24
PA[10]	PCR[10]	Option 0 Option 1 Option 2 Option 3	GPIO[10] DCU_G2 — —	RSDS5P	SIUL DCU3 — —	I/O	M / RSDS	None, none	128	152	H23
PA[11]	PCR[11]	Option 0 Option 1 Option 2 Option 3	GPIO[11] DCU_G3 — —	RSDS5M	SIUL DCU3 — —	I/O	M / RSDS	None, none	129	153	G23
PA[12]	PCR[12]	Option 0 Option 1 Option 2 Option 3	GPIO[12] DCU_G4 — —	RSDS6P	SIUL DCU3 — —	I/O	M / RSDS	None, none	130	154	F26
PA[13]	PCR[13]	Option 0 Option 1 Option 2 Option 3	GPIO[13] DCU_G5 — —	RSDS6M	SIUL DCU3 — —	I/O	M / RSDS	None, none	131	155	F25
PA[14]	PCR[14]	Option 0 Option 1 Option 2 Option 3	GPIO[14] DCU_G6 — —	RSDS7P	SIUL DCU3 — —	I/O	M / RSDS	None, none	134	158	F24
PA[15]	PCR[15]	Option 0 Option 1 Option 2 Option 3	GPIO[15] DCU_G7 — —	RSDS7M	SIUL DCU3 — —	I/O	M / RSDS	None, none	135	159	F23
PORT B											
PB[0]	PCR[16]	Option 0 Option 1 Option 2 Option 3	GPIO[16] CANTX_0 TXD_0 —	—	SIUL FlexCAN_0 LINFlex_0 —	I/O	S	None, none	13	13	W4

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PC[13]	PCR[43]	Option 0 Option 1 Option 2 Option 3	GPIO[43] — MA2 CS0_1	ANS[13]	SIUL — ADC DSPI_1	I/O	J	None, None	71	87	AF25
PC[14]	PCR[44]	Option 0 Option 1 Option 2 Option 3	GPIO[44] — — —	ANS[14] EXTAL32	SIUL — — —	I/O	J	None, None	70	86	AF24
PC[15]	PCR[45]	Option 0 Option 1 Option 2 Option 3	GPIO[45] — — —	ANS[15] XTAL32	SIUL — — —	I/O	J	None, None	69	85	AF23
PORT D											
PD[0]	PCR[46]	Option 0 Option 1 Option 2 Option 3	GPIO[46] M0C0M SSD0_0 eMIOS1[8]	—	SIUL SMD SSD PWM/Timer	I/O	SMD	None, None	90	106	AB26
PD[1]	PCR[47]	Option 0 Option 1 Option 2 Option 3	GPIO[47] M0C0P SSD0_1 eMIOS1[16]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	91	107	AB25
PD[2]	PCR[48]	Option 0 Option 1 Option 2 Option 3	GPIO[48] M0C1M SSD0_2 eMIOS1[23]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	92	108	AB24
PD[3]	PCR[49]	Option 0 Option 1 Option 2 Option 3	GPIO[49] M0C1P SSD0_3 eMIOS0[9]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	93	109	AB23
PD[4]	PCR[50]	Option 0 Option 1 Option 2 Option 3	GPIO[50] M1C0M SSD1_0 eMIOS0[8]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	96	112	AA26
PD[5]	PCR[51]	Option 0 Option 1 Option 2 Option 3	GPIO[51] M1C0P SSD1_1 eMIOS0[16]	—	SIUL SMC SSD PWM/Timer	I/O	SMD	None, None	97	113	AA23

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PP[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PP[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PP[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PP[15]	—	—	Reserved	—	—	—	—	—	—	—	—

1 Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIUL module.
PCR[PA] = 00 selects Option 0
PCR[PA] = 01 selects Option 1
PCR[PA] = 10 selects Option 2
PCR[PA] = 11 selects Option 3
This is intended to select the output functions. To use one of the input functions, the PCR[IBE] bit must be written to '1', regardless of the values selected in the PCR[PA] bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2 Special functions are enabled independently from the standard digital pin functions. Enabling standard I/O functions in the PCR registers may interfere with their functionality. ADC functions are enabled using the PCR[APC] bit; other functions are enabled by enabling the respective module.

3 Using the PSMI registers in the System Integration Unit Lite (SIUL), different pads can be multiplexed to the same peripheral input. Please see the SIUL chapter of the *MPC5645S Microcontroller Reference Manual* for details.

4 See the "Pad types" table for an explanation of the letters in this column.

5 Reset configuration is given as I/O direction and pull, e.g., "Input, pullup".

6 Out of reset pins PH[0:3] are available as JTAG pins (TCK, TDI, TDO and TMS respectively). It is up to the user to configure pins PH[0:3] when needed.

The location of TCON[0:3] pins is mentioned in the following table.

Table 8. Location of TCON[0:3] Pins

Function	Port Name	PCR	Ball Number
DCU_TAG / TCON0	PK11	PCR[132]	Ball No: AC09
DCU_TAG / TCON0	PJ12	PCR[117]	Ball No: A23
DCU_HSYNC/TCON1	PG9	PCR[95]	Ball No: T02
DCU_VSYNC / TCON2	PG8	PCR[94]	Ball No: T04
DCU_DE / TCON3	PG10	PCR[96]	Ball No: T01
DCU_TAG/TCON3	PM5	PCR[152]	NC (only on 176)

Table 21. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit	SpecID
					Min	Typ	Max		
V_{PORH}	CC	C	Power-on reset threshold	—	1.5	—	2.7	V	D5.11
$V_{LVDHV3H}$	CC	C	LVDHV3 low voltage detector high threshold	—	—	—	2.9		D5.12
$V_{LVDHV3L}$	CC	C	LVDHV3 low voltage detector low threshold	—	2.5	—	—		D5.13
$V_{LVDHV5H}$	CC	C	LVDHV5 low voltage detector high threshold	—	—	—	4.4		D5.14
$V_{LVDHV5L}$	CC	C	LVDHV5 low voltage detector low threshold	—	3.9	—	—		D5.15
$V_{LVDLVCORH}$	CC	C	LVDLVCOR low voltage detector high threshold	T_A = 25°C, after trimming	—	—	1.185		D5.16
$V_{LVDLVCORL}$	CC	C	LVDLVCOR low voltage detector low threshold		1.095	—	—		D5.17

1 V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = -40 / +105°C, unless otherwise specified

2 All values need to be confirmed during device validation.

4.7.3 Low voltage domain power consumption

Table 22 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 22. DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—	—	—	295	375[3]	mA
I_{DDRUN}[4]	CC	P	RUN mode typical average current[5]	f_{CPU} = 125MHz, Dual Display Drive with external DRAM, 416 TEPBGA package option only	—	—	275	—	mA
				f_{CPU} = 125MHz, Single Display Drive, no external DRAM, 176 LQFP / 208 LQFP package options	—	—	240	—	
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128KHz) running	T_A = 25 °C	—	17.5	23.5	mA
		P			T_A = 105 °C	—	35	45.5	
I_{DDSTOP}	CC	D	STOP mode current[7] [8]	Slow internal RC oscillator (128KHz) running	T_A = –40°C	—	645	—	µA
		D			T_A = 0°C	—	1100	—	
		P			T_A = 25°C	—	1531	5500	
		D			T_A = 55°C	—	3.8	—	mA
		D			T_A = 85°C	—	9.7	—	
		C			T_A = 105°C	—	17.67	36.5	

4.8.2 DC specification for CMOS090LP2fg library @ VDDE = 5.0 V

NOTE

These pad specifications are applicable for pads in the Analog segment Only. See the "GPIO power bank supplies and functionality" table in the "Voltage Regulators and Power Supplies" chapter of the reference manual for details.

Table 26. DC electrical specifications

Symbol		C	Parameter	Condition	Value		Unit	SpecID
					Min	Max		
Vdd	SR	P	Core supply voltage	—	1.08	1.32	V	D9.17
Vdde	SR	P	I/O supply voltage	—	4.5	5.5	V	D9.18
Vdd33	SR	P	I/O pre-driver supply voltage	—	3.0	3.6	V	D9.19
Vih_hys	SR	P	CMOS input buffer high voltage	With hysteresis enabled	0.65×Vdde	Vdde+0.3	V	D9.20
Vil_hys	SR	P	CMOS input buffer low voltage	With hysteresis enabled	Vss–0.3	0.35×Vdde	V	D9.21
Vih	SR	P	CMOS input buffer high voltage	With hysteresis disabled	0.55×Vdde	Vdde+0.3	V	D9.22
Vil	SR	P	CMOS input buffer low voltage	With hysteresis disabled	Vss–0.3	0.40×Vdde	V	D9.23
Vhys	SR	T	CMOS input buffer hysteresis	—	0.1×Vdde	—	V	D9.24
Pull_Ioh	SR	P	Weak pullup current	—	35	135	µA	D9.25
Pull_Iol	SR	P	Weak pulldown current	—	35	200	µA	D9.26
Iinact_d	SR	P	Digital pad input leakage current	Weak pull inactive	–2.5	2.5	µA	D9.27
Iinact_a	SR	P	Analog pad input leakage current	Weak pull inactive	–150	150	nA	D9.28
Voh	SR	P	Slew rate controlled output high voltage	—	0.8×Vdde	—	V	D9.29
Vol	SR	P	Slew rate controlled output low voltage	—	—	0.2×Vdde	V	D9.30
Voh_ls	SR	C	Low swing output pad output high voltage	—	2.64	—	V	D9.31
Ioh_msr	SR	C	pad_msr_hv Ioh	—	11.6	40.7	mA	D9.32
Iol_msr	SR	C	pad_msr_hv Iol	—	17.7	68.2	mA	D9.33
Ioh_ssr	SR	C	pad_ssr_hv Ioh	—	6.0	21.3	mA	D9.34
Iol_ssr	SR	C	pad_ssr_hv Iol	—	9.2	36.3	mA	D9.35
Rtgate	SR	D	Pad_tgate_hv input resistance	—	250	800	Ω	D9.39

Table 38. SMD pad electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{PU}	CC	P	Internal pull-up device current	$V_{in}=V_{IL}$	–130	—	—	µA
				$V_{in}=V_{IH}$	—	—	0	
I_{PD}	CC	P	Internal pull-down device current	$V_{in}=V_{IL}$	0	—	—	
				$V_{in}=V_{IH}$	—	—	130	
I_{IN}	CC	P	Input leakage current	—	–1	—	1	
R_{DSONH}	CC	C	SMD pad driver active high impedance	$I_{OH} \leq -30$ mA[2]	—	—	16	Ω
R_{DSONL}	CC	C	SMD pad driver active low impedance	$I_{OL} \leq 30$ mA[2]	—	—	16	Ω
V_{OMATCH}	CC	C	Output driver matching V_{OH} / V_{OL}	I_{OH} / $I_{OL} \leq 30$ mA[2]	—	—	90	mV

1 VDD = 5.0 V ±10%, Tj = –40 to +140 °C.

2 VDD = 5.0 V ±10%, Tj = –40 to +120 °C.

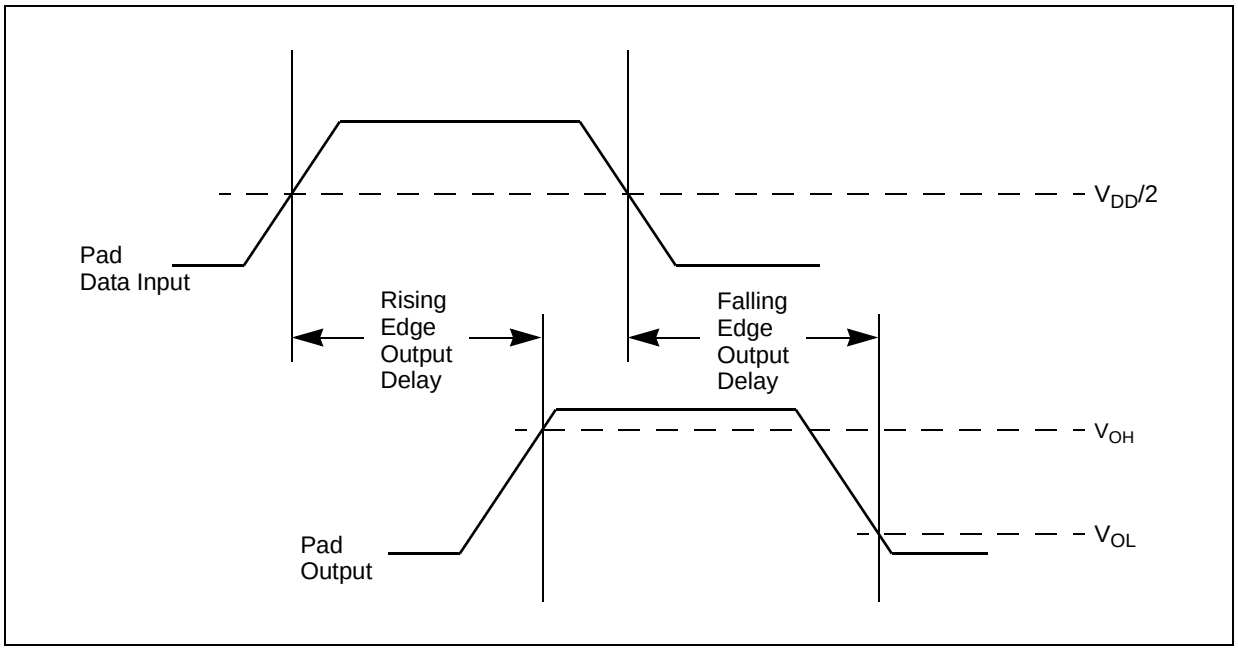

Figure 7. Pad output delay

Table 51. Functional pad type AC specifications (continued)

Name	C	Prop. delay (ns) L>H / H>L[1]		Rise/fall edge (ns)		Drive load (pF)	Drive/slew rate select
		Min	Max	Min	Max		MSB, LSB
pad_ssr_hv[2]	C	7.3 / 5.7	19 / 18	4.4 / 4.3	10 / 11	50	11[3]
		24 / 19	58 / 58	17 / 15	40 / 42	200	
		N/A					10[4]
		26 / 27	61 / 69	13 / 13	30 / 34	50	01
		49 / 45	115 / 115	27 / 23	61 / 61	200	
		137 / 142	320 / 330	72 / 74	156 / 164	50	00
		182 / 172	420 / 420	90 / 85	200 / 200	200	
pad_i_hv	C	0.5 / 0.5	1.9 / 1.9	0.3 / 0.3	1.5 / 1.5	0.5	N/A

1 L>H signifies low-to-high propagation delay and H>L signifies high-to-low propagation delay.

2 For input buffer timing, look at pad_i_hv.

3 Can be used on the tester.

4 This drive select value is not supported. If selected, it will be approximately equal to 11.

4.18.3 AC specification for CMOS090LP2fg library @ VDDE = 3.3 V

Table 52. Functional pad AC type specifications

Name	Prop. delay (ns) L>H / H>L		Rise/fall edge (ns)		Drive load (pF)	Drive/slew rate select
	Min	Max	Min	Max		MSB, LSB
pad_msr_hv	5.8 / 4.4	18 / 17	2.7 / 2.1	7.6 / 8.5	50	11
	16 / 13	46 / 49	11.2 / 8.6	30 / 34	200	
	N/A					10
	14 / 16	37 / 45	6.5 / 6.7	15.5 / 19	50	01
	27 / 27	69 / 82	15 / 13	38 / 43	200	
	83 / 86	200 / 210	38 / 38	86 / 86	50	00
	113 / 109	270 / 285	53 / 46	120 / 120	200	

Table 63. SDR Timings

—	Symbol	C	Parameter	Min	Max	Units
DD1	t_{QVS}	C	Data output Valid (Write transaction)	—	(0.5 x t_{SDCK}) + 1.5	ns
DD1.1	t_{QS}	C	Data output setup (t_{DSK} - DD1)[1]	2.5	—	ns
DD2	t_{QH}	C	Data output Hold (Write transaction)	2.0	—	ns
DD3	t_{IS}	C	Data Input Setup (Read transaction)	—	2.0	ns
DD4	t_{IH}	C	Data input Hold (Read transaction)	—	2.0	ns

1 This is alternate representation for DD1 for better clarity.

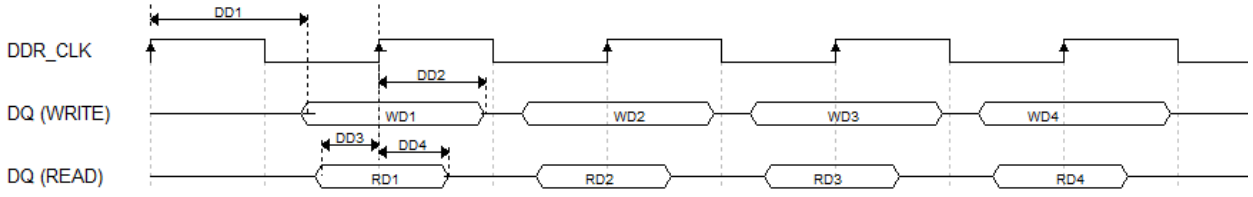

Figure 31. SDR Read and Write Timings

4.19.5.2 2.5 V DDR1

Table 64. SSTL_2 Class II 2.5 V DDR DC Specifications

Symbol	C	Parameter	Condition	Min	Nom	Max	Units	Notes	SpecID
vddet	P	I/O Supply Voltage	—	2.30	2.50	2.70	V	JESD8-9B	A5.1
vdd	P	Core Supply Voltage	—	1.08	1.20	1.32	V	—	A5.2
Vref(dc)	P	Input Reference Voltage	—	1.13	1.25	1.38	V	JESD8-9B	A5.3
Vtt	P	Termination Voltage	—	Vref-0.04	vref	Vref+0.04	V	JESD8-9B	A5.4
$V_{ih(dc)}$	C	DC Input Logic High	—	Vref+0.15	—	vddet+0.3	V	JESD8-9B	A5.5
$V_{il(dc)}$	C	DC Input Logic Low	—	-0.3	—	Vref-0.15	V	JESD8-9B	A5.6
$V_{ih(ac)}$	C	AC Input Logic High	—	Vref+0.31	—	—	V	JESD8-9B	A5.7
$V_{il(ac)}$	C	AC Input Logic Low	—	—	—	Vref-0.31	V	JESD8-9B	A5.8
I_{in}	P	Pad input Leakage Current	—	—	—	+/-10	µA	—	A5.9

4.19.9 FlexCAN timing

The CAN functions are available as TX pins at normal IO pads and as RX pins at the always on domain. There is no filter for the wakeup dominant pulse. Any high-to-low edge can cause wakeup if configured.

Table 70. FlexCAN timing[1]

Num	Symbol		C	Characteristic	Min. value	Max. value	Unit	SpecID
1	t_{CANOV}	CC[2]	D	CTNX Output Valid after CLKOUT Rising Edge (Output Delay)	—	22.48	ns	A10.1
2	t_{CANSU}	CC[2]	D	CNRX Input Valid to CLKOUT Rising Edge (Setup Time)	—	12.46	ns	A10.2

1 FlexCAN timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = -40 to 105 °C, and CL = 50 pF with SRC = 0b00.

2 Parameter values guaranteed by design.

4.19.10 Deserial Serial Peripheral Interface (DSPI)

Table 71. DSPI Timing[1]

Num	Symbol		C	Characteristic	Min	Max	Unit	SpecID
1	t_{SCK}	CC[2]	D	SCK Cycle TIme[3,4]	60[5]	—	ns	A11.1
2	t_{CSC}	CC[2]	D	PCS to SCK Delay[6]	-	—	ns	A11.2
3	t_{ASC}	CC[2]	D	After SCK Delay[7]	20	—	ns	A11.3
4	t_{SDC}	CC[2]	D	SCK Duty Cycle	$t_{SCK}/2$ –2ns	$t_{SCK}/2$ + 2ns	ns	A11.4
5	t_A	CC[2]	D	Slave Access Time (PCSx active to SOUT driven)	—	25	ns	A11.5
6	t_{DIS}	CC[2]	D	Slave SOUT Disable Time (PCSx inactive to SOUT High-Z or invalid)	—	25	ns	A11.6
7	t_{SUI}	CC[2]	D	Data Setup Time for Inputs				A11.7
				Master (MTFE = 0)	20	—	ns	
				Slave	10	—	ns	
				Master (MTFE = 1, CPHA = 0)[8]	5	—	ns	
				Master (MTFE = 1, CPHA = 1)	35	—	ns	
8	t_{HI}	CC[2]	D	Data Hold Time for Inputs				A11.8
				Master (MTFE = 0)	–4	—	ns	
				Slave	10	—	ns	
				Master (MTFE = 1, CPHA = 0)[8]	26	—	ns	
				Master (MTFE = 1, CPHA = 1)	–4	—	ns	
9	t_{SUO}	CC[2]	D	Data Valid (after SCK edge)				A11.9
				Master (MTFE = 0)	—	15	ns	
				Slave	—	20	ns	
				Master (MTFE = 1, CPHA=0)	—	30	ns	
				Master (MTFE = 1, CPHA=1)	—	15	ns	
10	t_{HO}	CC[2]	D	Data Hold Time for Outputs				A11.10
				Master (MTFE = 0)	–15	—	ns	
				Slave	5.5	—	ns	
				Master (MTFE = 1, CPHA = 0)	0	—	ns	
				Master (MTFE = 1, CPHA = 1)	–15	—	ns	

1 DSPI timing specified at VDDE_x = 3.0 V to 3.6 V, T_A = -40 to 105 °C, and CL = 50 pF with SRC = 0b10.

2 Parameter values guaranteed by design.

3 The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate.

4 The actual minimum SCK Cycle Time is limited by pad performance.

5 Maximum clock possible is System clock/2.

6 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK], program PSSCK=2 & CSSCK = 2.

7 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

8 This delay value is corresponding to SMPL_PT=00b which is bit field 9 and 8 of DSPI_MCR register.

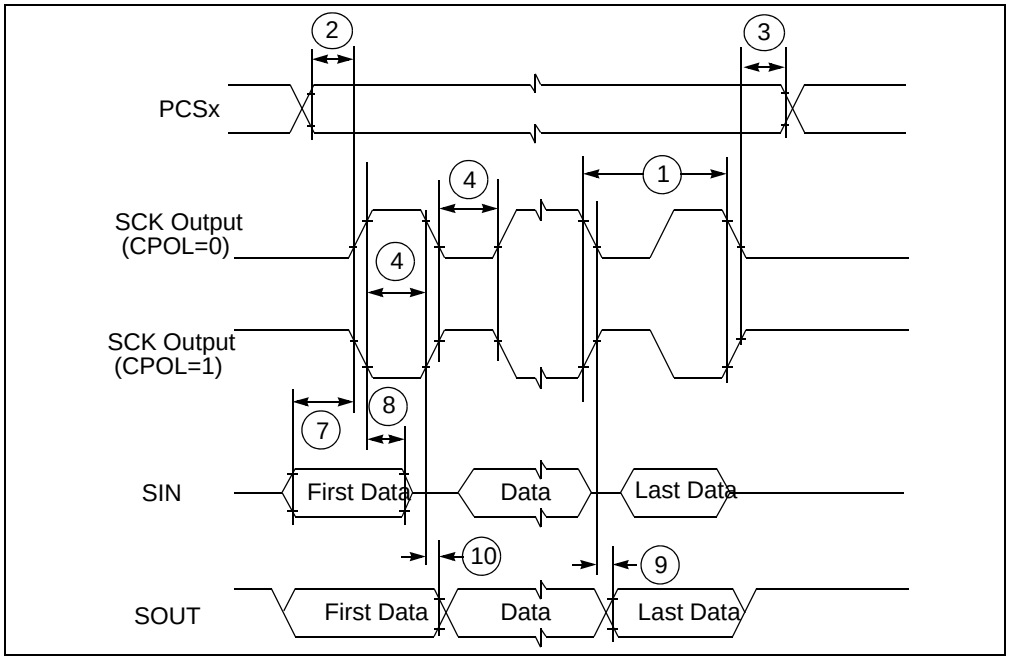

Figure 36. DSPI Classic SPI Timing — Master, CPHA = 0

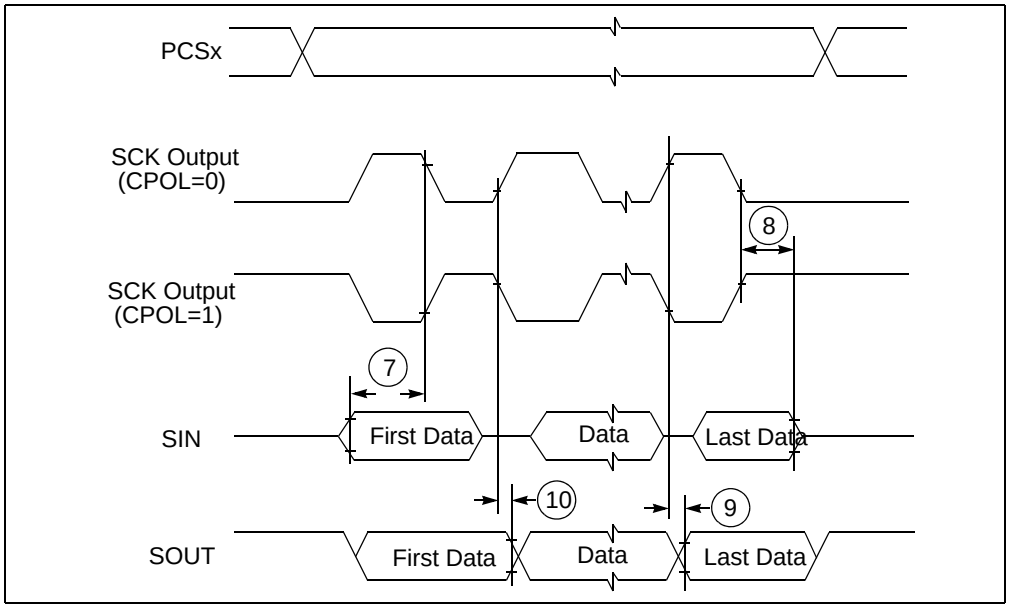

Figure 37. DSPI Classic SPI Timing — Master, CPHA = 1

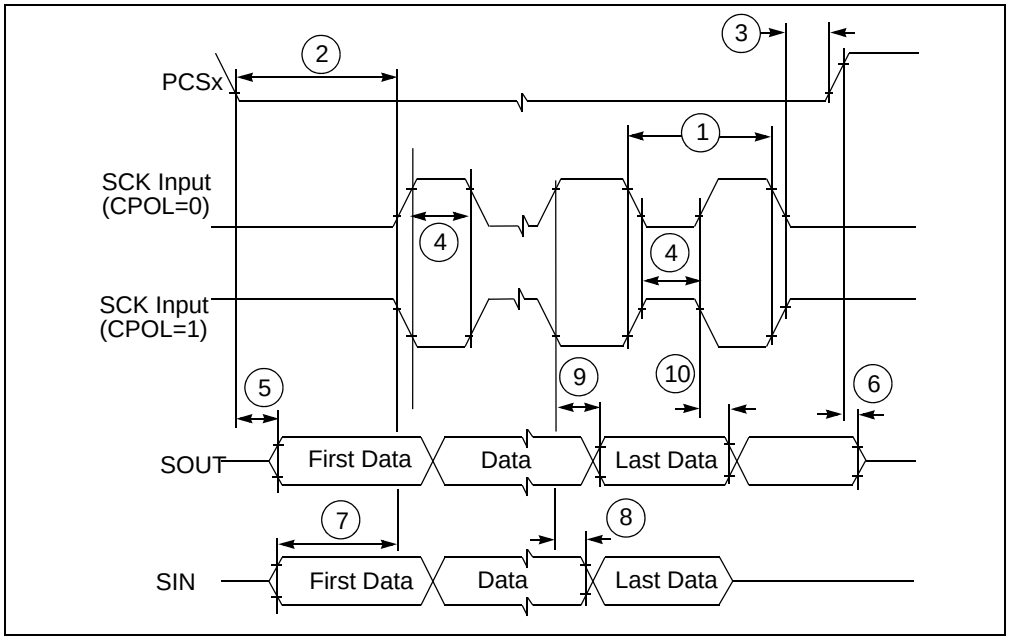

Figure 42. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

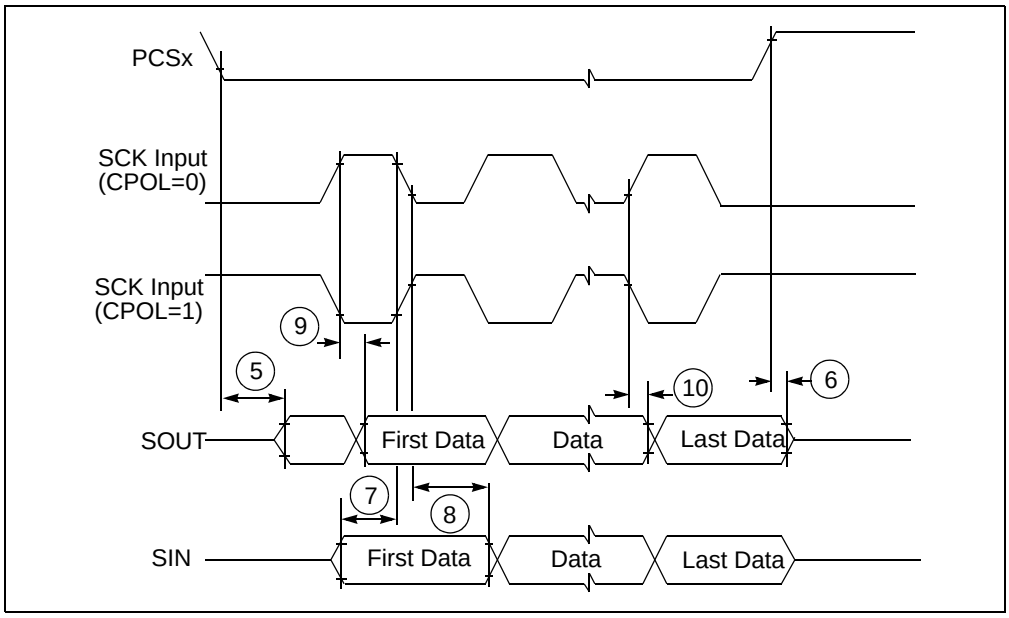

Figure 43. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

Table 78. Revision history (continued)

Revision (Date)	Description
4 (continued) (24 Jun 2010)	In the 208-pin pinout: • For pin 68, changed eMIOSA23 to eMIOS0[23]. • For pin 69, changed eMIOSA16 to eMIOS0[16]. • For pin 70, changed eMIOSA15 to eMIOS0[15]. • For pin 71, changed eMIOSA14 to eMIOS0[14]. In the 324-pin pinout: • Added content to indicate which functions are available only in this package. • Renamed pin J10 (was VSS_DR, is VSS). In the “Voltage supply pin descriptions” table: • Deleted the entry for VSS_DR. • Added pin J10 to the VSS group in the 324-pin package. Revised the “Nexus pins” table. In the “Recommended operating conditions (3.3 V)” table, changed the specification for TV_{DD} (was 0.25 V/µs, is 12 V/ms). In the “Recommended operating conditions (5.0 V)” table, changed the specification for TV_{DD} (was 0.25 V/µs, is 12 V/ms). In the “FMPLL electrical characteristics” table, changed footnote 6 (was “f_{CPU} 64 MHz can be achieved only at up to 105 °C”, is “f_{CPU} of 125 MHz can be achieved only at temperatures up to 105 °C with a maximum FM depth of 2%.”.) In the “DC specification for CMOS090LP2 library @ VDDE = 3.3 V” > “DC electrical specifications” table, deleted the specifications for Vih_pci and Vil_pci. Revised the “Low power oscillator electrical characteristics” table. In the “ADC electrical characteristics” table, changed “V_{DD}-0.1” to “V_{DDE_A}–0.1” and “V_{DD}+0.1” to “V_{DDE_A}+0.1”. Renamed “QuadSPI2 Timing” to “QuadSPI timing” and added meaningful content. Added the “TCON/RSDS timing” section.
5 (25 Feb 2011)	In the “Feature List” section: • Changed RTC optional clocking from “main“ to “fast“ 4-16 MHz external oscillator. • Changed CMU monitor feature from “main crystal oscillator“ to “fast (4–16 MHz) external crystal oscillator”. In the “Feature details“ section, changed “main oscillator“ to “external oscillator“ in the “System clocks and clock generation modules“ section. In the “Pad configuration during reset phases“ section, changed “Main oscillator pads” to “Fast (4-16 MHz oscillator pads“. In the ““Voltage supply pin descriptions” table, changed V_{DD_DR} function from “DDR SDRAM interface supply“ to “1.8V, 2.5V, and 3.3V SDRAM supply“ In the “System pin descriptions” table, specified an external capacitor value of 47pF in the footnote. In the “Functional ports” section, added list of pad types. In the “Power-up sequencing” section: • Added list item that specifies VDDE_B and VDD33_DR are to be powered up first. • Added VDD33_DR to the list of generic I/O or noise-free supplies. • Added details to VREG HV list item. • Changed post-list text regarding DDR to be a separate NOTE, and identified the 3.3V supply as VDD33_DR. • Added power-up information to the LV supply (VDD12) list item. • Added “Parameter classification” section and accompanying table. Added “C” classification column and values to tables throughout the “Electrical characteristics“ section.