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Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12kg128mfue

Chapter 17
Interrupt (INTV1) Block Description

Chapter 18
Multiplexed External Bus Interface (MEBIV3)

Table 2-3. Detailed Flash Memory Map Summary

MCU Address Range	PPAGE	Protectable Lower Range	Protectable Higher Range	Block Relative Address[1]
0x4000-0x7FFF	Unpaged (0x3E)	0x4000-0x43FF 0x4000-0x47FF 0x4000-0x4FFF 0x4000-0x5FFF	N.A.	0x18000-0x1BFFF
0x8000-0xBFFF	0x38	N.A.	N.A.	0x00000-0x03FFF
	0x39	N.A.	N.A.	0x04000-0x07FFF
	0x3A	N.A.	N.A.	0x08000-0x0BFFF
	0x3B	N.A.	N.A.	0x0C000-0x0FFFF
	0x3C	N.A.	N.A.	0x10000-0x13FFF
	0x3D	N.A.	N.A.	0x14000-0x17FFF
	0x3E	0x8000-0x83FF 0x8000-0x87FF 0x8000-0x8FFF 0x8000-0x9FFF	N.A.	0x18000-0x1BFFF
	0x3F	N.A.	0xB800-0xBFFF 0xB000-0xBFFF 0xA000-0xBFFF 0x8000-0xBFFF	0x1C000-0x1FFFF
0xC000-0xFFFF	Unpaged (0x3F)	N.A.	0xF800-0xFFFF 0xF000-0xFFFF 0xE000-0xFFFF 0xC000-0xFFFF	0x1C000-0x1FFFF

1 Block Relative Address for 128 Kbyte Flash block consists of 17 address bits.

The Flash module also contains a set of 16 control and status registers located in address space module base + 0x0000 to module base + 0x000F. A summary of these registers is given in Table 2-4 while their accessibility in normal and special modes is detailed in Section 2.3.2, “Register Descriptions”.

Table 2-4. Flash Register Map

MODULE BASE +	Use	Normal Mode Access
0x0000	Flash Clock Divider Register (FCLKDIV)	R/W
0x0001	Flash Security Register (FSEC)	R
0x0002	Flash Test Mode Register (FTSTMOD)	R/W
0x0003	Flash Configuration Register (FCNFG)	R/W
0x0004	Flash Protection Register (FPROT)	R/W

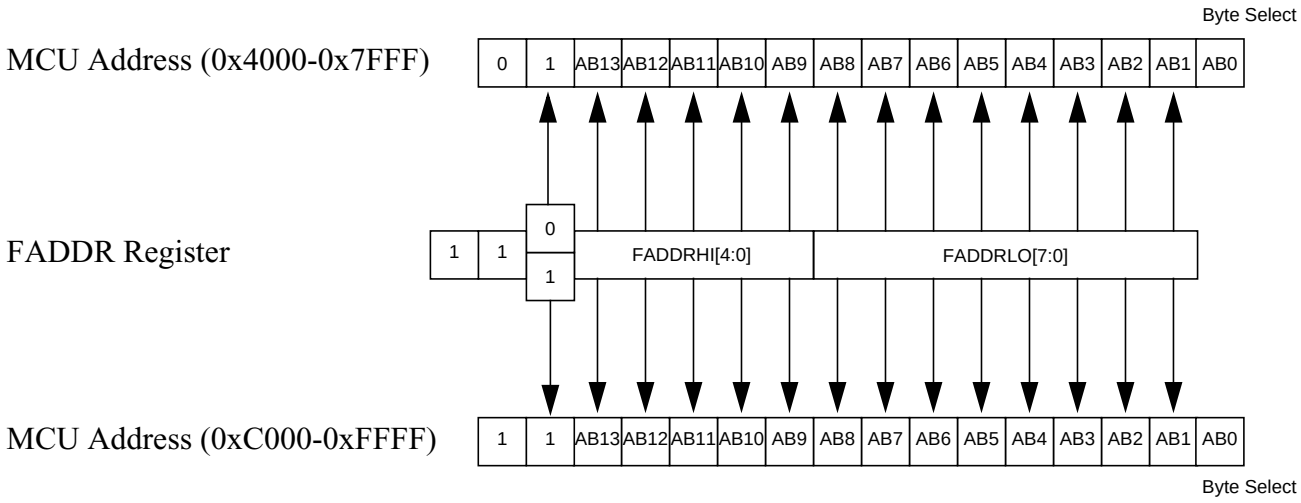

Figure 2-16. FADDR to MCU Address Mapping (Unpaged)

2.3.2.11 Flash Data Registers (FDATA)

The FDATAHI and FDATALO registers are the Flash data registers.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	FDATAHI							
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-17. Flash Data High Register (FDATAHI)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R	FDATALO							
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-18. Flash Data Low Register (FDATALO)

All FDATAHI and FDATALO bits are readable but are not writable. After an array write as part of a command write sequence, the FDATA registers will contain the data written. At the completion of a data compress operation, the resulting 16-bit signature is stored in the FDATA registers. The data compression signature is readable in the FDATA registers until a new command write sequence is started or a double bit fault is detected in a Flash array read operation. If a double bit fault is detected during a Flash array read, erase verify or data compress operation, the parity bits stored in the Flash array at the failed location will

2.4.1.3.1 Erase Verify Command

The erase verify operation is used to confirm that a Flash block is erased. After launching the erase verify command, the CCIF flag in the FSTAT register will set after the operation has completed unless a second command has been buffered. The number of bus cycles required to execute the erase verify operation is equal to the number of addresses in the Flash block plus 12 bus cycles as measured from the time the CBEIF flag is cleared until the CCIF flag is set. The result of the erase verify operation is reflected in the state of the BLANK flag in the FSTAT register. If the BLANK flag is set in the FSTAT register, the Flash memory is erased.

If the ECC logic detects a double bit fault during the erase verify operation, the operation will terminate immediately and set the DFDIF and ACCERR flags in the FSTAT register. The faulty address will be stored in the FADDR registers and the ECC parity bits read at the faulty address will be stored in the FDATALO register. The CCIF flag will set after the DFDIF flag is set and the faulty information is stored in the FADDR and FDATALO registers.

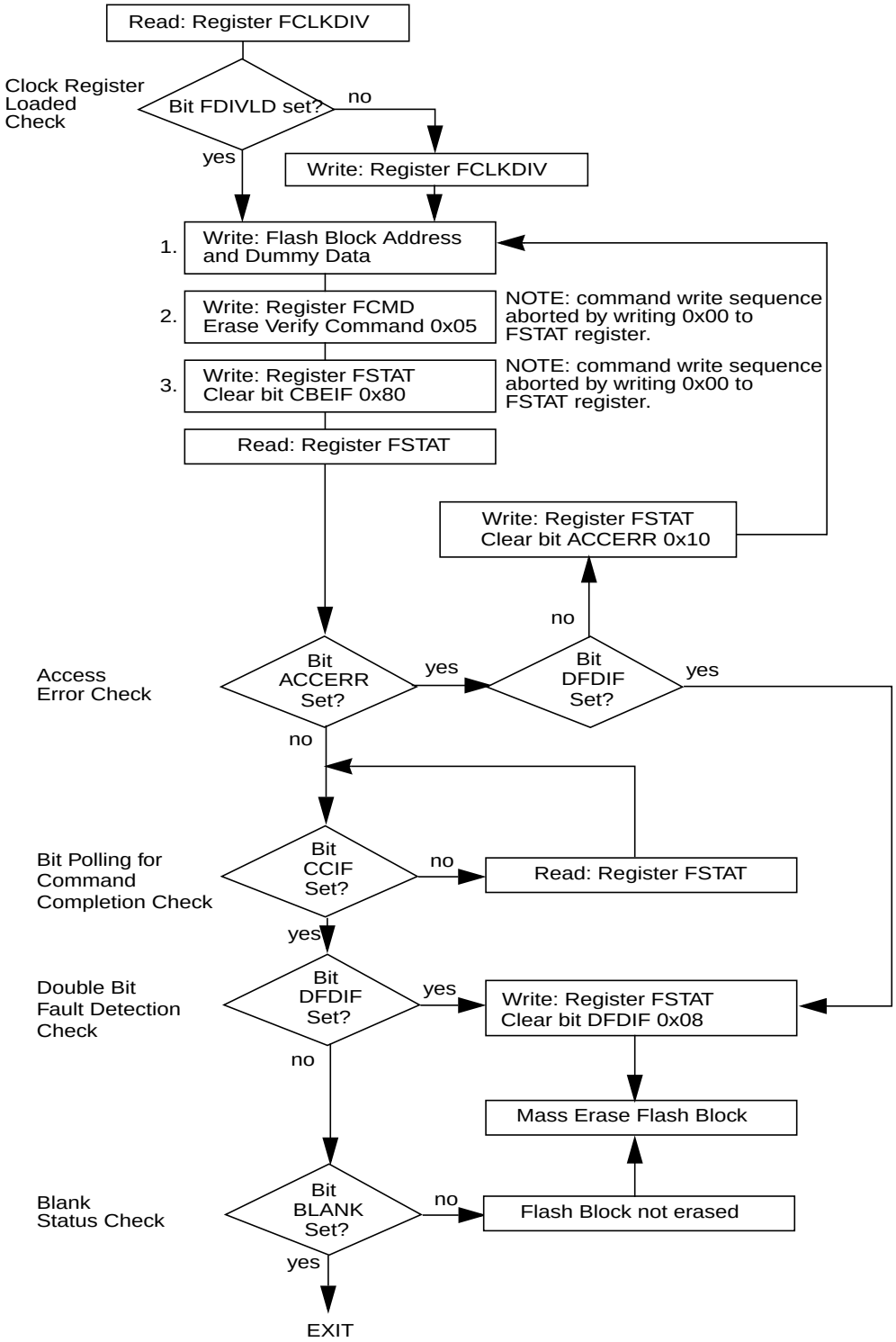

Figure 2-24. Example Erase Verify Command Flow

2.4.1.3.2 Data Compress Command

The data compress command is used to check Flash code integrity by compressing data from a selected portion of the Flash block into a signature analyzer. The starting address for the data compress operation is defined by the address written during the command write sequence. The number of consecutive word addresses compressed is defined by the data written during the command write sequence. The number of words that can be compressed in a single data compress operation ranges from 1 to 16,384. After launching the data compress command, the CCIF flag in the FSTAT register will set after the data compress operation has completed. The number of bus cycles required to execute the data compress operation is equal to two times the number of addresses read plus 20 bus cycles as measured from the time the CBEIF flag is cleared until the CCIF flag is set. After the CCIF flag is set, the signature generated by the data compress operation is available in the FDATA register. The signature in the FDATA register can be compared to the expected signature to determine the integrity of the selected data stored in the Flash block. If the last address of the Flash block is reached during the data compress operation, data compression will continue with the starting address of the Flash block.

NOTE

Since the FDATA register (or data buffer) is written to as part of the data compress operation, a command write sequence is not allowed to be buffered behind a data compress command write sequence. The CBEIF flag will not set after launching the data compress command to indicate that a command must not be buffered behind it. If an attempt is made to start a new command write sequence with a data compress operation active, the ACCERR flag in the FSTAT register will be set. A new command write sequence must only be started after reading the signature stored in the FDATA register. A Flash array read that generates a double bit fault will overwrite the contents of the FDATA register.

In order to take corrective action, it is recommended that the data compress command be executed on a Flash sector or subset of a Flash sector. If the data compress operation on a Flash sector returns an invalid signature, the Flash sector should be erased using the sector erase command and then reprogrammed using the program command.

NOTE

During the data compress operation, the Flash array is read with a sense-amp margin setting that is different from the normal array read setting. Therefore, if the data compress operation returns an invalid signature, the section of the Flash array compressed may still be functional. The failing section of the Flash array could be validated using normal array read operations.

The data compress command can be used to verify that a sector or sequential set of sectors are erased.

If the ECC logic detects a double bit fault during the data compress operation, the operation will terminate immediately and set the DFDIF and ACCERR flags in the FSTAT register. The faulty address will be stored in the FADDR registers and the ECC parity bits read at the faulty address will be stored in the FDATALO register. The CCIF flag will set after the DFDIF flag is set and the faulty information is stored in the FADDR and FDATALO registers.

If a double bit fault is detected during array reads as part of the reset sequence, the ACCERR flag will set in the FSTAT register.

2.7.2 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector / block being erased is not guaranteed.

2.8 Interrupts

The Flash module can generate an interrupt when all Flash command operations have completed, when the Flash address, data, and command buffers are empty, or when a Flash array read or operation has detected a double bit fault.

Table 2-21. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Address, Data and Command Buffers empty	CBEIF (FSTAT register)	CBEIE (FCNFG register)	I-Bit
All Flash commands completed	CCIF (FSTAT register)	CCIE (FCNFG register)	I-Bit
Flash array read or verify operation detected a double bit fault	DFDIF (FSTAT register)	DFDIE (FCNFG register)	I-Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

2.8.1 Description of Flash Interrupt Operation

The logic used for generating interrupts is shown in Figure 2-31.

The Flash module uses the CBEIF and CCIF flags in combination with the CBIE and CCIE enable bits to generate the Flash command interrupt request. The Flash module uses the DFDIF flag in combination with the DFDIE enable bit to generate the Flash double fault detect interrupt request.

4.4.3 Data Direction Register

The Data Direction Register defines whether the pin is used as an input or an output. A Data Direction Register bit set to 0 configures the pin as an input. A Data Direction Register bit set to 0 configures the pin as an output. If a peripheral module controls the pin the contents of the data direction register is ignored (Figure 4-47).

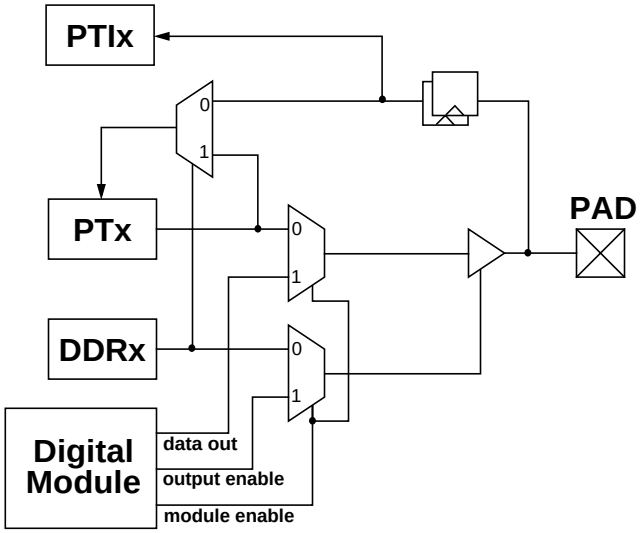

Figure 4-47. Illustration of I/O Pin Functionality

Figure 4-48 shows the state of digital inputs and outputs when an analog module drives the port. When the analog module is enabled all associated digital output ports are disabled and all associated digital input ports read “1”.

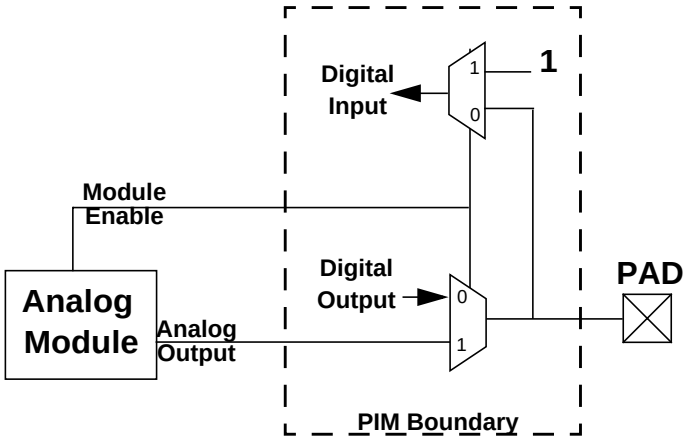

Figure 4-48. Digital Ports and Analog Module

4.4.4 Reduced Drive Register

If the port is used as an output the Reduced Drive Register allows the configuration of the drive strength.

Table 5-5. PLLCTL Field Descriptions (continued)

Field	Description
5 AUTO	**Automatic Bandwidth Control Bit** — AUTO selects either the high bandwidth (acquisition) mode or the low bandwidth (tracking) mode depending on how close to the desired frequency the VCO is running. Write anytime except when PLLWAI=1, because PLLWAI sets the AUTO bit to 1. 0 Automatic mode control is disabled and the PLL is under software control, using ACQ bit. 1 Automatic mode control is enabled and ACQ bit has no effect.
4 ACQ	**Acquisition Bit** — Write anytime. If AUTO=1 this bit has no effect. 0 Low bandwidth filter is selected. 1 High bandwidth filter is selected.
2 PRE	**RTI Enable during Pseudo-Stop Bit** — PRE enables the RTI during pseudo-stop mode. Write anytime. 0 RTI stops running during pseudo-stop mode. 1 RTI continues running during pseudo-stop mode. **Note:** If the PRE bit is cleared the RTI dividers will go static while pseudo-stop mode is active. The RTI dividers will not initialize like in wait mode with RTIWAI bit set.
1 PCE	**COP Enable during Pseudo-Stop Bit** — PCE enables the COP during pseudo-stop mode. Write anytime. 0 COP stops running during pseudo-stop mode 1 COP continues running during pseudo-stop mode **Note:** If the PCE bit is cleared the COP dividers will go static while pseudo-stop mode is active. The COP dividers will *not* initialize like in wait mode with COPWAI bit set.
0 SCME	**Self-Clock Mode Enable Bit** — Normal modes: Write once —Special modes: Write anytime — SCME can not be cleared while operating in self-clock mode (SCM=1). 0 Detection of crystal clock failure causes clock monitor reset (see Section 5.5.1, “Clock Monitor Reset”). 1 Detection of crystal clock failure forces the MCU in self-clock mode (see Section 5.4.7.2, “Self-Clock Mode”).

5.3.2.8 CRG RTI Control Register (RTICTL)

This register selects the timeout period for the real-time interrupt.

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-11. CRG RTI Control Register (RTICTL)

Read: anytime

Write: anytime

NOTE

A write to this register initializes the RTI counter.

5.6 Interrupts

The interrupts/reset vectors requested by the CRG are listed in Table 5-15. Refer to the device overview chapter for related vector addresses and priorities.

Table 5-15. CRG Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Real-time interrupt	I bit	CRGINT (RTIE)
LOCK interrupt	I bit	CRGINT (LOCKIE)
SCM interrupt	I bit	CRGINT (SCMIE)

5.6.1 Real-Time Interrupt

The CRGV4 generates a real-time interrupt when the selected interrupt time period elapses. RTI interrupts are locally disabled by setting the RTIE bit to 0. The real-time interrupt flag (RTIF) is set to 1 when a timeout occurs, and is cleared to 0 by writing a 1 to the RTIF bit.

The RTI continues to run during pseudo-stop mode if the PRE bit is set to 1. This feature can be used for periodic wakeup from pseudo-stop if the RTI interrupt is enabled.

5.6.2 PLL Lock Interrupt

The CRGV4 generates a PLL lock interrupt when the LOCK condition of the PLL has changed, either from a locked state to an unlocked state or vice versa. Lock interrupts are locally disabled by setting the LOCKIE bit to 0. The PLL Lock interrupt flag (LOCKIF) is set to1 when the LOCK condition has changed, and is cleared to 0 by writing a 1 to the LOCKIF bit.

5.6.3 Self-Clock Mode Interrupt

The CRGV4 generates a self-clock mode interrupt when the SCM condition of the system has changed, either entered or exited self-clock mode. SCM conditions can only change if the self-clock mode enable bit (SCME) is set to 1. SCM conditions are caused by a failing clock quality check after power-on reset (POR) or low voltage reset (LVR) or recovery from full stop mode (PSTP = 0) or clock monitor failure. For details on the clock quality check refer to Section 5.4.4, “Clock Quality Checker.” If the clock monitor is enabled (CME = 1) a loss of external clock will also cause a SCM condition (SCME = 1).

SCM interrupts are locally disabled by setting the SCMIE bit to 0. The SCM interrupt flag (SCMIF) is set to 1 when the SCM condition has changed, and is cleared to 0 by writing a 1 to the SCMIF bit.

6.2.3 XCLKS — Input Signal

The XCLKS is an input signal which controls whether a crystal in combination with the internal loop controlled (low power) Pierce oscillator is used or whether full swing Pierce oscillator/external clock circuitry is used. Refer to the Device Overview chapter for polarity and sampling conditions of the XCLKS pin. Table 6-1 lists the state coding of the sampled XCLKS signal.

Table 6-1. Clock Selection Based on XCLKS

XCLKS	Description
0	Loop controlled Pierce oscillator selected
1	Full swing Pierce oscillator/external clock selected

6.3 Memory Map and Register Definition

The CRG contains the registers and associated bits for controlling and monitoring the oscillator module.

6.4 Functional Description

The XOSC module has control circuitry to maintain the crystal oscillator circuit voltage level to an optimal level which is determined by the amount of hysteresis being used and the maximum oscillation range.

The oscillator block has two external pins, EXTAL and XTAL. The oscillator input pin, EXTAL, is intended to be connected to either a crystal or an external clock source. The selection of loop controlled Pierce oscillator or full swing Pierce oscillator/external clock depends on the XCLKS signal which is sampled during reset. The XTAL pin is an output signal that provides crystal circuit feedback.

A buffered EXTAL signal becomes the internal clock. To improve noise immunity, the oscillator is powered by the V_{DDPLL} and V_{SSPLL} power supply pins.

6.4.1 Gain Control

A closed loop control system will be utilized whereby the amplifier is modulated to keep the output waveform sinusoidal and to limit the oscillation amplitude. The output peak to peak voltage will be kept above twice the maximum hysteresis level of the input buffer. Electrical specification details are provided in the Electrical Characteristics appendix.

6.4.2 Clock Monitor

The clock monitor circuit is based on an internal RC time delay so that it can operate without any MCU clocks. If no OSCCLK edges are detected within this RC time delay, the clock monitor indicates failure which asserts self-clock mode or generates a system reset depending on the state of SCME bit. If the clock monitor is disabled or the presence of clocks is detected no failure is indicated.The clock monitor function is enabled/disabled by the CME control bit, described in the CRG block description chapter.

Table 7-17. Analog Input Channel Select Coding

CD	CC	CB	CA	Analog Input Channel
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

Module Base + 0x0001

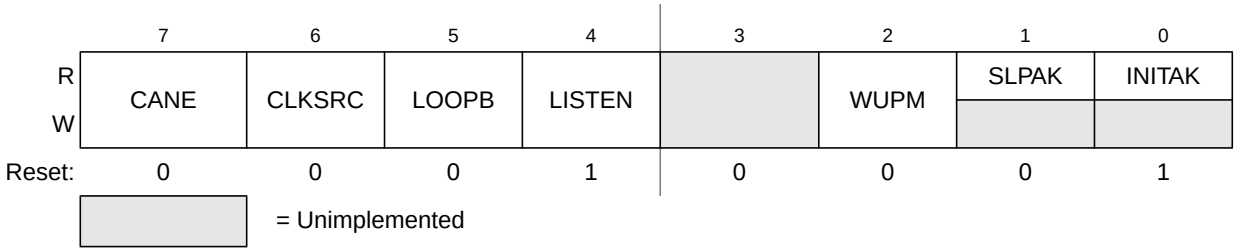

Figure 9-5. MSCAN Control Register 1 (CANCTL1)

Read: Anytime
Write: Anytime when INITRQ = 1 and INITAK = 1, except CANE which is write once in normal and anytime in special system operation modes when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1).

Table 9-2. CANCTL1 Register Field Descriptions

Field	Description
7 CANE	**MSCAN Enable** 0 MSCAN module is disabled 1 MSCAN module is enabled
6 CLKSRC	**MSCAN Clock Source** — This bit defines the clock source for the MSCAN module (only for systems with a clock generation module; Section 9.4.3.2, "Clock System," and Section Figure 9-42., "MSCAN Clocking Scheme,"). 0 MSCAN clock source is the oscillator clock 1 MSCAN clock source is the bus clock
5 LOOPB	**Loopback Self Test Mode** — When this bit is set, the MSCAN performs an internal loopback which can be used for self test operation. The bit stream output of the transmitter is fed back to the receiver internally. The RXCAN input pin is ignored and the TXCAN output goes to the recessive state (logic 1). The MSCAN behaves as it does normally when transmitting and treats its own transmitted message as a message received from a remote node. In this state, the MSCAN ignores the bit sent during the ACK slot in the CAN frame acknowledge field to ensure proper reception of its own message. Both transmit and receive interrupts are generated. 0 Loopback self test disabled 1 Loopback self test enabled
4 LISTEN	**Listen Only Mode** — This bit configures the MSCAN as a CAN bus monitor. When LISTEN is set, all valid CAN messages with matching ID are received, but no acknowledgement or error frames are sent out (see Section 9.4.4.4, "Listen-Only Mode"). In addition, the error counters are frozen. Listen only mode supports applications which require "hot plugging" or throughput analysis. The MSCAN is unable to transmit any messages when listen only mode is active. 0 Normal operation 1 Listen only mode activated
2 WUPM	**Wake-Up Mode** — If WUPE in CANCTL0 is enabled, this bit defines whether the integrated low-pass filter is applied to protect the MSCAN from spurious wake-up (see Section 9.4.5.4, "MSCAN Sleep Mode"). 0 MSCAN wakes up on any dominant level on the CAN bus 1 MSCAN wakes up only in case of a dominant pulse on the CAN bus that has a length of T_{wup}

9.3.2.3 MSCAN Bus Timing Register 0 (CANBTR0)

The CANBTR0 register configures various CAN bus timing parameters of the MSCAN module.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
Reset:	0	0	0	0	0	0	0	0

Figure 9-6. MSCAN Bus Timing Register 0 (CANBTR0)

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 9-3. CANBTR0 Register Field Descriptions

Field	Description
7:6 SJW[1:0]	**Synchronization Jump Width** — The synchronization jump width defines the maximum number of time quanta (Tq) clock cycles a bit can be shortened or lengthened to achieve resynchronization to data transitions on the CAN bus (see Table 9-4).
5:0 BRP[5:0]	**Baud Rate Prescaler** — These bits determine the time quanta (Tq) clock which is used to build up the bit timing (see Table 9-5).

Table 9-4. Synchronization Jump Width

SJW1	SJW0	Synchronization Jump Width
0	0	1 Tq clock cycle
0	1	2 Tq clock cycles
1	0	3 Tq clock cycles
1	1	4 Tq clock cycles

Table 9-5. Baud Rate Prescaler

BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	Prescaler value (P)
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
:	:	:	:	:	:	:
1	1	1	1	1	1	64

NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the **Tx output** signal. Setting TE after the stop bit appears on **Tx output signal** causes data previously written to the SCI data register to be lost. Toggle the TE bit for a queued idle character while the TDRE flag is set and immediately before writing the next byte to the SCI data register.

NOTE

If the TE bit is clear and the transmission is complete, the SCI is not the master of the TXD pin

10.4.4 Receiver

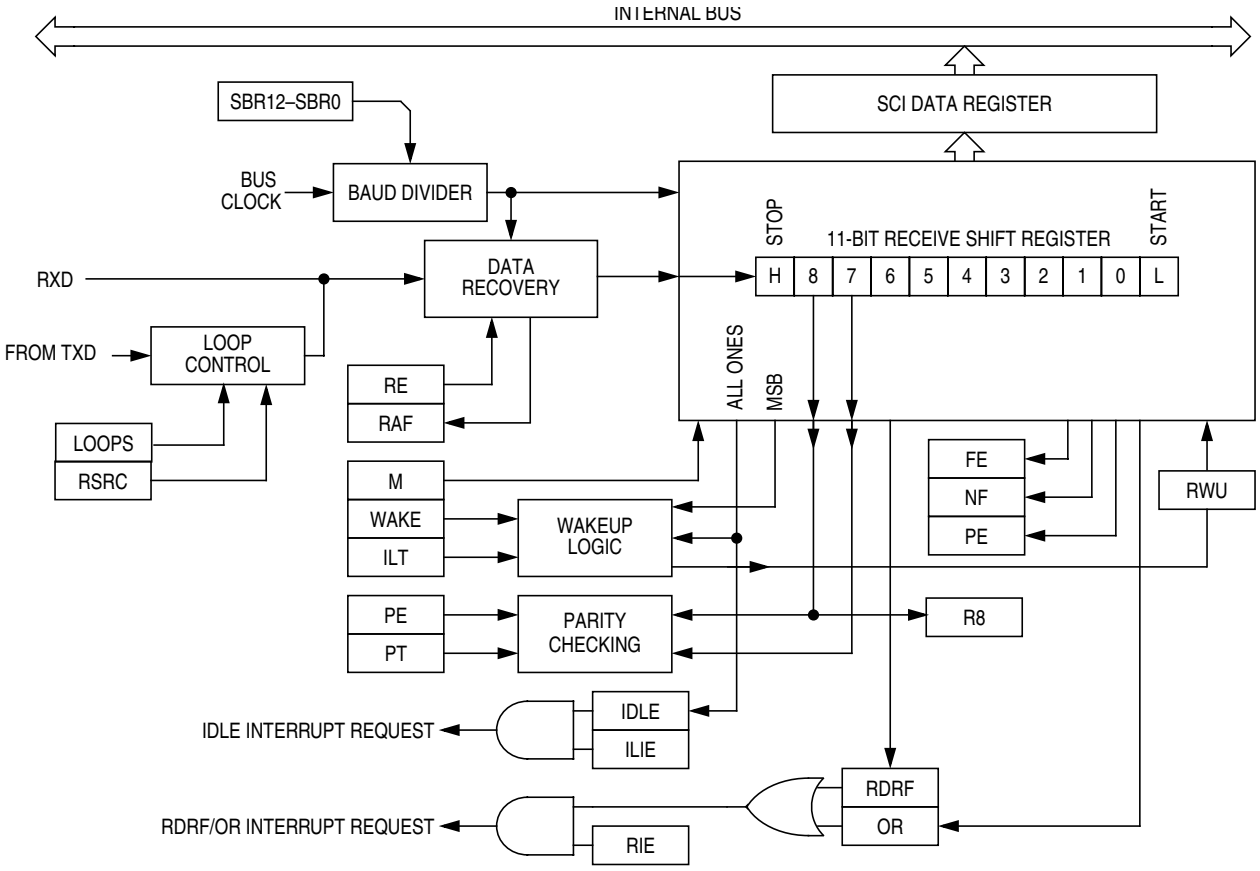

Figure 10-12. SCI Receiver Block Diagram

10.4.4.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

On the front end of the PWM timer, the clock is enabled to the PWM circuit by the PWMEx bit being high. There is an edge-synchronizing circuit to guarantee that the clock will only be enabled or disabled at an edge. When the channel is disabled (PWMEx = 0), the counter for the channel does not count.

12.4.2.2 PWM Polarity

Each channel has a polarity bit to allow starting a waveform cycle with a high or low signal. This is shown on the block diagram as a mux select of either the Q output or the $\overline{Q}$ output of the PWM output flip flop. When one of the bits in the PWMPOL register is set, the associated PWM channel output is high at the beginning of the waveform, then goes low when the duty count is reached. Conversely, if the polarity bit is zero, the output starts low and then goes high when the duty count is reached.

12.4.2.3 PWM Period and Duty

Dedicated period and duty registers exist for each channel and are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period and duty registers will go directly to the latches as well as the buffer.

A change in duty or period can be forced into effect “immediately” by writing the new value to the duty and/or period registers and then writing to the counter. This forces the counter to reset and the new duty and/or period values to be latched. In addition, since the counter is readable, it is possible to know where the count is with respect to the duty value and software can be used to make adjustments

NOTE

When forcing a new period or duty into effect immediately, an irregular PWM cycle can occur.

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time.

12.4.2.4 PWM Timer Counters

Each channel has a dedicated 8-bit up/down counter which runs at the rate of the selected clock source (see Section 12.4.1, “PWM Clock Select” for the available clock sources and rates). The counter compares to two registers, a duty register and a period register as shown in Figure 12-19. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register behaves differently depending on what output mode is selected as shown in Figure 12-19 and described in Section 12.4.2.5, “Left Aligned Outputs” and Section 12.4.2.6, “Center Aligned Outputs”.

If a read command is issued but the data is not retrieved within 512 serial clock cycles, a soft-reset will occur causing the command to be disregarded. The data is not available for retrieval after the time-out has occurred. This is the expected behavior if the handshake protocol is not enabled. However, consider the behavior where the BDC is running in a frequency much greater than the CPU frequency. In this case, the command could time out before the data is ready to be retrieved. In order to allow the data to be retrieved even with a large clock frequency mismatch (between BDC and CPU) when the hardware handshake protocol is enabled, the time out between a read command and the data retrieval is disabled. Therefore, the host could wait for more then 512 serial clock cycles and continue to be able to retrieve the data from an issued read command. However, as soon as the handshake pulse (ACK pulse) is issued, the time-out feature is re-activated, meaning that the target will time out after 512 clock cycles. Therefore, the host needs to retrieve the data within a 512 serial clock cycles time frame after the ACK pulse had been issued. After that period, the read command is discarded and the data is no longer available for retrieval. Any falling edge of the BKGD pin after the time-out period is considered to be a new command or a SYNC request.

Note that whenever a partially issued command, or partially retrieved data, has occurred the time out in the serial communication is active. This means that if a time frame higher than 512 serial clock cycles is observed between two consecutive negative edges and the command being issued or data being retrieved is not complete, a soft-reset will occur causing the partially received command or data retrieved to be disregarded. The next falling edge of the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDM command, or the start of a SYNC request pulse.

15.4.13 Operation in Wait Mode

The BDM cannot be used in wait mode if the system disables the clocks to the BDM.

There is a clearing mechanism associated with the WAIT instruction when the clocks to the BDM (CPU core platform) are disabled. As the clocks restart from wait mode, the BDM receives a soft reset (clearing any command in progress) and the ACK function will be disabled. This is a change from previous BDM modules.

15.4.14 Operation in Stop Mode

The BDM is completely shutdown in stop mode.

There is a clearing mechanism associated with the STOP instruction. STOP must be enabled and the part must go into stop mode for this to occur. As the clocks restart from stop mode, the BDM receives a soft reset (clearing any command in progress) and the ACK function will be disabled. This is a change from previous BDM modules.

A.2 Voltage Regulator

This section describes the characteristics of the on chip voltage regulator.

Table A-9. VREG_3V3 — Operating Conditions

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	P	Input Voltages	$V_{VDDR,A}$	3.15	—	5.5	V
2	P	Output Voltage Core Full Performance Mode	V_{DD}	2.35	2.5	2.75	V
3	P	Output Voltage PLL Full Performance Mode	V_{DDPLL}	2.35	2.5	2.75	V
4	P	Low Voltage Interrupt[1] Assert Level Deassert Level	 V_{LVIA} V_{LVID}	 4.0 4.15	 4.37 4.52	 4.66 4.77	 V V
5	P	Low Voltage Reset[2] Assert Level Deassert Level	 V_{LVRA} V_{LVRD}	 2.25 —	 — —	 — 2.55	 V V
6	C	Power-on Reset[3] Assert Level Deassert Level	 V_{PORA} V_{PORD}	 0.97 —	 — -—	 — 2.05	 V V

1 Monitors V_{DDA}, active only in Full Performance Mode. Indicates I/O & ADC performance degradation due to low supply voltage.

2 Monitors V_{DD}, active only in Full Performance Mode. V_{LVRA} and V_{PORD} must overlap

3 Monitors V_{DD}. Active in all modes.

The electrical characteristics given in this section are preliminary and should be used as a guide only. Values in this section cannot be guaranteed by Freescale and are subject to change without notice.

A.6.1.3 Sector Erase

Erasing a 1024 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.6.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.6.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-16. NVM Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5	—	50 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1	—	—	MHz
3	D	Operating Frequency	f_{NVMOP}	150	—	200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]	—	74.5 [3]	µs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 [2]	—	31 [3]	µs
6	D	Flash Burst Programming Time for 64 Words [4]	t_{brpgm}	1331.2 [2]	—	2027.5 [3]	µs
7	P	Sector Erase Time	t_{era}	20 [5]	—	26.7 [3]	ms
8	P	Mass Erase Time	t_{mass}	100 [5]	—	133 [3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]	—	65546 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 [6]	—	2058[7]	t_{cyc}

1 Restrictions for oscillator in crystal mode apply!

2 Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3 Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formula in Section A.6.1.1, “Single Word Programming” and Section A.6.1.4, “Mass Erase” for guidance.

4 Burst Programming operations are not applicable to EEPROM

5 Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}

6 Minimum time, if first word in the array is not blank

7 Maximum time to complete check on an erased block

Appendix C
Package Information

This section provides the physical dimensions of the MC9S12KG128 packages.