Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12kg128vfue

Table 1-2. Signal Properties (Sheet 2 of 3)

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
PH4	**KWH4**	**MISO2**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, MISO of SPI2**
PH3	**KWH3**	**$\overline{SS1}$**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, $\overline{SS}$ of SPI1**
PH2	**KWH2**	**SCK1**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, SCK of SPI1**
PH1	**KWH1**	**MOSI1**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, MOSI of SPI1**
PH0	**KWH0**	**MISO1**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, MISO of SPI1**
PJ7	KWJ7	TXCAN4	SCL	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, TX of CAN4, SCL of IIC
PJ6	KWJ6	RXCAN4	SDA	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, RX of CAN4, SDA of IIC
PJ[1:0]	**KWJ[1:0]**	**—**	**—**	**VDDX**	**PERJ/ PPSJ**	**Up**	**Port J I/O, Interrupts**
PK7	**$\overline{ECS}$**	**ROMCTL**	**—**	**VDDX**	**PUCR**	**Up**	**Port K I/O, Emulation Chip Select, ROM On Enable**
PK[5:0]	**XADDR[19:14]**	**—**	**—**	**VDDX**	**PUCR**	**Up**	**Port K I/O, Extended Addresses**
PM7	**TXCAN4**	**—**	**—**	**VDDX**	**PERM/ PPSM**	**Disabled**	**Port M I/O, CAN4 TX**
PM6	**RXCAN4**	**—**	**—**	**VDDX**	**PERM/ PPSM**	**Disabled**	**Port M I/O, CAN4 RX**
PM5	TXCAN0	TXCAN4	SCK0	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 TX, CAN4 TX, SPI0 SCK
PM4	RXCAN0	RXCAN4	MOSI0	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 RX, CAN4 RX, SPI0 MOSI
PM3	TXCAN0	—	$\overline{SS0}$	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 TX, SPI0 $\overline{SS}$
PM2	RXCAN0	—	MISO0	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 RX, SPI0 MISO
PM1	TXCAN0	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 TX
PM0	RXCAN0	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 RX
PP7	KWP7	PWM7	SCK2	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, PWM Channel 7, SCK of SPI2
PP6	**KWP6**	**PWM6**	**$\overline{SS2}$**	**VDDX**	**PERP/ PPSP**	**Disabled**	**Port P I/O, Interrupt, PWM Channel 6, SPI2 $\overline{SS}$**

0x00F0–0x00F7 SPI1 (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00F0	SPI1CR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x00F1	SPI1CR2	R	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x00F2	SPI1BR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x00F3	SPI1SR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x00F4	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00F5	SPI1DR	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00F6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00F7	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x00F8–0x00FF SPI2 (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00F8	SPI2CR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x00F9	SPI2CR2	R	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x00FA	SPI2BR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x00FB	SPI2SR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x00FC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00FD	SPI2DR	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00FE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0100–0x010F Flash Control Register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0100	FCLKDIV	R	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		W								
0x0101	FSEC	R	KEYEN		RNV5	RNV4	RNV3	RNV2	SEC	
		W								

0x0240–0x027F PIM (Port Integration Module) (Sheet 2 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0243	RDRT	R	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		W								
0x0244	PERT	R	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		W								
0x0245	PPST	R	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		W								
0x0246	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0247	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0248	PTS	R	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
		W								
0x0249	PTIS	R	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		W								
0x024A	DDRS	R	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		W								
0x024B	RDRS	R	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
		W								
0x024C	PERS	R	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		W								
0x024D	PPSS	R	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		W								
0x024E	WOMS	R	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		W								
0x024F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0250	PTM	R	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		W								
0x0251	PTIM	R	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		W								
0x0252	DDRM	R	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		W								
0x0253	RDRM	R	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
		W								
0x0254	PERM	R	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		W								
0x0255	PPSM	R	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		W								
0x0256	WOMM	R	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		W								
0x0257	MODRR	R	0	MODRR6	MODRR5	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
		W								
0x0258	PTP	R	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		W								
0x0259	PTIP	R	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		W								

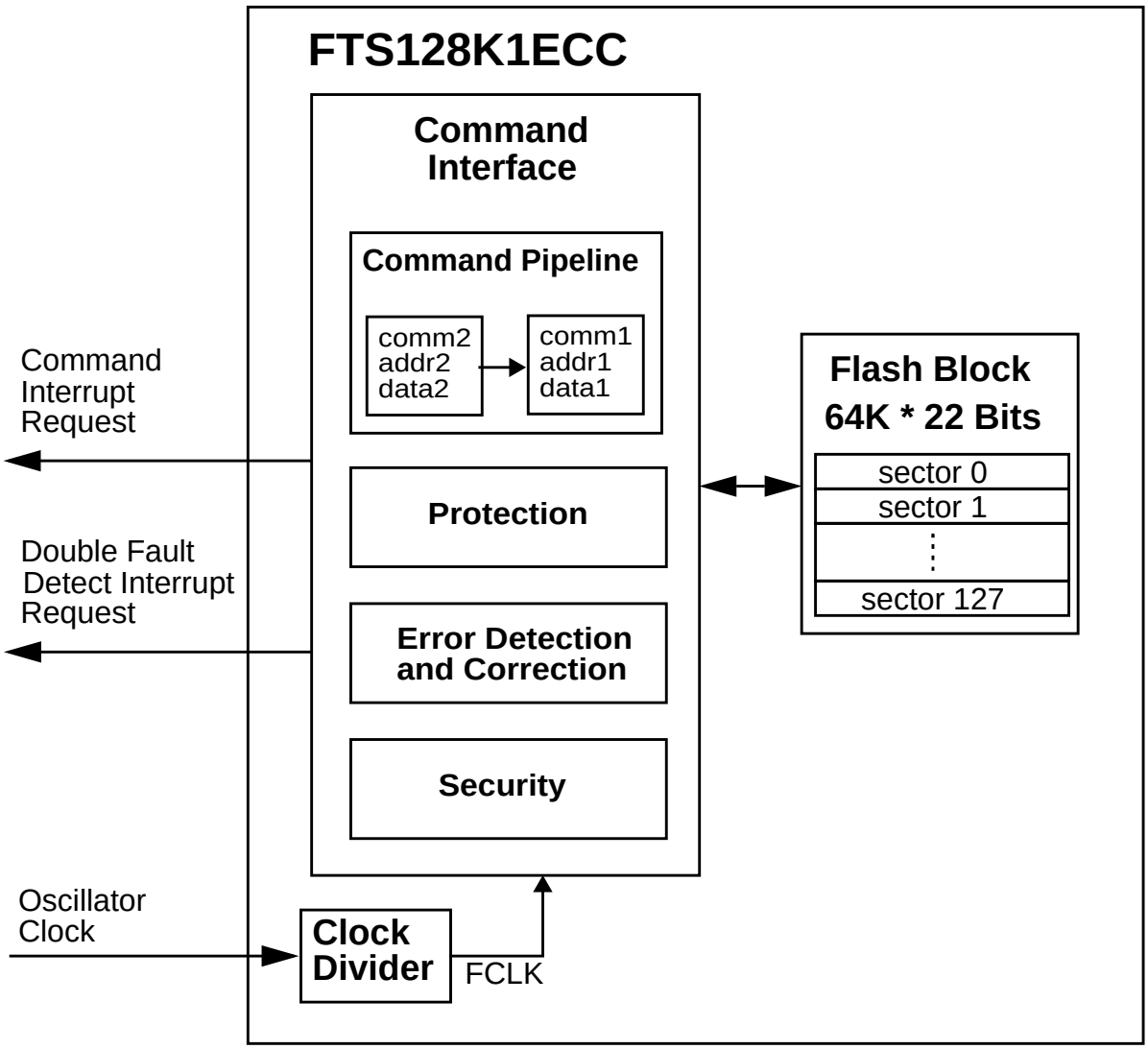

Figure 2-1. FTS128K1ECC Block Diagram

2.2 External Signal Description

The Flash module contains no signals that connect off-chip.

2.3 Memory Map and Register Definition

This subsection describes the memory map and registers for the Flash module.

2.3.1 Module Memory Map

The Flash memory map is shown in Figure 2-2. The HCS12 architecture places the Flash memory addresses between 0x4000 and 0xFFFF which corresponds to three 16-Kbyte pages. The content of the

4.3.2.6 Port S Polarity Select Register (PPSS)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R W	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
Reset	0	0	0	0	0	0	0	0

Figure 4-13. Port S Polarity Select Register (PPSS)

Read: Anytime. Write: Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

Table 4-10. PPSS Field Descriptions

Field	Description
7–0 PPSS[7:0]	**Pull Select Port S** 0 A pull-up device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input or as wired-OR output. 1 A pull-down device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input.

4.3.2.7 Port S Wired-OR Mode Register (WOMS)

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R W	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
Reset	0	0	0	0	0	0	0	0

Figure 4-14. Port S Wired-OR Mode Register (WOMS)

Read: Anytime. Write: Anytime.

This register configures the output pins as wired-OR. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven. It applies also to the SPI and SCI outputs and allows a multipoint connection of several serial modules. This bit has no influence on pins used as inputs.

Table 4-11. WOMS Field Descriptions

Field	Description
7–0 WOMS[7:0]	**Wired-OR Mode Port S** 0 Output buffers operate as push-pull outputs. 1 Output buffers operate as open-drain outputs.

4.5 Resets

The reset values of all registers are given in the Register Description in Section 4.3, “Memory Map and Register Definition”.

4.5.1 Reset Initialization

All registers including the data registers get set/reset asynchronously. Table 4-44 summarizes the port properties after reset initialization.

Table 4-44. Port Reset State Summary

Port	Reset States				
	Data Direction	Pull Mode	Reduced Drive	Wired-OR Mode	Interrupt
T	Input	Hi-Z	Disabled	N/A	N/A
S	Input	Pull-up	Disabled	Disabled	N/A
M	Input	Hi-Z	Disabled	Disabled	N/A
P	Input	Hi-Z	Disabled	N/A	Disabled
H	Input	Hi-Z	Disabled	N/A	Disabled
J	Input	Pull-up	Disabled	N/A	Disabled

4.6 Interrupts

4.6.1 General

Port P, H and J generate a separate edge sensitive interrupt if enabled. Each port offers I/O pins with edge triggered interrupt capability in wired-or fashion. The interrupt enable as well as the sensitivity to rising or falling edges can be individually configured on per pin basis. All bits/pins per port share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a bit in the port interrupt flag register and its corresponding port interrupt enable bit are both set. This external interrupt feature is capable to wake up the CPU when it is in stop or wait mode.

A digital filter on each pin prevents pulses (Figure 4-49) shorter than a specified time from generating an interrupt. The minimum time varies over process conditions, temperature and voltage (Figure 4-50 and Table 4-45).

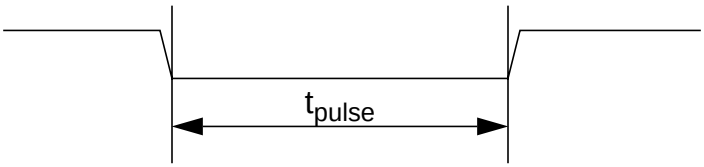

Figure 4-49. Pulse Illustration

Chapter 7
Analog-to-Digital Converter (ATD10B16CV3) Block Description

7.1 Introduction

The ATD10B16C is a 16-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electical for ATD accuracy.

7.1.1 Features

- 8-/10-bit resolution
- 7 µs, 10-bit single conversion time
- Sample buffer amplifier
- Programmable sample time
- Left/right justified, signed/unsigned result data
- External trigger control
- Conversion completion interrupt generation
- Analog input multiplexer for 16 analog input channels
- Analog/digital input pin multiplexing
- 1 to 16 conversion sequence lengths
- Continuous conversion mode
- Multiple channel scans
- Configurable external trigger functionality on any AD channel or additional trigger input. The additional trigger input can be chip external or internal. Refer to device specification for availability and connectivity
- Configurable location for channel wrap around (when converting multiple channels in a sequence)

7.1.2 Modes of Operation

There is software programmable selection between performing **single** or **continuous conversion** on a **single channel** or **multiple channels**.

7.1.3 Block Diagram

Refer to Figure 7-1 for a block diagram of the ATD0B16C block.

In either level or edge triggered modes, the first conversion begins when the trigger is received. In both cases, the maximum latency time is one bus clock cycle plus any skew or delay introduced by the trigger circuitry.

After ETRIGE is enabled, conversions cannot be started by a write to ATDCTL5, but rather must be triggered externally.

If the level mode is active and the external trigger both de-asserts and re-asserts itself during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger remains asserted in level mode while a sequence is completing, another sequence will be triggered immediately.

7.4.2.2 General-Purpose Digital Input Port Operation

The input channel pins can be multiplexed between analog and digital data. As analog inputs, they are multiplexed and sampled to supply signals to the A/D converter. As digital inputs, they supply external input data that can be accessed through the digital port registers (PORTAD0 & PORTAD1) (input-only).

The analog/digital multiplex operation is performed in the input pads. The input pad is always connected to the analog inputs of the ATD10B16C. The input pad signal is buffered to the digital port registers. This buffer can be turned on or off with the ATDDIEN0 & ATDDIEN1 register. This is important so that the buffer does not draw excess current when analog potentials are presented at its input.

7.4.3 Operation in Low Power Modes

The ATD10B16C can be configured for lower MCU power consumption in three different ways:

- **Stop Mode**
  Stop Mode: This halts A/D conversion. Exit from Stop mode will resume A/D conversion, But due to the recovery time the result of this conversion should be ignored.

  Entering stop mode causes all clocks to halt and thus the system is placed in a minimum power standby mode. This halts any conversion sequence in progress. During recovery from stop mode, there must be a minimum delay for the stop recovery time t_{SR} before initiating a new ATD conversion sequence.
- **Wait Mode**
  Wait Mode with AWAI = 1: This halts A/D conversion. Exit from Wait mode will resume A/D conversion, but due to the recovery time the result of this conversion should be ignored.

  Entering wait mode, the ATD conversion either continues or halts for low power depending on the logical value of the AWAIT bit.
- **Freeze Mode**
  Writing ADPU = 0 (Note that all ATD registers remain accessible.): This aborts any A/D conversion in progress.

  In freeze mode, the ATD10B16C will behave according to the logical values of the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

NOTE

The reset value for the ADPU bit is zero. Therefore, when this module is reset, it is reset into the power down state.

In cases of more than one buffer having the same lowest priority, the message buffer with the lower index number wins.

Module Base + 0xXXXD

	7	6	5	4	3	2	1	0
R W	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
Reset:	0	0	0	0	0	0	0	0

Figure 9-35. Transmit Buffer Priority Register (TBPR)

Read: Anytime when TXEx flag is set (see Section 9.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 9.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

Write: Anytime when TXEx flag is set (see Section 9.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 9.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

9.3.3.5 Time Stamp Register (TSRH–TSRL)

If the TIME bit is enabled, the MSCAN will write a time stamp to the respective registers in the active transmit or receive buffer right after the EOF of a valid message on the CAN bus (see Section 9.3.2.1, "MSCAN Control Register 0 (CANCTL0)"). In case of a transmission, the CPU can only read the time stamp after the respective transmit buffer has been flagged empty.

The timer value, which is used for stamping, is taken from a free running internal CAN bit clock. A timer overrun is not indicated by the MSCAN. The timer is reset (all bits set to 0) during initialization mode. The CPU can only read the time stamp registers.

Module Base + 0xXXXE

	7	6	5	4	3	2	1	0
R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
W								
Reset:	x	x	x	x	x	x	x	x

Figure 9-36. Time Stamp Register — High Byte (TSRH)

Module Base + 0xXXXF

	7	6	5	4	3	2	1	0
R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
W								
Reset:	x	x	x	x	x	x	x	x

Figure 9-37. Time Stamp Register — Low Byte (TSRL)

- Four identifier acceptance filters, each to be applied to
  - a) the 14 most significant bits of the extended identifier plus the SRR and IDE bits of CAN 2.0B messages or
  - b) the 11 bits of the standard identifier, the RTR and IDE bits of CAN 2.0A/B messages. Figure 9-40 shows how the first 32-bit filter bank (CANIDAR0–CANIDA3, CANIDMR0–3CANIDMR) produces filter 0 and 1 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 2 and 3 hits.
- Eight identifier acceptance filters, each to be applied to the first 8 bits of the identifier. This mode implements eight independent filters for the first 8 bits of a CAN 2.0A/B compliant standard identifier or a CAN 2.0B compliant extended identifier. Figure 9-41 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces filter 0 to 3 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 4 to 7 hits.
- Closed filter. No CAN message is copied into the foreground buffer RxFG, and the RXF flag is never set.

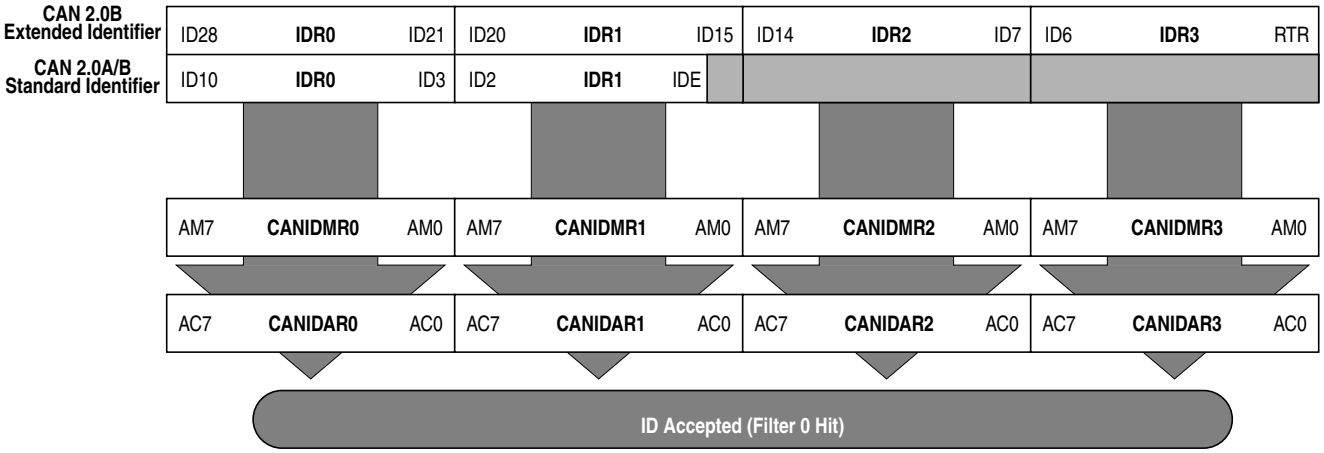

Figure 9-39. 32-bit Maskable Identifier Acceptance Filter

With the misaligned character shown in Figure 10-20, the receiver counts 167 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit character with no errors is:

((167 – 160) / 167) X 100 = 4.19%

10.4.4.5.2 Fast Data Tolerance

Figure 10-21 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but is still sampled at RT8, RT9, and RT10.

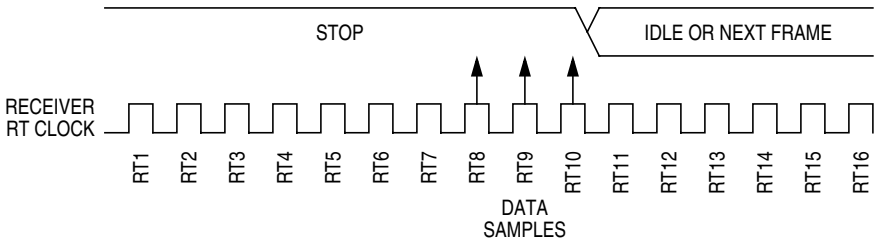

Figure 10-21. Fast Data

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles + 10 RTr cycles = 154 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 10-21, the receiver counts 154 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is:

((160 – 154) / 160) x 100 = 3.75%

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 10 RTr cycles = 170 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 10-21, the receiver counts 170 RTr cycles at the point when the count of the transmitting device is 11 bit times x 16 RTt cycles = 176 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is:

((176 – 170) / 176) x 100 = 3.40%

10.4.4.6 Receiver Wakeup

To enable the SCI to ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCI control register 2 (SCICR2) puts the receiver into standby state during which receiver interrupts are disabled.The SCI will still load the receive data into the SCIDRH/L registers, but it will not set the RDRF flag.

The 16-bit main timer is an up counter.

A full access for the counter register should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

Read: Anytime

Write: Has no meaning or effect in the normal mode; only writable in special modes (test_mode = 1).

The period of the first count after a write to the TCNT registers may be a different size because the write is not synchronized with the prescaler clock.

13.3.2.6 Timer System Control Register 1 (TSCR1)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-12. Timer System Control Register 1 (TSCR1)

Read: Anytime

Write: Anytime

Table 13-7. TSCR1 Field Descriptions

Field	Description
7 TEN	**Timer Enable** 0 Disables the main timer, including the counter. Can be used for reducing power consumption. 1 Allows the timer to function normally. If for any reason the timer is not active, there is no ÷64 clock for the pulse accumulator because the ÷64 is generated by the timer prescaler.
6 TSWAI	**Timer Module Stops While in Wait** 0 Allows the timer module to continue running during wait. 1 Disables the timer module when the MCU is in the wait mode. Timer interrupts cannot be used to get the MCU out of wait. TSWAI also affects pulse accumulator.

15.3 Memory Map and Register Definition

A summary of the registers associated with the BDM is shown in Figure 15-2. Registers are accessed by host-driven communications to the BDM hardware using READ_BD and WRITE_BD commands. Detailed descriptions of the registers and associated bits are given in the subsections that follow.

15.3.1 Module Memory Map

Table 15-1. INT Memory Map

Register Address	Use	Access
0xFF00	Reserved	—
0xFF01	BDM Status Register (BDMSTS)	R/W
0xFF02–0xFF05	Reserved	—
0xFF06	BDM CCR Holding Register (BDMCCR)	R/W
0xFF07	BDM Internal Register Position (BDMINR)	R
0xFF08–0xFF0B	Reserved	—

16.3.2.5 Debug Comparator C Extended Register (DBGCCX)

Module Base + 0x0025
Starting address location affected by INITRG register setting.

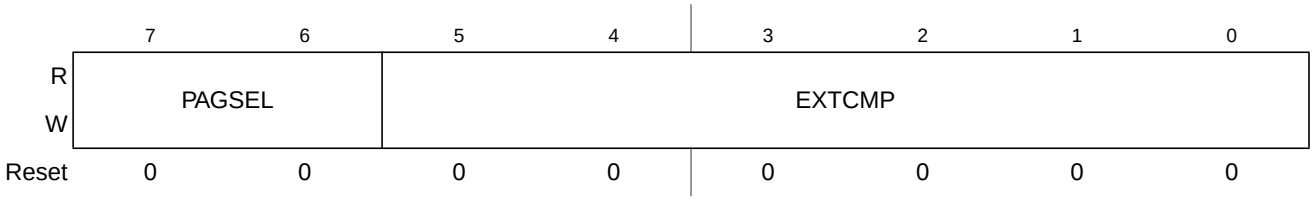

Figure 16-9. Debug Comparator C Extended Register (DBGCCX)

Table 16-10. DBGCCX Field Descriptions

Field	Description
7:6 PAGSEL	**Page Selector Field** — In both BKP and DBG mode, PAGSEL selects the type of paging as shown in Table 16-11. DPAGE and EPAGE are not yet implemented so the value in bit 7 will be ignored (i.e., PAGSEL values of 10 and 11 will be interpreted as values of 00 and 01, respectively).
5:0 EXTCMP	**Comparator C Extended Compare Bits** — The EXTCMP bits are used as comparison address bits as shown in Table 16-11 along with the appropriate PPAGE, DPAGE, or EPAGE signal from the core. **Note:** Comparator C can be used when the DBG module is configured for BKP mode. Extended addressing comparisons for comparator C use PAGSEL and will operate differently to the way that comparator A and B operate in BKP mode.

Table 16-11. PAGSEL Decoding[1]

PAGSEL	Description	EXTCMP	Comment
00	Normal (64k)	Not used	No paged memory
01	PPAGE (256 — 16K pages)	EXTCMP[5:0] is compared to address bits [21:16][2]	PPAGE[7:0] / XAB[21:14] becomes address bits [21:14][1]
10[3]	DPAGE (reserved) (256 — 4K pages)	EXTCMP[3:0] is compared to address bits [19:16]	DPAGE / XAB[21:14] becomes address bits [19:12]
11[2]	EPAGE (reserved) (256 — 1K pages)	EXTCMP[1:0] is compared to address bits [17:16]	EPAGE / XAB[21:14] becomes address bits [17:10]

1 See Figure 16-10.

2 Current HCS12 implementations have PPAGE limited to 6 bits. Therefore, EXTCMP[5:4] should be set to 00.

3 Data page (DPAGE) and Extra page (EPAGE) are reserved for implementation on devices that support paged data and extra space.

16.4.2.5.8 Inside Range (A ≤ address ≤ B)

In the inside range trigger mode, if the match condition for A and B happen on the same bus cycle, both the A and B flags in DBGSC are set and a trigger occurs. If a match condition on only A or only B occurs no flags are set. If TRGSEL = 1, the inside range is accurate only to word boundaries. If TRGSEL = 0, an aligned word access which straddles the range boundary will cause a trigger only if the aligned address is within the range.

16.4.2.5.9 Outside Range (address < A or address > B)

In the outside range trigger mode, if the match condition for A or B is met, the corresponding flag in DBGSC is set and a trigger occurs. If TRGSEL = 1, the outside range is accurate only to word boundaries. If TRGSEL = 0, an aligned word access which straddles the range boundary will cause a trigger only if the aligned address is outside the range.

16.4.2.5.10 Control Bit Priorities

The definitions of some of the control bits are incompatible with each other. Table 16-25 and the notes associated with it summarize how these incompatibilities are managed:

- Read/write comparisons are not compatible with TRGSEL = 1. Therefore, RWAEN and RWBEN are ignored.
- Event-only trigger modes are always considered a begin-type trigger. See Section 16.4.2.8.1, “Storing with Begin-Trigger,” and Section 16.4.2.8.2, “Storing with End-Trigger.”
- Detail capture mode has priority over the event-only trigger/capture modes. Therefore, event-only modes have no meaning in detail mode and their functions default to similar trigger modes.

Table 16-25. Resolution of Mode Conflicts

Mode	Normal / Loop1		Detail	
	Tag	Force	Tag	Force
A only				
A or B				
A then B				
Event-only B	1		1, 3	3
A then event-only B	2		4	4
A and B (full mode)	5		5	
A and not B (full mode)	5		5	
Inside range	6		6	
Outside range	6		6	

1 — Ignored — same as force
2 — Ignored for comparator B
3 — Reduces to effectively “B only”
4 — Works same as A then B
5 — Reduces to effectively “A only” — B not compared
6 — Only accurate to word boundaries

18.3.2.16 Port K Data Direction Register (DDRK)

Module Base + 0x0033
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 18-20. Port K Data Direction Register (DDRK)

Read: Anytime

Write: Anytime

This register determines the primary direction for each port K pin configured as general-purpose I/O. This register is not in the map in peripheral or expanded modes while the EMK control bit in MODE register is set. Therefore, these accesses will be echoed externally.

Table 18-14. EBICTL Field Descriptions

Field	Description
7:0 DDRK	**Data Direction Port K Bits** 0 Associated pin is a high-impedance input 1 Associated pin is an output **Note:** It is unwise to write PORTK and DDRK as a word access. If you are changing port K pins from inputs to outputs, the data may have extra transitions during the write. It is best to initialize PORTK before enabling as outputs. **Note:** To ensure that you read the correct value from the PORTK pins, always wait at least one cycle after writing to the DDRK register before reading from the PORTK register.

18.4 Functional Description

18.4.1 Detecting Access Type from External Signals

The external signals $\overline{\text{LSTRB}}$, R/$\overline{\text{W}}$, and AB0 indicate the type of bus access that is taking place. Accesses to the internal RAM module are the only type of access that would produce $\overline{\text{LSTRB}}$ = AB0 = 1, because the internal RAM is specifically designed to allow misaligned 16-bit accesses in a single cycle. In these cases the data for the address that was accessed is on the low half of the data bus and the data for address + 1 is on the high half of the data bus. This is summarized in Table 18-15.

Table 18-15. Access Type vs. Bus Control Pins

$\overline{\text{LSTRB}}$	AB0	R/$\overline{\text{W}}$	Type of Access
1	0	1	8-bit read of an even address
0	1	1	8-bit read of an odd address
1	0	0	8-bit write of an even address
0	1	0	8-bit write of an odd address

Appendix A
Electrical Characteristics

A.1 General

NOTE

The electrical characteristics given in this section are preliminary and should be used as a guide only. Values cannot be guaranteed by Freescale and are subject to change without notice.

This supplement contains the most accurate electrical information for the MC9S12KG128 microcontroller available at the time of publication. The information should be considered **PRELIMINARY** and is subject to change.

This introduction is intended to give an overview on several common topics like power supply, current injection, etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

NOTE

This classification is shown in the column labeled “C” in the parameter tables where appropriate.

P: Those parameters are guaranteed during production testing on each individual device.

C: Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. They are regularly verified by production monitors.

T: Those parameters are achieved by design characterization on a small sample size from typical devices. All values shown in the typical column are within this category.

D: Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12KG128 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator, PLL and internal logic.

The VDDA, VSSA pair supplies the A/D converter.

The VDDX, VSSX pair supplies the I/O pins.

The VDDR, VSSR pair supplies the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic.

VDDPLL, VSSPLL supply the oscillator and the PLL.

A.6.1.3 Sector Erase

Erasing a 1024 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.6.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.6.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-16. NVM Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5	—	50 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1	—	—	MHz
3	D	Operating Frequency	f_{NVMOP}	150	—	200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]	—	74.5 [3]	µs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 [2]	—	31 [3]	µs
6	D	Flash Burst Programming Time for 64 Words [4]	t_{brpgm}	1331.2 [2]	—	2027.5 [3]	µs
7	P	Sector Erase Time	t_{era}	20 [5]	—	26.7 [3]	ms
8	P	Mass Erase Time	t_{mass}	100 [5]	—	133 [3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]	—	65546 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 [6]	—	2058[7]	t_{cyc}

1 Restrictions for oscillator in crystal mode apply!

2 Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3 Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formula in Section A.6.1.1, “Single Word Programming” and Section A.6.1.4, “Mass Erase” for guidance.

4 Burst Programming operations are not applicable to EEPROM

5 Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}

6 Minimum time, if first word in the array is not blank

7 Maximum time to complete check on an erased block

A.7.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.7.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

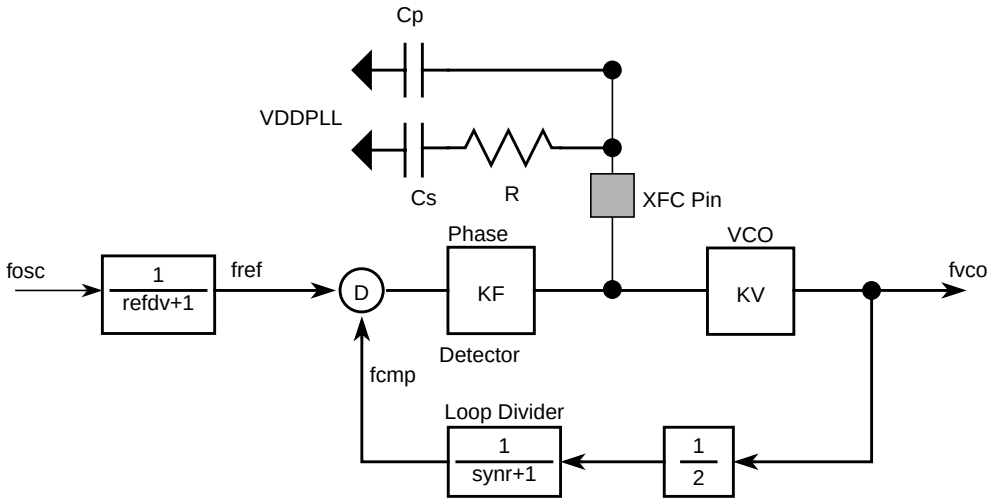

Figure A-3. Basic PLL Functional Diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from Table A-20.

The grey boxes show the calculation for f_{VCO} = 50MHz and f_{ref} = 1MHz. E.g., these frequencies are used for f_{OSC} = 4MHz and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60-50)}{-100}} = \text{-90.48MHz/V}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

And finally the frequency relationship is defined as

Appendix B
Recommended PCB Layout

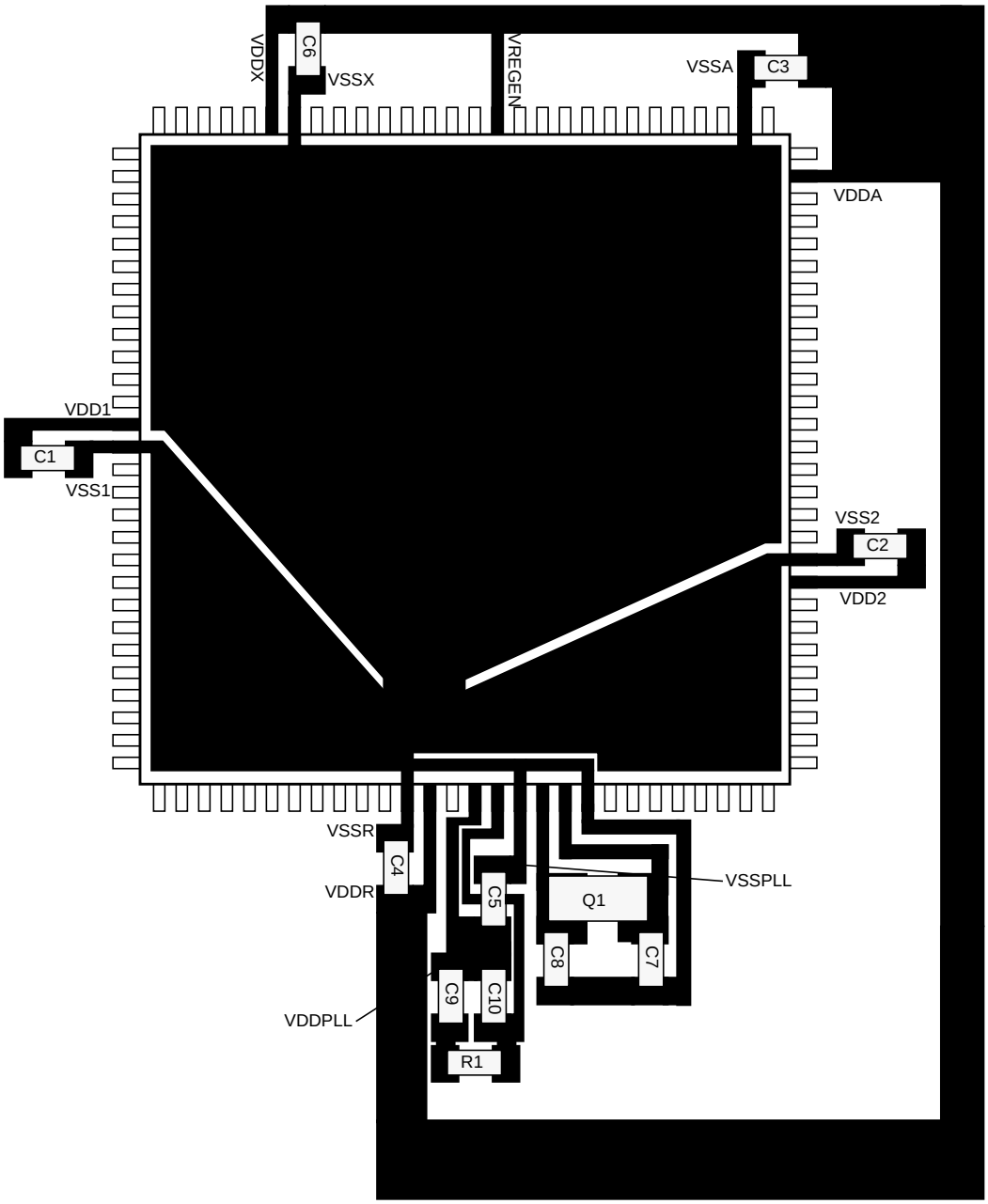

Figure B-1. Recommended PCB Layout for 112LQFP