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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f6393t-i-pt

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PIC18F6393/6493/8393/8493

NOTES:

PIC18F6393/6493/8393/8493

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6393
- PIC18F8393
- PIC18F6493
- PIC18F8493

Note: This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F6390/6490/8390/8490 devices. For information on the features and specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price. In addition to these features, the PIC18F6393/6493/8393/8493 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

1.1 Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduces code overhead.

1.2 Details on Individual Family Members

Devices in the PIC18F6393/6493/8393/8493 family are available in 64-pin (PIC18F6X93) and 80-pin (PIC18F8X93) packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2, respectively.

The devices are differentiated from each other in the following ways:

- I/O Ports:
 - 64-pin devices – 7 bidirectional ports
 - 80-pin devices – 9 bidirectional ports
- LCD Pixels:
 - 64-pin devices – 128 (32 SEGs x 4 COMs) pixels can be driven
 - 80-pin devices – 192 (48 SEGs x 4 COMs) pixels can be driven
- Flash Program Memory:
 - PIC18FX393 devices – 8 Kbytes
 - PIC18FX493 devices – 16 Kbytes

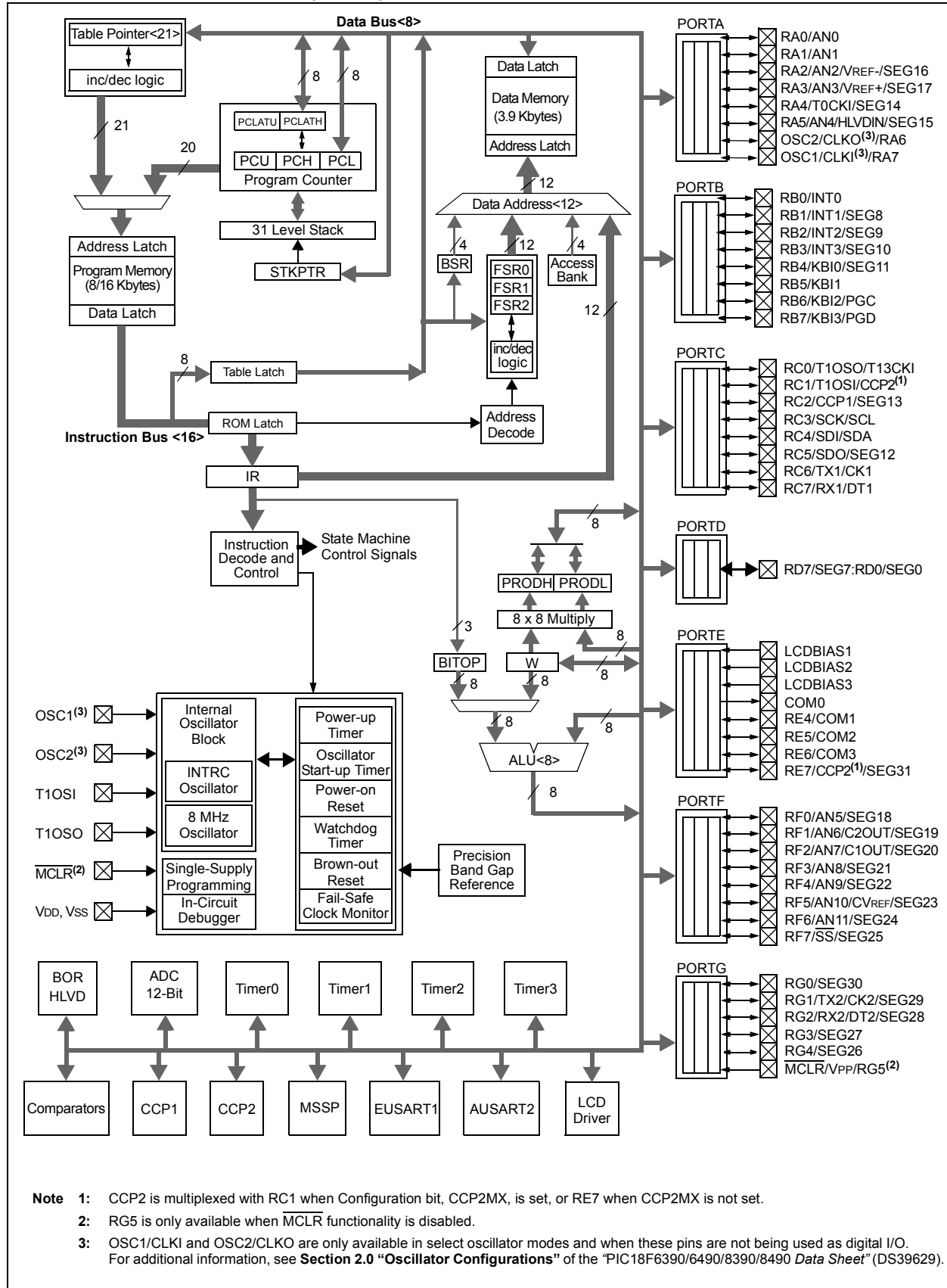
All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F6393/6493/8393/8493 family are available as both standard and low-voltage devices. Standard devices with Flash memory, designated with an "F" in the part number (such as PIC18F6393), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF6490), function over an extended VDD range of 2.0V to 5.5V.

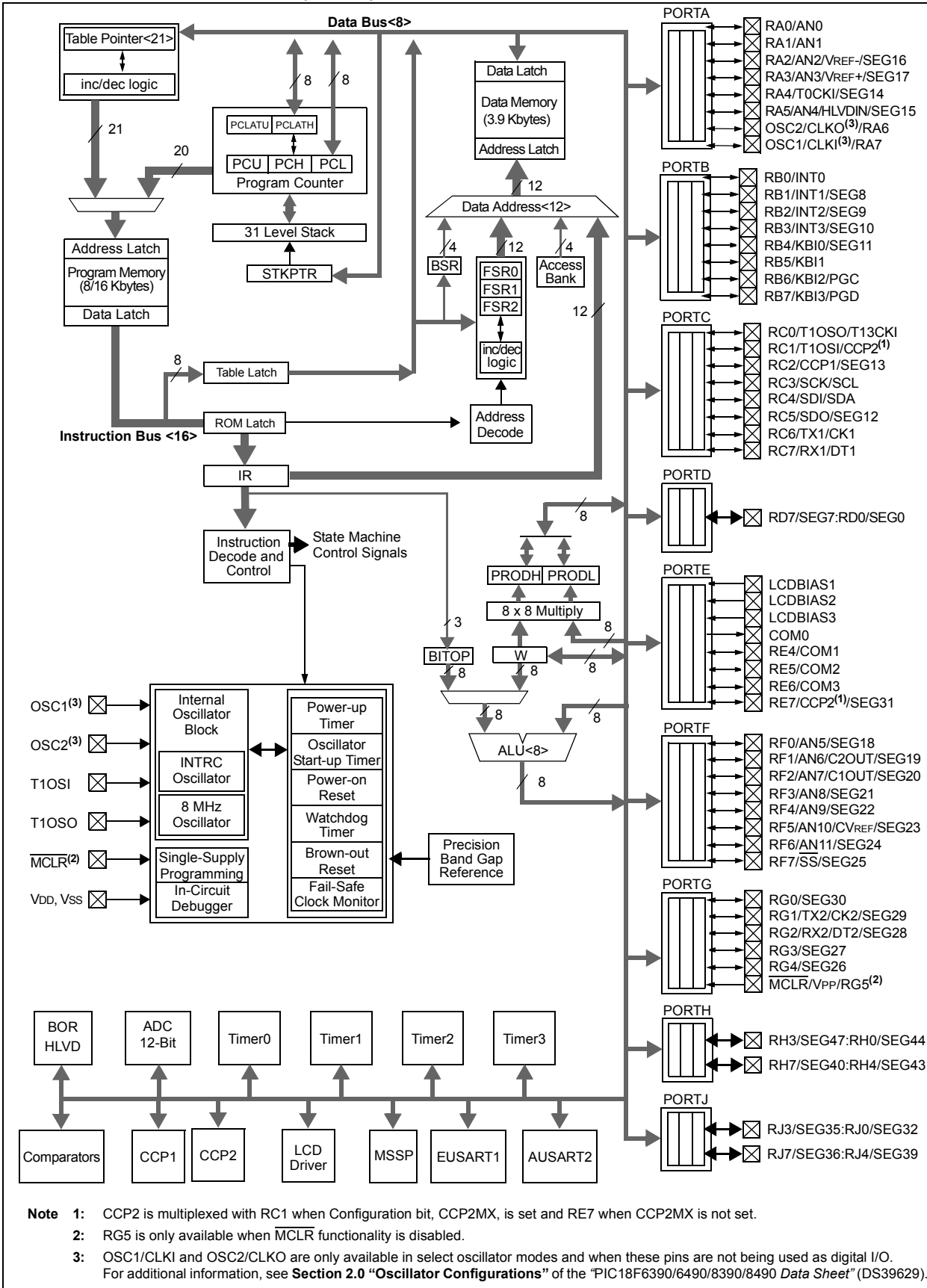
PIC18F6393/6493/8393/8493

FIGURE 1-1: PIC18F6X93 (64-PIN) BLOCK DIAGRAM



PIC18F6393/6493/8393/8493

FIGURE 1-2: PIC18F8X93 (80-PIN) BLOCK DIAGRAM



PIC18F6393/6493/8393/8493

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RA0/AN0	24	I/O	TTL	PORTA is a bidirectional I/O port.
RA0		I	Analog	Digital I/O.
AN0				Analog Input 0.
RA1/AN1	23	I/O	TTL	Digital I/O.
RA1		I	Analog	Analog Input 1.
AN1				
RA2/AN2/VREF-/SEG16	22	I/O	TTL	Digital I/O.
RA2		I	Analog	Analog Input 2.
AN2		I	Analog	A/D reference voltage (Low) input.
VREF-		I	Analog	SEG16 output for LCD.
SEG16		O	Analog	
RA3/AN3/VREF+/SEG17	21	I/O	TTL	Digital I/O.
RA3		I	Analog	Analog Input 3.
AN3		I	Analog	A/D reference voltage (High) input.
VREF+		I	Analog	SEG17 output for LCD.
SEG17		O	Analog	
RA4/T0CKI/SEG14	28	I/O	ST	Digital I/O.
RA4		I	ST	Timer0 external clock input.
T0CKI		I	ST	SEG14 output for LCD.
SEG14		O	Analog	
RA5/AN4/HLVDIN/SEG15	27	I/O	TTL	Digital I/O.
RA5		I	Analog	Analog Input 4.
AN4		I	Analog	Low-Voltage Detect input.
HLVDIN		I	Analog	SEG15 output for LCD.
SEG15		O	Analog	
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/SEG0 RD0 SEG0	58	I/O O	ST Analog	PORTD is a bidirectional I/O port. Digital I/O. SEG0 output for LCD.
RD1/SEG1 RD1 SEG1	55	I/O O	ST Analog	Digital I/O. SEG1 output for LCD.
RD2/SEG2 RD2 SEG2	54	I/O O	ST Analog	Digital I/O. SEG2 output for LCD.
RD3/SEG3 RD3 SEG3	53	I/O O	ST Analog	Digital I/O. SEG3 output for LCD.
RD4/SEG4 RD4 SEG4	52	I/O O	ST Analog	Digital I/O. SEG4 output for LCD.
RD5/SEG5 RD5 SEG5	51	I/O O	ST Analog	Digital I/O. SEG5 output for LCD.
RD6/SEG6 RD6 SEG6	50	I/O O	ST Analog	Digital I/O. SEG6 output for LCD.
RD7/SEG7 RD7 SEG7	49	I/O O	ST Analog	Digital I/O. SEG7 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
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2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	36			PORTC is a bidirectional I/O port.
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	35			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2 ⁽¹⁾		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/SEG13	43			
RC2		I/O	ST	Digital I/O.
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
SEG13		O	Analog	SEG13 output for LCD.
RC3/SCK/SCL	44			
RC3		I/O	ST	Digital I/O.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL		I/O	I ² C	Synchronous serial clock input/output for I ² C™ mode.
RC4/SDI/SDA	45			
RC4		I/O	ST	Digital I/O.
SDI		I	ST	SPI data in.
SDA		I/O	I ² C	I ² C data I/O.
RC5/SDO/SEG12	46			
RC5		I/O	ST	Digital I/O.
SDO		O	—	SPI data out.
SEG12		O	Analog	SEG12 output for LCD.
RC6/TX1/CK1	37			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	38			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
LCDBIAS1 LCDBIAS1	4	I	Analog	BIAS1 input for LCD.
LCDBIAS2 LCDBIAS2	3	I	Analog	BIAS2 input for LCD.
LCDBIAS3 LCDBIAS3	78	I	Analog	BIAS3 input for LCD.
COM0 COM0	77	O	Analog	COM0 output for LCD.
RE4/COM1 RE4 COM1	76	I/O O	ST Analog	Digital I/O. COM1 output for LCD.
RE5/COM2 RE5 COM2	75	I/O O	ST Analog	Digital I/O. COM2 output for LCD.
RE6/COM3 RE6 COM3	74	I/O O	ST Analog	Digital I/O. COM3 output for LCD.
RE7/CCP2/SEG31 RE7 CCP2 ⁽²⁾ SEG31	73	I/O I/O O	ST ST Analog	Digital I/O. Capture 2 input/Compare 2 output/PWM2 output. SEG31 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

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2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/SEG30 RG0 SEG30	5	I/O O	ST Analog	PORTG is a bidirectional I/O port. Digital I/O. SEG30 output for LCD.
RG1/TX2/CK2/SEG29 RG1 TX2 CK2 SEG29	6	I/O O I/O O	ST — ST Analog	Digital I/O. AUSART2 asynchronous transmit. AUSART2 synchronous clock (see related RX2/DT2). SEG29 output for LCD.
RG2/RX2/DT2/SEG28 RG2 RX2 DT2 SEG28	7	I/O I I/O O	ST ST ST Analog	Digital I/O. AUSART2 asynchronous receive. AUSART2 synchronous data (see related TX2/CK2). SEG28 output for LCD.
RG3/SEG27 RG3 SEG27	8	I/O O	ST Analog	Digital I/O. SEG27 output for LCD.
RG4/SEG26 RG4 SEG26	10	I/O O	ST Analog	Digital I/O. SEG26 output for LCD.
RG5				See $\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$ pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RH0/SEG47 RH0 SEG47	79	I/O O	ST Analog	PORTH is a bidirectional I/O port. Digital I/O. SEG47 output for LCD.
RH1/SEG46 RH1 SEG46	80	I/O O	ST Analog	Digital I/O. SEG46 output for LCD.
RH2/SEG45 RH2 SEG45	1	I/O O	ST Analog	Digital I/O. SEG45 output for LCD.
RH3/SEG44 RH3 SEG44	2	I/O O	ST Analog	Digital I/O. SEG44 output for LCD.
RH4/SEG40 RH4 SEG40	22	I/O O	ST Analog	Digital I/O. SEG40 output for LCD.
RH5/SEG41 RH5 SEG41	21	I/O O	ST Analog	Digital I/O. SEG41 output for LCD.
RH6/SEG42 RH6 SEG42	20	I/O O	ST Analog	Digital I/O. SEG42 output for LCD.
RH7/SEG43 RH7 SEG43	19	I/O O	ST Analog	Digital I/O. SEG43 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6

Unimplemented: Read as '0'

bit 5-4

VCFG<1:0>: Voltage Reference Configuration bits

	A/D VREF+	A/D VREF-
00	AVDD	AVss
01	External VREF+	AVss
10	AVDD	External VREF-
11	External VREF+	External VREF-

bit 3-0

PCFG<3:0>: A/D Port Configuration Control bits

PCFG<3:0>	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A
0011	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

D = Digital I/O

PIC18F6393/6493/8393/8493

REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified

0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits

111 = 20 TAD

110 = 16 TAD

101 = 12 TAD

100 = 8 TAD

011 = 6 TAD

010 = 4 TAD

001 = 2 TAD

000 = 0 TAD⁽¹⁾

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)⁽¹⁾

110 = FOSC/64

101 = FOSC/16

100 = FOSC/4

011 = FRC (clock derived from A/D RC oscillator)⁽¹⁾

010 = FOSC/32

001 = FOSC/8

000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one T_{CY} (instruction cycle) is added before the A/D clock starts. This allows the *SLEEP* instruction to be executed before starting a conversion.

PIC18F6393/6493/8393/8493

The analog reference voltage is software-selectable to either the device's positive and negative supply voltage (AVDD and AVSS), or the voltage level on the RA3/AN3/VREF+/SEG17 and RA2/AN2/VREF-/SEG16 pins.

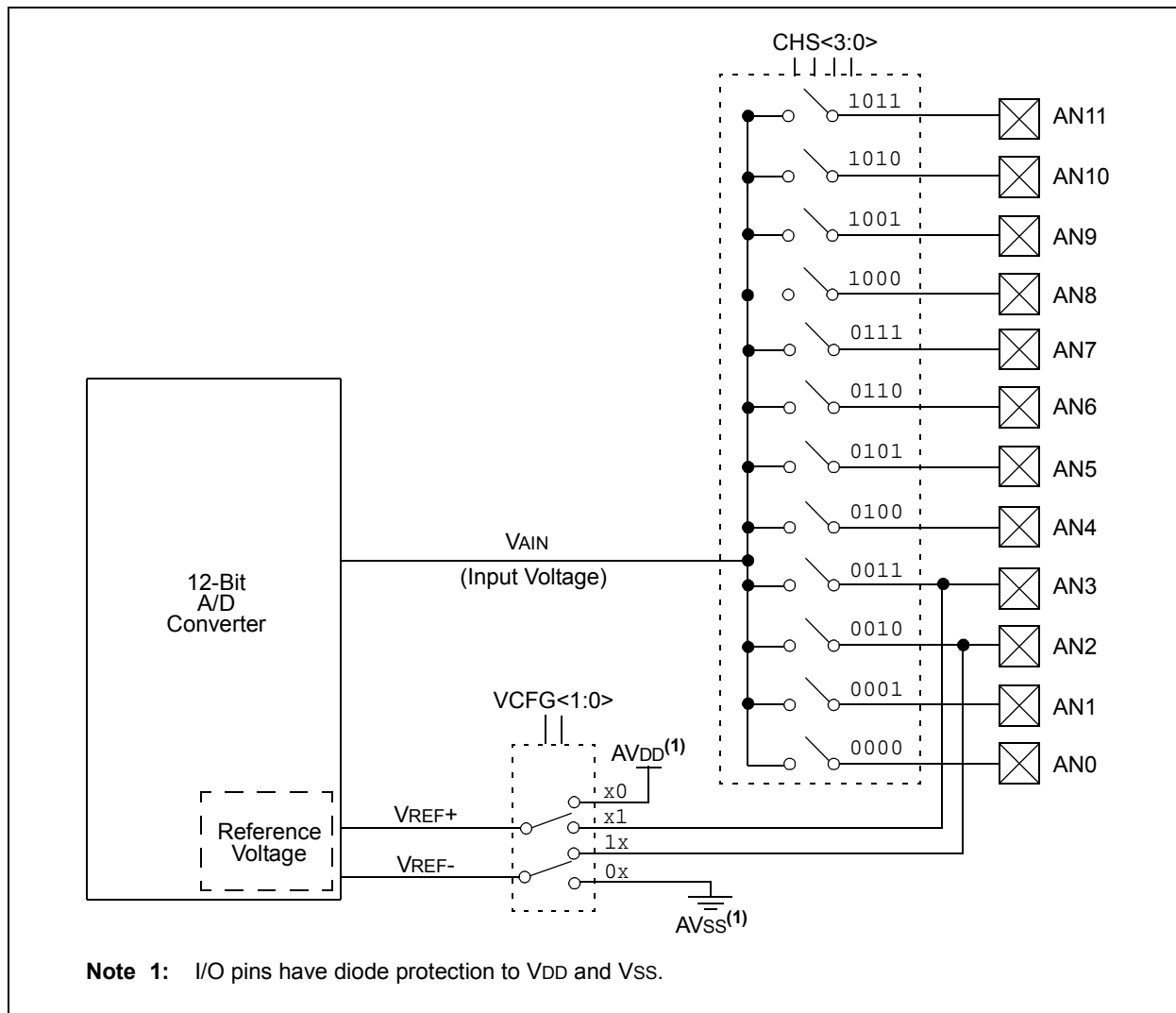
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

FIGURE 2-1: A/D BLOCK DIAGRAM



2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT<2:0> bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT<2:0> = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software-selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (See parameter 130 for more information.)

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 μ s
Operation	ADCS<2:0>	Maximum Fosc
2 TOSC	000	2.5 MHz
4 TOSC	100	5 MHz
8 TOSC	001	10 MHz
16 TOSC	101	20 MHz
32 TOSC	010	40 MHz
64 TOSC	110	40 MHz
RC ⁽¹⁾	x11	1 MHz ⁽²⁾

Note 1: The RC source has a typical TAD time of 2.5 μ s.

2: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a Fosc divider should be used instead; otherwise, the A/D accuracy specification may not be met.

2.4 Operation in Power-Managed Modes

If the A/D is expected to operate while the device is in a power-managed mode, the ACQT<2:0> and ADCS<2:0> bits in ADCON2 should be updated in accordance with the clock source to be used in that mode. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits, ACQT<2:0>, are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the *SLEEP* instruction, and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

Note 1: When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.

2: Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

PIC18F6393/6493/8393/8493

TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F6393/6493/8393/8493 (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
A01	NR	Resolution	—	—	12	bit	$\Delta V_{REF} \geq 3.0V$
A03	EIL	Integral Linearity Error	—	$<\pm 1$	± 2.0	LSB	$V_{DD} = 3.0V$
			—	—	± 2.0	LSB	$V_{DD} = 5.0V$
A04	EDL	Differential Linearity Error	—	$<\pm 1$	$+1.5/-1.0$	LSB	$V_{DD} = 3.0V$
			—	—	$+1.5/-1.0$	LSB	$V_{DD} = 5.0V$
A06	EOFF	Offset Error	—	$<\pm 1$	± 5	LSB	$V_{DD} = 3.0V$
			—	—	± 3	LSB	$V_{DD} = 5.0V$
A07	EGN	Gain Error	—	$<\pm 1$	± 2.00	LSB	$V_{DD} = 3.0V$
			—	—	± 2.00	LSB	$V_{DD} = 5.0V$
A10	—	Monotonicity	Guaranteed ⁽¹⁾			—	$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	ΔV_{REF}	Reference Voltage Range ($V_{REFH} - V_{REFL}$)	3	—	$V_{DD} - V_{SS}$	V	For 12-bit resolution
A21	V_{REFH}	Reference Voltage High	$V_{SS} + \Delta V_{REF}$	—	V_{DD}	V	For 12-bit resolution
A22	V_{REFL}	Reference Voltage Low	V_{SS}	—	$V_{DD} - \Delta V_{REF}$	V	For 12-bit resolution
A25	V_{AIN}	Analog Input Voltage	V_{REFL}	—	V_{REFH}	V	
A30	Z_{AIN}	Recommended Impedance of Analog Voltage Source	—	—	2.5	k Ω	
A50	I _{REF}	V _{REF} Input Current ⁽²⁾	—	—	5	μA	During V _{AIN} acquisition. During A/D conversion cycle.
			—	—	150	μA	

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

Note 2: V_{REFH} current is from the RA3/AN3/ V_{REF+} /SEG17 pin or V_{DD} , whichever is selected as the V_{REFH} source. V_{REFL} current is from the RA2/AN2/ V_{REF-} /SEG16 pin or V_{SS} , whichever is selected as the V_{REFL} source.

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

INDEX

A

A/D	31
A/D Converter Interrupt, Configuring	35
Acquisition Requirements	36
ADCON0 Register	31
ADCON1 Register	31
ADCON2 Register	31
ADRESH Register	31, 34
ADRESL Register	31
Analog Port Pins, Configuring	38
Associated Registers	40
Configuring the Module	35
Conversion Clock (TAD)	37
Conversion Requirements	46
Conversion Status (GO/DONE Bit)	34
Conversions	39
Converter Characteristics	45
Discharge	39
Operation in Power-Managed Modes	38
Selecting and Configuring Acquisition Time	37
Special Event Trigger (ECCP2)	40
Transfer Function	35
Use of the ECCP2 Trigger	40
Absolute Maximum Ratings	43
ADCON0 Register	31
GO/DONE Bit	34
ADCON1 Register	31
ADCON2 Register	31
ADRESH Register	31
ADRESL Register	31, 34
Analog-to-Digital Converter. See A/D.	

B

Block Diagrams	
A/D	34
Analog Input Model	35
PIC18F6X93 (64-Pin)	11
PIC18F8X93 (80-Pin)	12

C

Compare (ECCP2 Module)	
Special Event Trigger	40
Conversion Considerations	54
Customer Change Notification Service	59
Customer Notification Service	59
Customer Support	59

D

Device Differences	53
Device ID Registers	41
Device Overview	9
Details of Individual Devices	9
Features (table)	10
Special Features	9
Documentation	
Most Current Versions	7
Related Data Sheet	9

E

Electrical Characteristics	43
A/D Converter	45
Absolute Maximum Ratings	43
Low-Power Voltage-Frequency Graph	44
Voltage-Frequency Graph	44
Equations	
A/D Acquisition Time	36
A/D Minimum Charging Time	36
Calculating the Minimum Required Acquisition Time	36
Errata	7

I

Internet Address	59
Interrupt Sources	
A/D Conversion Complete	35

L

LCD Driver	
Features	3

M

Microchip Internet Web Site	59
Microcontroller	
Special Features	3
Migration from Baseline to Enhanced Devices	54
Migration from High-End to Enhanced Devices	55
Migration from Mid-Range to Enhanced Devices	55

O

Oscillator Structure	
Features	3

P

Packaging	
Information	47
Marking	47
Peripheral Highlights	3
Pin Diagrams	
64-Pin TQFP	4
80-Pin TQFP	5
Pin Functions	
AVDD	30
AVDD	20
AVss	20
AVss	30
COM0	18, 26
LCDBIAS1	18, 26
LCDBIAS2	18, 26
LCDBIAS3	18, 26
MCLR/VPP/RG5	13, 21
OSC1/CLKI/RA7	13, 21
OSC2/CLKO/RA6	13, 21
RA0/AN0	14, 22
RA1/AN1	14, 22
RA2/AN2/VREF-/SEG16	14, 22

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