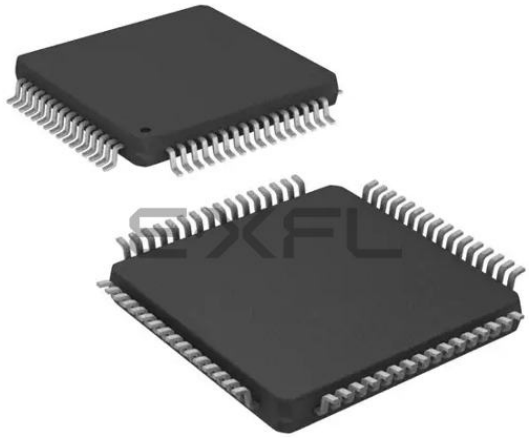

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f6493-i-pt

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PIC18F6393/6493/8393/8493

64/80-Pin High-Performance, Flash Microcontrollers with LCD Driver, 12-Bit ADC and nanoWatt Technology

LCD Driver Module Features:

- Direct Driving of LCD Panel
- Up to 192 Pixels: Software-Selectable
- Programmable LCD Timing module:
  - Multiple LCD timing sources available
  - Up to four commons: Static, 1/2, 1/3 or 1/4 multiplex
  - Static, 1/2 or 1/3 bias configuration
- Can Drive LCD Panel while in Sleep mode for Low-Power Operation

Power-Managed Modes:

- Run: CPU On, Peripherals On
- Idle: CPU Off, Peripherals On
- Sleep: CPU Off, Peripherals Off
- Ultra Low 50 nA Input Leakage
- Run mode Current Down to 14 μA Typical
- Idle mode Currents Down to 2.3 μA Typical
- Sleep mode Currents Down to 0.1 μA Typical
- Timer1 Oscillator: 1.0 μA, 32 kHz, 2V Typical
- Watchdog Timer: 1.7 μA Typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (available for crystal and internal oscillators)
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal Oscillator Block:
  - Fast wake from Sleep and Idle, 1 μs typical
  - Eight selectable frequencies, from 31 kHz to 8 MHz
  - Provides a complete range of clock speeds from 31 kHz to 32 MHz when used with PLL
  - User-tunable to compensate for frequency drift
- Secondary Oscillator Using Timer1 at 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops

Peripheral Highlights:

- 12-Bit, up to 12-Channel Analog-to-Digital (A/D) Converter module:
  - Auto-acquisition capability
  - Conversion available during Sleep
- High-Current Sink/Source 25 mA/25 mA
- Four External Interrupts
- Four Input Change Interrupts
- Four 8-Bit/16-Bit Timer/Counter modules
- Real-Time Clock (RTC) Software module:
  - Configurable 24-hour clock, calendar, automatic 100-year or 12,800-year, day-of-week calculator
  - Uses Timer1
- Up to Two Capture/Compare/PWM (CCP) modules
- Master Synchronous Serial Port (MSSP) module Supporting Three-Wire SPI (all four modes) and I^2C™ Master and Slave modes
- Addressable USART module:
  - Supports RS-485 and RS-232
- Enhanced Addressable USART module:
  - Supports RS-485, RS-232 and LIN/J2602
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing
- Programmable 16-Level High/Low-Voltage Detection (HLVD) module:
  - Supports interrupt on High/Low-Voltage Detection

Special Microcontroller Features:

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 1000 Erase/Write Cycle Flash Program Memory, Typical
- Flash Retention: 100 Years Typical
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 132s
  - 2% stability over V_{DD} and temperature
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V
- Programmable Brown-out Reset (BOR) with Software Enable Option

Note: This document is supplemented by the *"PIC18F6390/6490/8390/8490 Data Sheet"* (DS39629). See **Section 1.0 "Device Overview"**.

Device	Program Memory		Data Memory	I/O	LCD (pixel)	12-Bit A/D (channels)	CCP (PWM)	MSSP		EUSART/ AUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)					SPI	Master I^2C™			
PIC18F6393	8K	4096	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F6493	16K	8192	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F8393	8K	4096	768	66	192	12	2	Y	Y	1/1	2	1/3
PIC18F8493	16K	8192	768	66	192	12	2	Y	Y	1/1	2	1/3

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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NOTES:

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6393
- PIC18F6493
- PIC18F8393
- PIC18F8493

Note: This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F6390/6490/8390/8490 devices. For information on the features and specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the *"*PIC18F6390/6490/8390/8490 *Data Sheet"* (DS39629).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price. In addition to these features, the PIC18F6393/6493/8393/8493 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

1.1 Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduces code overhead.

1.2 Details on Individual Family Members

Devices in the PIC18F6393/6493/8393/8493 family are available in 64-pin (PIC18F6X93) and 80-pin (PIC18F8X93) packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2, respectively.

The devices are differentiated from each other in the following ways:

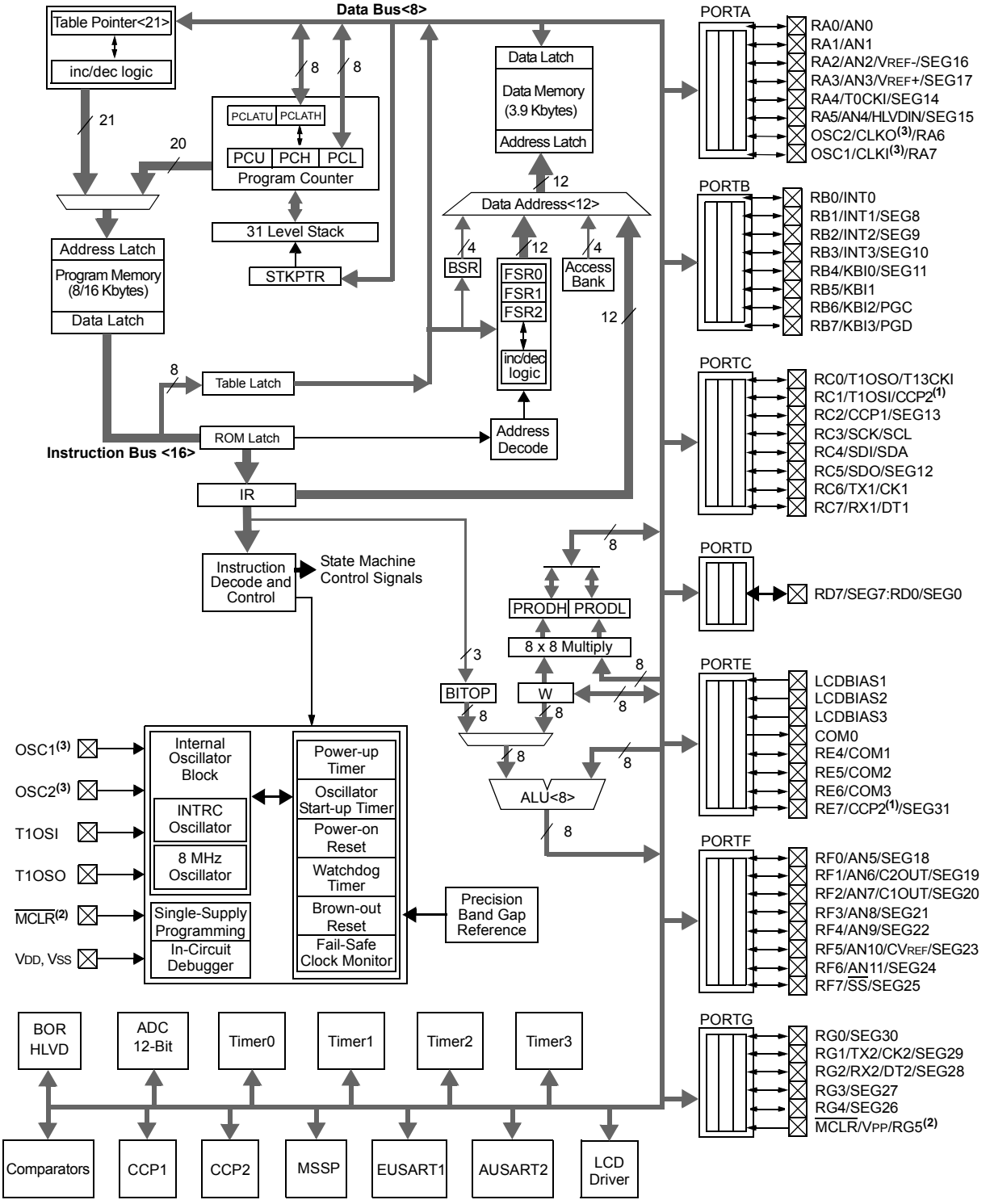
- I/O Ports:
  - 64-pin devices – 7 bidirectional ports
  - 80-pin devices – 9 bidirectional ports
- LCD Pixels:
  - 64-pin devices – 128 (32 SEGs x 4 COMs) pixels can be driven
  - 80-pin devices – 192 (48 SEGs x 4 COMs) pixels can be driven
- Flash Program Memory:
  - PIC18FX393 devices – 8 Kbytes
  - PIC18FX493 devices – 16 Kbytes

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F6393/6493/8393/8493 family are available as both standard and low-voltage devices. Standard devices with Flash memory, designated with an "F" in the part number (such as PIC18F6393), accommodate an operating V_{DD} range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF6490), function over an extended V_{DD} range of 2.0V to 5.5V.

FIGURE 1-1: PIC18F6X93 (64-PIN) BLOCK DIAGRAM



Note 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set, or RE7 when CCP2MX is not set.

2: RG5 is only available when MCLR functionality is disabled.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the "PIC18F6390/6490/8390/8490 *Data Sheet*" (DS39629).

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0	48			
RB0		I/O	TTL	Digital I/O.
INT0		I	ST	External Interrupt 0.
RB1/INT1/SEG8	47			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External Interrupt 1.
SEG8		O	Analog	SEG8 output for LCD.
RB2/INT2/SEG9	46			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External Interrupt 2.
SEG9		O	Analog	SEG9 output for LCD.
RB3/INT3/SEG10	45			
RB3		I/O	TTL	Digital I/O.
INT3		I	ST	External Interrupt 3.
SEG10		O	Analog	SEG10 output for LCD.
RB4/KBI0/SEG11	44			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
SEG11		O	Analog	SEG11 output for LCD.
RB5/KBI1	43			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
RB6/KBI2/PGC	42			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD	37			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C = ST with I^2C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTF is a bidirectional I/O port.
RF0/AN5/SEG18	18			
RF0		I/O	ST	Digital I/O.
AN5		I	Analog	Analog input 5.
SEG18		O	Analog	SEG18 output for LCD.
RF1/AN6/C2OUT/SEG19	17			
RF1		I/O	ST	Digital I/O.
AN6		I	Analog	Analog input 6.
C2OUT		O	—	Comparator 2 output.
SEG19		O	Analog	SEG19 output for LCD.
RF2/AN7/C1OUT/SEG20	16			
RF2		I/O	ST	Digital I/O.
AN7		I	Analog	Analog input 7.
C1OUT		O	—	Comparator 1 output.
SEG20		O	Analog	SEG20 output for LCD.
RF3/AN8/SEG21	15			
RF3		I/O	ST	Digital I/O.
AN8		I	Analog	Analog input 8.
SEG21		O	Analog	SEG21 output for LCD.
RF4/AN9/SEG22	14			
RF4		I/O	ST	Digital I/O.
AN9		I	Analog	Analog input 9.
SEG22		O	Analog	SEG22 output for LCD.
RF5/AN10/CVREF/SEG23	13			
RF5		I/O	ST	Digital I/O.
AN10		I	Analog	Analog input 10.
CVREF		O	Analog	Comparator reference voltage output.
SEG23		O	Analog	SEG23 output for LCD.
RF6/AN11/SEG24	12			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog input 11.
SEG24		O	Analog	SEG24 output for LCD.
RF7/$\overline{SS}$/SEG25	11			
RF7		I/O	ST	Digital I/O.
$\overline{SS}$		I	TTL	SPI™ slave select input.
SEG25		O	Analog	SEG25 output for LCD.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C = ST with I^2C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTG is a bidirectional I/O port.
RG0/SEG30	3			
RG0		I/O	ST	Digital I/O.
SEG30		O	Analog	SEG30 output for LCD.
RG1/TX2/CK2/SEG29	4			
RG1		I/O	ST	Digital I/O.
TX2		O	—	AUSART2 asynchronous transmit.
CK2		I/O	ST	AUSART2 synchronous clock (see related RX2/DT2).
SEG29		O	Analog	SEG29 output for LCD.
RG2/RX2/DT2/SEG28	5			
RG2		I/O	ST	Digital I/O.
RX2		I	ST	AUSART2 asynchronous receive.
DT2		I/O	ST	AUSART2 synchronous data (see related TX2/CK2).
SEG28		O	Analog	SEG28 output for LCD.
RG3/SEG27	6			
RG3		I/O	ST	Digital I/O.
SEG27		O	Analog	SEG27 output for LCD.
RG4/SEG26	8			
RG4		I/O	ST	Digital I/O.
SEG26		O	Analog	SEG26 output for LCD.
RG5				See $\overline{MCLR}$/VPP/RG5 pin.
VSS	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	10, 26, 38, 57	P	—	Positive supply for logic and I/O pins.
AVSS	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C = ST with I^2C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTA is a bidirectional I/O port.
RA0/AN0	30			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog Input 0.
RA1/AN1	29			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog Input 1.
RA2/AN2/VREF-/SEG16	28			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog Input 2.
VREF-		I	Analog	A/D reference voltage (Low) input.
SEG16		O	Analog	SEG16 output for LCD.
RA3/AN3/VREF+/SEG17	27			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog Input 3.
VREF+		I	Analog	A/D reference voltage (High) input.
SEG17		O	Analog	SEG17 output for LCD.
RA4/T0CKI/SEG14	34			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
SEG14		O	Analog	SEG14 output for LCD.
RA5/AN4/HLVDIN/SEG15	33			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog Input 4.
HLVDIN		I	Analog	Low-Voltage Detect input.
SEG15		O	Analog	SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C = ST with I^2C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTH is a bidirectional I/O port.
RH0/SEG47	79			
RH0		I/O	ST	Digital I/O.
SEG47		O	Analog	SEG47 output for LCD.
RH1/SEG46	80			
RH1		I/O	ST	Digital I/O.
SEG46		O	Analog	SEG46 output for LCD.
RH2/SEG45	1			
RH2		I/O	ST	Digital I/O.
SEG45		O	Analog	SEG45 output for LCD.
RH3/SEG44	2			
RH3		I/O	ST	Digital I/O.
SEG44		O	Analog	SEG44 output for LCD.
RH4/SEG40	22			
RH4		I/O	ST	Digital I/O.
SEG40		O	Analog	SEG40 output for LCD.
RH5/SEG41	21			
RH5		I/O	ST	Digital I/O.
SEG41		O	Analog	SEG41 output for LCD.
RH6/SEG42	20			
RH6		I/O	ST	Digital I/O.
SEG42		O	Analog	SEG42 output for LCD.
RH7/SEG43	19			
RH7		I/O	ST	Digital I/O.
SEG43		O	Analog	SEG43 output for LCD.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C = ST with I^2C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **VCFG<1:0>:** Voltage Reference Configuration bits

	A/D VREF+	**A/D VREF-**
00	AVDD	AVSS
01	External VREF+	AVSS
10	AVDD	External VREF-
11	External VREF+	External VREF-

bit 3-0 **PCFG<3:0>:** A/D Port Configuration Control bits

PCFG<3:0>	**AN11**	**AN10**	**AN9**	**AN8**	**AN7**	**AN6**	**AN5**	**AN4**	**AN3**	**AN2**	**AN1**	**AN0**
0000	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A
0011	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set and the ACQT<2:0> bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set, the ACQT<2:0> bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will *not* be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2 μs after enabling the A/D before beginning an acquisition and conversion cycle.

2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)

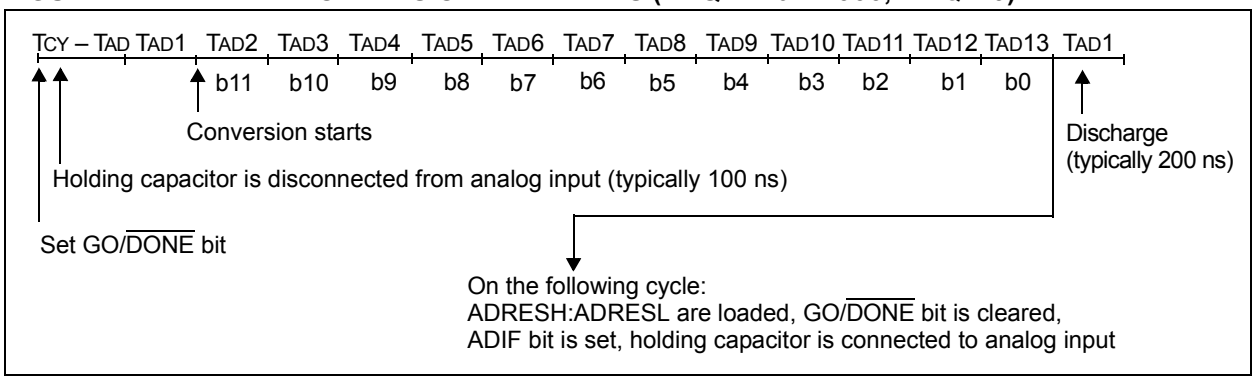
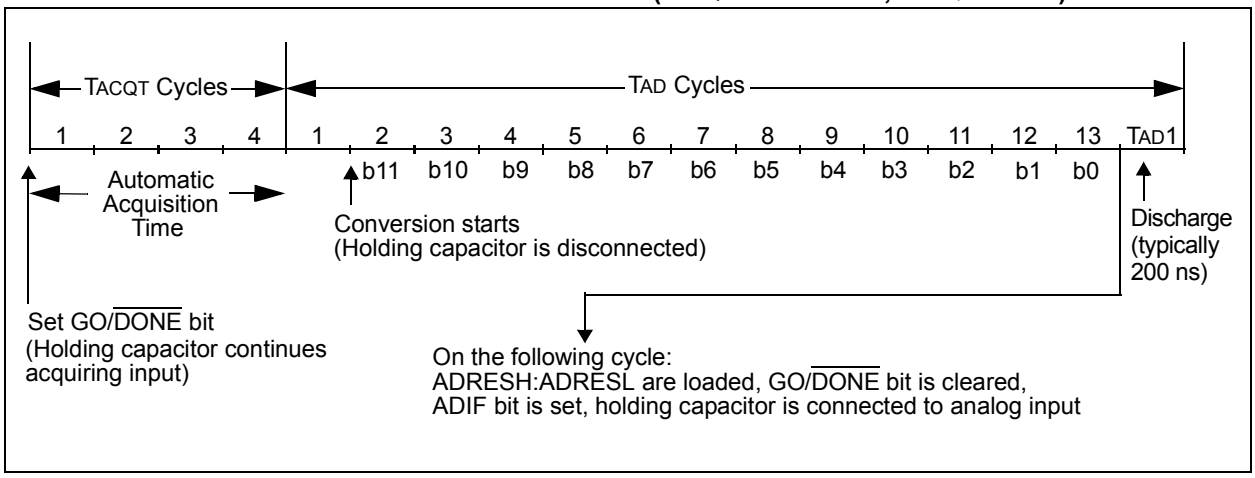


FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F6393/6493/8393/8493 DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-5 **DEV<2:0>:** Device ID bits
See Register 3-2 for a complete listing.

bit 4-0 **REV<4:0>:** Revision ID bits
These bits are used to indicate the device revision.

REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F6393/6493/8393/8493 DEVICES

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-0 **DEV10:DEV3:** Device ID bits

Device	DEV<10:3> (DEVID2<7:0>)	DEV<2:0> (DEVID1<7:5>)
PIC18F6393	0001 1010	000
PIC18F6493	0000 1110	000
PIC18F8393	0001 1010	001
PIC18F8493	0000 1110	001

4.0 ELECTRICAL CHARACTERISTICS

Note: Other than some basic data, this section documents only the PIC18F6393/6493/8393/8493 devices' specifications that differ from those of the PIC18F6390/6490/8390/8490 devices. For detailed information on the electrical specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the "PIC18F6390/6490/8390/8490 *Data Sheet"* (DS39629).

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.3V to (V_{DD} + 0.3V)

Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} **(Note 2)** ..... 0V to +13.25V

Total power dissipation **(Note 1)** 1.0W

Maximum current out of V_{SS} pin ..... 300 mA

Maximum current into V_{DD} pin ..... 250 mA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

Maximum current sunk by all ports ..... 200 mA

Maximum current sourced by all ports ..... 200 mA

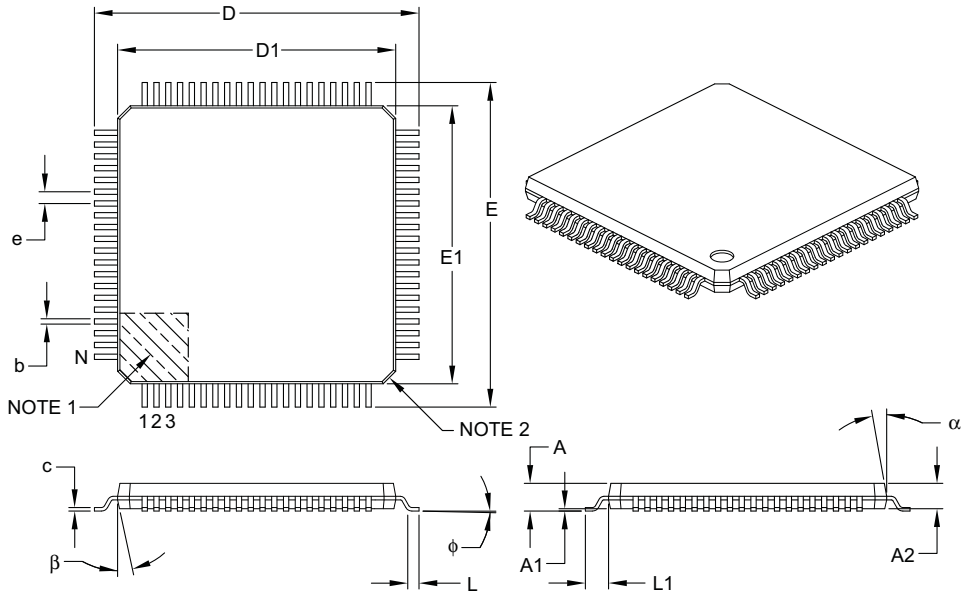
Note 1: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$/V_{PP}/RG5 pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$/V_{PP}/RG5 pin, rather than pulling this pin directly to V_{SS}.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

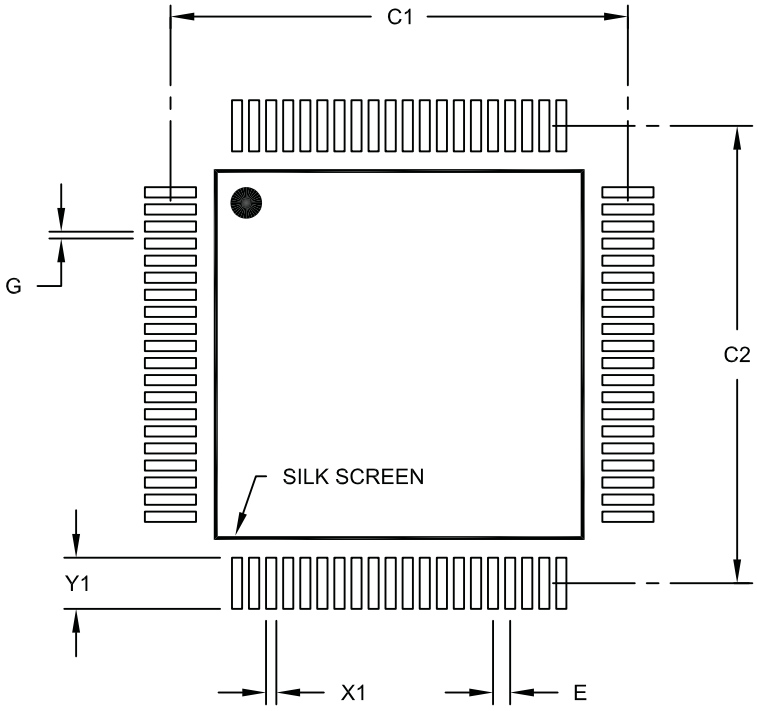
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X80)	X1			0.30
Contact Pad Length (X80)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2092A

NOTES: