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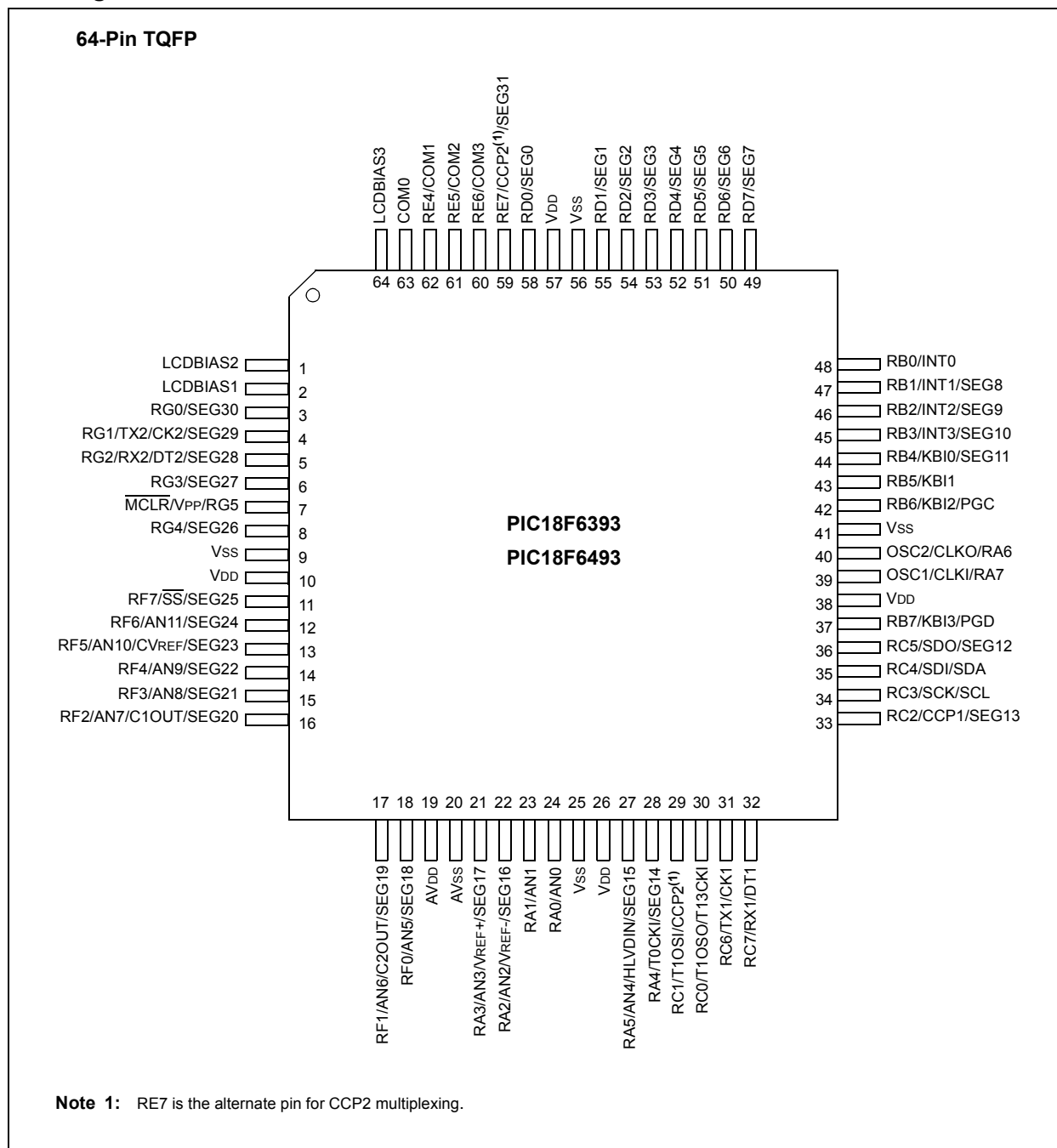
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, LCD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f8493-i-pt

PIC18F6393/6493/8393/8493

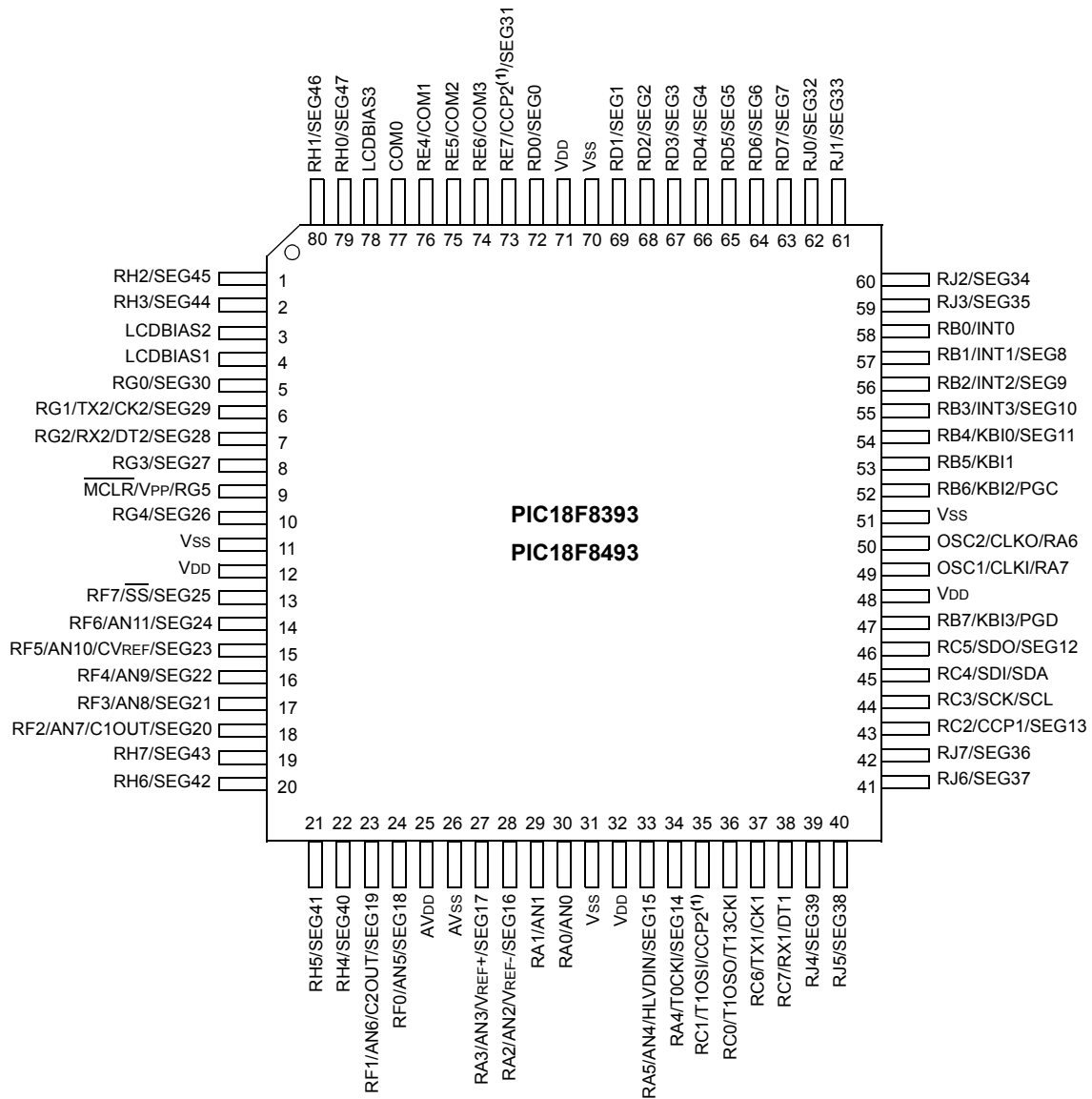
Pin Diagrams



PIC18F6393/6493/8393/8493

Pin Diagrams (Continued)

80-Pin TQFP



Note 1: RE7 is the alternate pin for CCP2 multiplexing.

PIC18F6393/6493/8393/8493

NOTES:

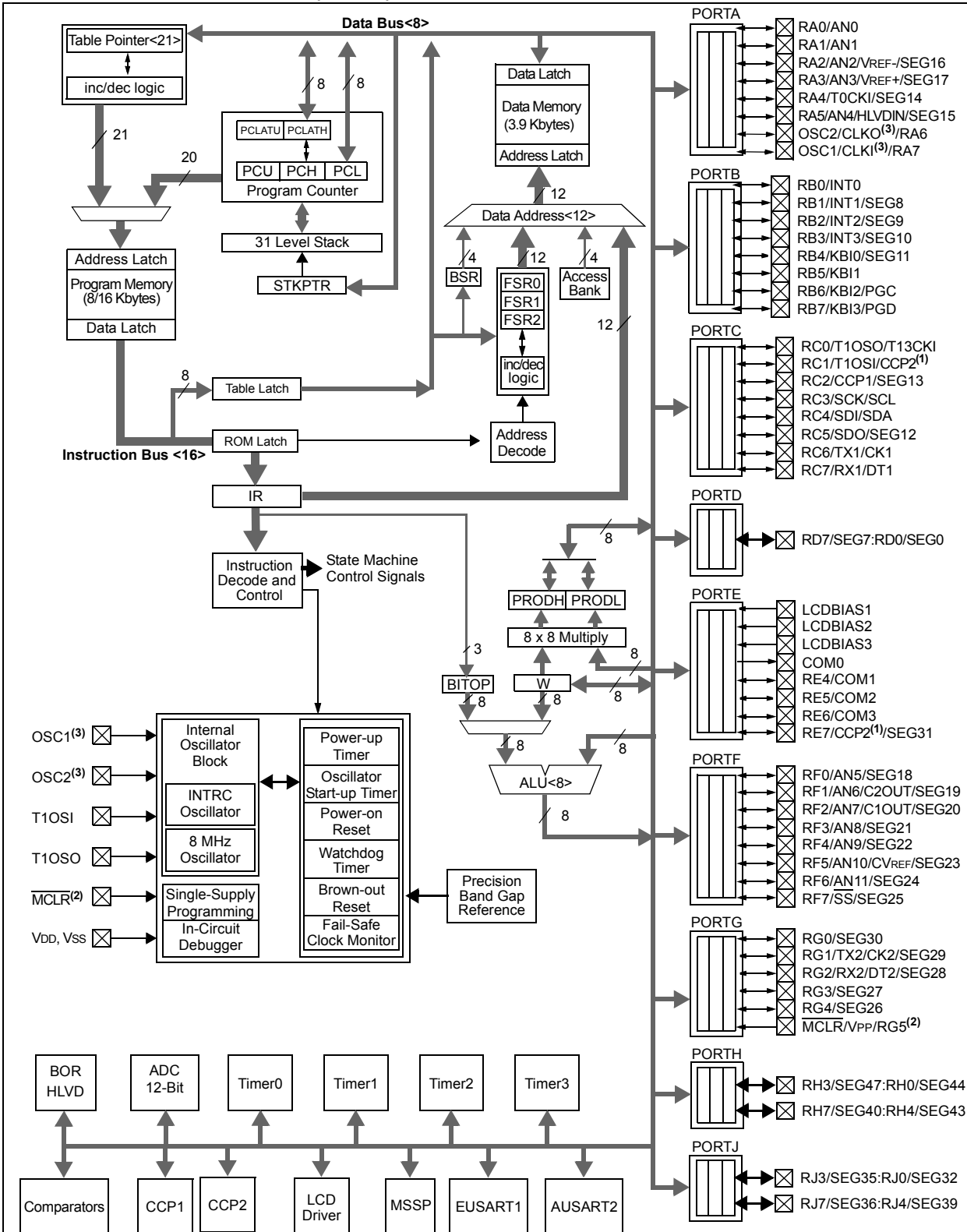
PIC18F6393/6493/8393/8493

TABLE 1-1: DEVICE FEATURES

Features	PIC18F6393	PIC18F6493	PIC18F8393	PIC18F8493
Operating Frequency	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	8K	16K	8K	16K
Program Memory (Instructions)	4096	8192	4096	8192
Data Memory (Bytes)	768	768	768	768
Interrupt Sources	22	22	22	22
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Number of Pixels the LCD Driver Can Drive	128 (32 SEGs x 4 COMs)	128 (32 SEGs x 4 COMs)	192 (48 SEGs x 4 COMs)	192 (48 SEGs x 4 COMs)
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART
12-Bit Analog-to-Digital Module	12 Input Channels	12 Input Channels	12 Input Channels	12 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

PIC18F6393/6493/8393/8493

FIGURE 1-2: PIC18F8X93 (80-PIN) BLOCK DIAGRAM



- Note**
- 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set and RE7 when CCP2MX is not set.
 - 2: RG5 is only available when MCLR functionality is disabled.
 - 3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see Section 2.0 "Oscillator Configurations" of the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).

PIC18F6393/6493/8393/8493

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RA0/AN0	24	I/O	TTL	PORTA is a bidirectional I/O port.
RA0		I	Analog	Digital I/O.
AN0				Analog Input 0.
RA1/AN1	23	I/O	TTL	Digital I/O.
RA1		I	Analog	Analog Input 1.
AN1				
RA2/AN2/VREF-/SEG16	22	I/O	TTL	Digital I/O.
RA2		I	Analog	Analog Input 2.
AN2		I	Analog	A/D reference voltage (Low) input.
VREF-		I	Analog	SEG16 output for LCD.
SEG16		O	Analog	
RA3/AN3/VREF+/SEG17	21	I/O	TTL	Digital I/O.
RA3		I	Analog	Analog Input 3.
AN3		I	Analog	A/D reference voltage (High) input.
VREF+		I	Analog	SEG17 output for LCD.
SEG17		O	Analog	
RA4/T0CKI/SEG14	28	I/O	ST	Digital I/O.
RA4		I	ST	Timer0 external clock input.
T0CKI		I	ST	SEG14 output for LCD.
SEG14		O	Analog	
RA5/AN4/HLVDIN/SEG15	27	I/O	TTL	Digital I/O.
RA5		I	Analog	Analog Input 4.
AN4		I	Analog	Low-Voltage Detect input.
HLVDIN		I	Analog	SEG15 output for LCD.
SEG15		O	Analog	
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/SEG0 RD0 SEG0	58	I/O O	ST Analog	PORTD is a bidirectional I/O port. Digital I/O. SEG0 output for LCD.
RD1/SEG1 RD1 SEG1	55	I/O O	ST Analog	Digital I/O. SEG1 output for LCD.
RD2/SEG2 RD2 SEG2	54	I/O O	ST Analog	Digital I/O. SEG2 output for LCD.
RD3/SEG3 RD3 SEG3	53	I/O O	ST Analog	Digital I/O. SEG3 output for LCD.
RD4/SEG4 RD4 SEG4	52	I/O O	ST Analog	Digital I/O. SEG4 output for LCD.
RD5/SEG5 RD5 SEG5	51	I/O O	ST Analog	Digital I/O. SEG5 output for LCD.
RD6/SEG6 RD6 SEG6	50	I/O O	ST Analog	Digital I/O. SEG6 output for LCD.
RD7/SEG7 RD7 SEG7	49	I/O O	ST Analog	Digital I/O. SEG7 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/SEG30 RG0 SEG30	3	I/O O	ST Analog	PORTG is a bidirectional I/O port. Digital I/O. SEG30 output for LCD.
RG1/TX2/CK2/SEG29 RG1 TX2 CK2 SEG29	4	I/O O I/O O	ST — ST Analog	Digital I/O. AUSART2 asynchronous transmit. AUSART2 synchronous clock (see related RX2/DT2). SEG29 output for LCD.
RG2/RX2/DT2/SEG28 RG2 RX2 DT2 SEG28	5	I/O I I/O O	ST ST ST Analog	Digital I/O. AUSART2 asynchronous receive. AUSART2 synchronous data (see related TX2/CK2). SEG28 output for LCD.
RG3/SEG27 RG3 SEG27	6	I/O O	ST Analog	Digital I/O. SEG27 output for LCD.
RG4/SEG26 RG4 SEG26	8	I/O O	ST Analog	Digital I/O. SEG26 output for LCD.
RG5				See $\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$ pin.
Vss	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	10, 26, 38, 57	P	—	Positive supply for logic and I/O pins.
AVss	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0 RB0 INT0	58	I/O I	TTL ST	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. Digital I/O. External interrupt 0.
RB1/INT1/SEG8 RB1 INT1 SEG8	57	I/O I O	TTL ST Analog	Digital I/O. External interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9 RB2 INT2 SEG9	56	I/O I O	TTL ST Analog	Digital I/O. External interrupt 2. SEG9 output for LCD.
RB3/INT3/SEG10 RB3 INT3 SEG10	55	I/O I O	TTL ST Analog	Digital I/O. External interrupt 3. SEG10 output for LCD.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	54	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1 RB5 KBI1	53	I/O I	TTL TTL	Digital I/O. Interrupt-on-change pin.
RB6/KBI2/PGC RB6 KBI2 PGC	52	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	47	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

- Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RF0/AN5/SEG18	24	I/O	ST	PORTF is a bidirectional I/O port.
RF0		I	Analog	Digital I/O.
AN5		O	Analog	Analog Input 5.
SEG18		O	Analog	SEG18 output for LCD.
RF1/AN6/C2OUT/SEG19	23	I/O	ST	Digital I/O.
RF1		I	Analog	Analog Input 6.
AN6		O	—	Comparator 2 output.
C2OUT		O	Analog	SEG19 output for LCD.
SEG19		O	Analog	
RF2/AN7/C1OUT/SEG20	18	I/O	ST	Digital I/O.
RF2		I	Analog	Analog Input 7.
AN7		O	—	Comparator 1 output.
C1OUT		O	Analog	SEG20 output for LCD.
SEG20		O	Analog	
RF3/AN8/SEG21	17	I/O	ST	Digital I/O.
RF3		I	Analog	Analog Input 8.
AN8		O	Analog	SEG21 output for LCD.
SEG21		O	Analog	
RF4/AN9/SEG22	16	I/O	ST	Digital I/O.
RF4		I	Analog	Analog Input 9.
AN9		O	Analog	SEG22 output for LCD.
SEG22		O	Analog	
RF5/AN10/CVREF/SEG23	15	I/O	ST	Digital I/O.
RF5		I	Analog	Analog Input 10.
AN10		O	Analog	Comparator reference voltage output.
CVREF		O	Analog	SEG23 output for LCD.
SEG23		O	Analog	
RF6/AN11/SEG24	14	I/O	ST	Digital I/O.
RF6		I	Analog	Analog Input 11.
AN11		O	Analog	SEG24 output for LCD.
SEG24		O	Analog	
RF7/ $\overline{SS}$ /SEG25	13	I/O	ST	Digital I/O.
RF7		I	TTL	SPI slave select input.
$\overline{SS}$		O	Analog	SEG25 output for LCD.
SEG25		O	Analog	

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/SEG30 RG0 SEG30	5	I/O O	ST Analog	PORTG is a bidirectional I/O port. Digital I/O. SEG30 output for LCD.
RG1/TX2/CK2/SEG29 RG1 TX2 CK2 SEG29	6	I/O O I/O O	ST — ST Analog	Digital I/O. AUSART2 asynchronous transmit. AUSART2 synchronous clock (see related RX2/DT2). SEG29 output for LCD.
RG2/RX2/DT2/SEG28 RG2 RX2 DT2 SEG28	7	I/O I I/O O	ST ST ST Analog	Digital I/O. AUSART2 asynchronous receive. AUSART2 synchronous data (see related TX2/CK2). SEG28 output for LCD.
RG3/SEG27 RG3 SEG27	8	I/O O	ST Analog	Digital I/O. SEG27 output for LCD.
RG4/SEG26 RG4 SEG26	10	I/O O	ST Analog	Digital I/O. SEG26 output for LCD.
RG5				See $\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$ pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RJ0/SEG32 RJ0 SEG32	62	I/O O	ST Analog	PORTJ is a bidirectional I/O port. Digital I/O. SEG32 output for LCD.
RJ1/SEG33 RJ1 SEG33	61	I/O O	ST Analog	Digital I/O. SEG33 output for LCD.
RJ2/SEG34 RJ2 SEG34	60	I/O O	ST Analog	Digital I/O. SEG34 output for LCD.
RJ3/SEG35 RJ3 SEG35	59	I/O O	ST Analog	Digital I/O. SEG35 output for LCD.
RJ4/SEG39 RJ4 SEG39	39	I/O O	ST Analog	Digital I/O. SEG39 output for LCD.
RJ5/SEG38 RJ5 SEG38	40	I/O O	ST Analog	Digital I/O. SEG38 output for LCD.
RJ6/SEG37 RJ6 SEG37	41	I/O O	ST Analog	Digital I/O. SEG37 output for LCD.
RJ7/SEG36 RJ7 SEG36	42	I/O O	ST Analog	Digital I/O. SEG36 output for LCD.
Vss	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.
VDD	12, 32, 48, 71	P	—	Positive supply for logic and I/O pins.
AVss	26	P	—	Ground reference for analog modules.
AVDD	25	P	—	Positive supply for analog modules.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6

Unimplemented: Read as '0'

bit 5-4

VCFG<1:0>: Voltage Reference Configuration bits

	A/D VREF+	A/D VREF-
00	AVDD	AVss
01	External VREF+	AVss
10	AVDD	External VREF-
11	External VREF+	External VREF-

bit 3-0

PCFG<3:0>: A/D Port Configuration Control bits

PCFG<3:0>	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A
0011	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

D = Digital I/O

PIC18F6393/6493/8393/8493

The value in the ADRESH:ADRESL registers is unknown following Power-on and Brown-out Resets and is not affected by any other Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 “A/D Acquisition Requirements”**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D acquisition time (ADCON2)
 - Select A/D conversion clock (ADCON2)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
 - Set GO/DONE bit (ADCON0<1>)

5. Wait for A/D conversion to complete by either:
 - Polling for the GO/DONE bit to be cleared
 OR
 - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit, ADIF, if required.
7. For the next conversion, go to Step 1 or Step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

FIGURE 2-2: A/D TRANSFER FUNCTION

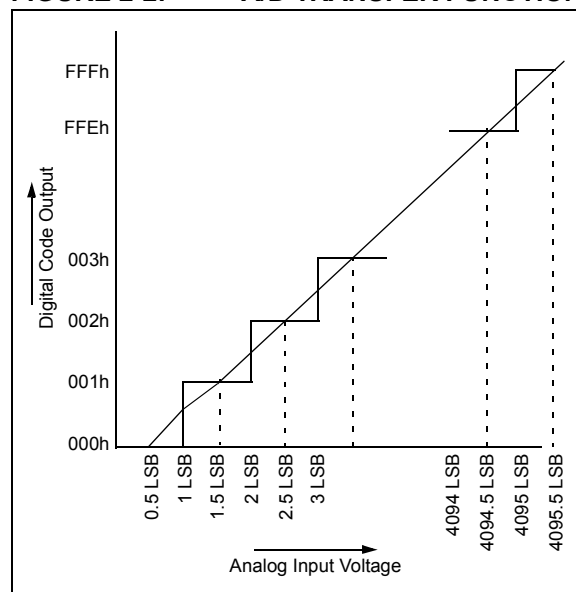
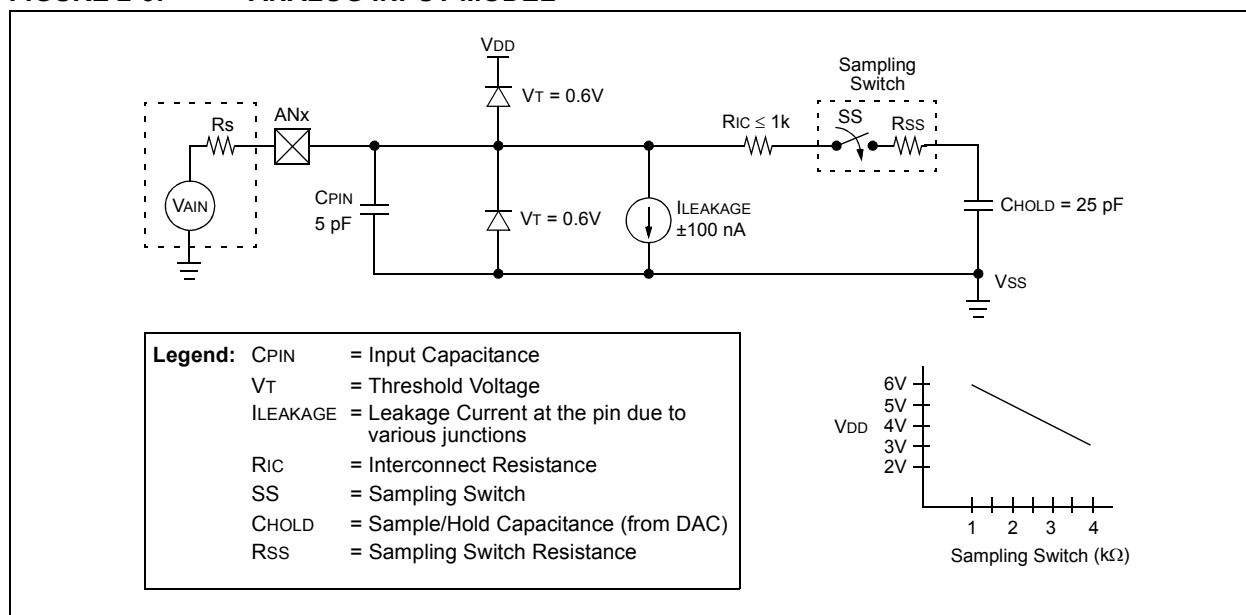


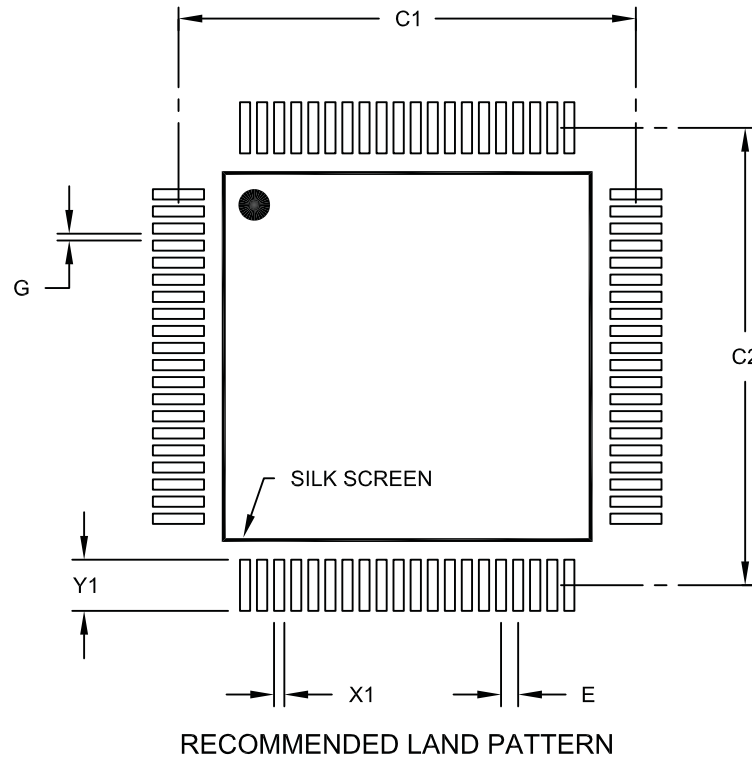
FIGURE 2-3: ANALOG INPUT MODEL



PIC18F6393/6493/8393/8493

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X80)	X1			0.30
Contact Pad Length (X80)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2092A

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

INDEX

A

A/D	31
A/D Converter Interrupt, Configuring	35
Acquisition Requirements	36
ADCON0 Register	31
ADCON1 Register	31
ADCON2 Register	31
ADRESH Register	31, 34
ADRESL Register	31
Analog Port Pins, Configuring	38
Associated Registers	40
Configuring the Module	35
Conversion Clock (TAD)	37
Conversion Requirements	46
Conversion Status (GO/DONE Bit)	34
Conversions	39
Converter Characteristics	45
Discharge	39
Operation in Power-Managed Modes	38
Selecting and Configuring Acquisition Time	37
Special Event Trigger (ECCP2)	40
Transfer Function	35
Use of the ECCP2 Trigger	40
Absolute Maximum Ratings	43
ADCON0 Register	31
GO/DONE Bit	34
ADCON1 Register	31
ADCON2 Register	31
ADRESH Register	31
ADRESL Register	31, 34
Analog-to-Digital Converter. See A/D.	

B

Block Diagrams	
A/D	34
Analog Input Model	35
PIC18F6X93 (64-Pin)	11
PIC18F8X93 (80-Pin)	12

C

Compare (ECCP2 Module)	
Special Event Trigger	40
Conversion Considerations	54
Customer Change Notification Service	59
Customer Notification Service	59
Customer Support	59

D

Device Differences	53
Device ID Registers	41
Device Overview	9
Details of Individual Devices	9
Features (table)	10
Special Features	9
Documentation	
Most Current Versions	7
Related Data Sheet	9

E

Electrical Characteristics	43
A/D Converter	45
Absolute Maximum Ratings	43
Low-Power Voltage-Frequency Graph	44
Voltage-Frequency Graph	44
Equations	
A/D Acquisition Time	36
A/D Minimum Charging Time	36
Calculating the Minimum Required Acquisition Time	36
Errata	7

I

Internet Address	59
Interrupt Sources	
A/D Conversion Complete	35

L

LCD Driver	
Features	3

M

Microchip Internet Web Site	59
Microcontroller	
Special Features	3
Migration from Baseline to Enhanced Devices	54
Migration from High-End to Enhanced Devices	55
Migration from Mid-Range to Enhanced Devices	55

O

Oscillator Structure	
Features	3

P

Packaging	
Information	47
Marking	47
Peripheral Highlights	3
Pin Diagrams	
64-Pin TQFP	4
80-Pin TQFP	5
Pin Functions	
AVDD	30
AVDD	20
AVss	20
AVss	30
COM0	18, 26
LCDBIAS1	18, 26
LCDBIAS2	18, 26
LCDBIAS3	18, 26
MCLR/VPP/RG5	13, 21
OSC1/CLKI/RA7	13, 21
OSC2/CLKO/RA6	13, 21
RA0/AN0	14, 22
RA1/AN1	14, 22
RA2/AN2/VREF-/SEG16	14, 22

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