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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf6493-i-pt

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**MICROCHIP****PIC18F6393/6493/8393/8493**

64/80-Pin High-Performance, Flash Microcontrollers with LCD Driver, 12-Bit ADC and nanoWatt Technology

LCD Driver Module Features:

- Direct Driving of LCD Panel
- Up to 192 Pixels: Software-Selectable
- Programmable LCD Timing module:
 - Multiple LCD timing sources available
 - Up to four commons: Static, 1/2, 1/3 or 1/4 multiplex
 - Static, 1/2 or 1/3 bias configuration
- Can Drive LCD Panel while in Sleep mode for Low-Power Operation

Power-Managed Modes:

- Run: CPU On, Peripherals On
- Idle: CPU Off, Peripherals On
- Sleep: CPU Off, Peripherals Off
- Ultra Low 50 nA Input Leakage
- Run mode Current Down to 14 μ A Typical
- Idle mode Currents Down to 2.3 μ A Typical
- Sleep mode Currents Down to 0.1 μ A Typical
- Timer1 Oscillator: 1.0 μ A, 32 kHz, 2V Typical
- Watchdog Timer: 1.7 μ A Typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (available for crystal and internal oscillators)
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal Oscillator Block:
 - Fast wake from Sleep and Idle, 1 μ s typical
 - Eight selectable frequencies, from 31 kHz to 8 MHz
 - Provides a complete range of clock speeds from 31 kHz to 32 MHz when used with PLL
 - User-tunable to compensate for frequency drift
- Secondary Oscillator Using Timer1 at 32 kHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if peripheral clock stops

Peripheral Highlights:

- 12-Bit, up to 12-Channel Analog-to-Digital (A/D) Converter module:
 - Auto-acquisition capability
 - Conversion available during Sleep
- High-Current Sink/Source 25 mA/25 mA
- Four External Interrupts
- Four Input Change Interrupts
- Four 8-Bit/16-Bit Timer/Counter modules
- Real-Time Clock (RTC) Software module:
 - Configurable 24-hour clock, calendar, automatic 100-year or 12,800-year, day-of-week calculator
 - Uses Timer1
- Up to Two Capture/Compare/PWM (CCP) modules
- Master Synchronous Serial Port (MSSP) module Supporting Three-Wire SPI (all four modes) and I²C™ Master and Slave modes
- Addressable USART module:
 - Supports RS-485 and RS-232
- Enhanced Addressable USART module:
 - Supports RS-485, RS-232 and LIN/J2602
 - Auto-wake-up on Start bit
 - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing
- Programmable 16-Level High/Low-Voltage Detection (HLVD) module:
 - Supports interrupt on High/Low-Voltage Detection

Special Microcontroller Features:

- C Compiler Optimized Architecture:
 - Optional extended instruction set designed to optimize re-entrant code
- 1000 Erase/Write Cycle Flash Program Memory, Typical
- Flash Retention: 100 Years Typical
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 132s
 - 2% stability over VDD and temperature
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V
- Programmable Brown-out Reset (BOR) with Software Enable Option

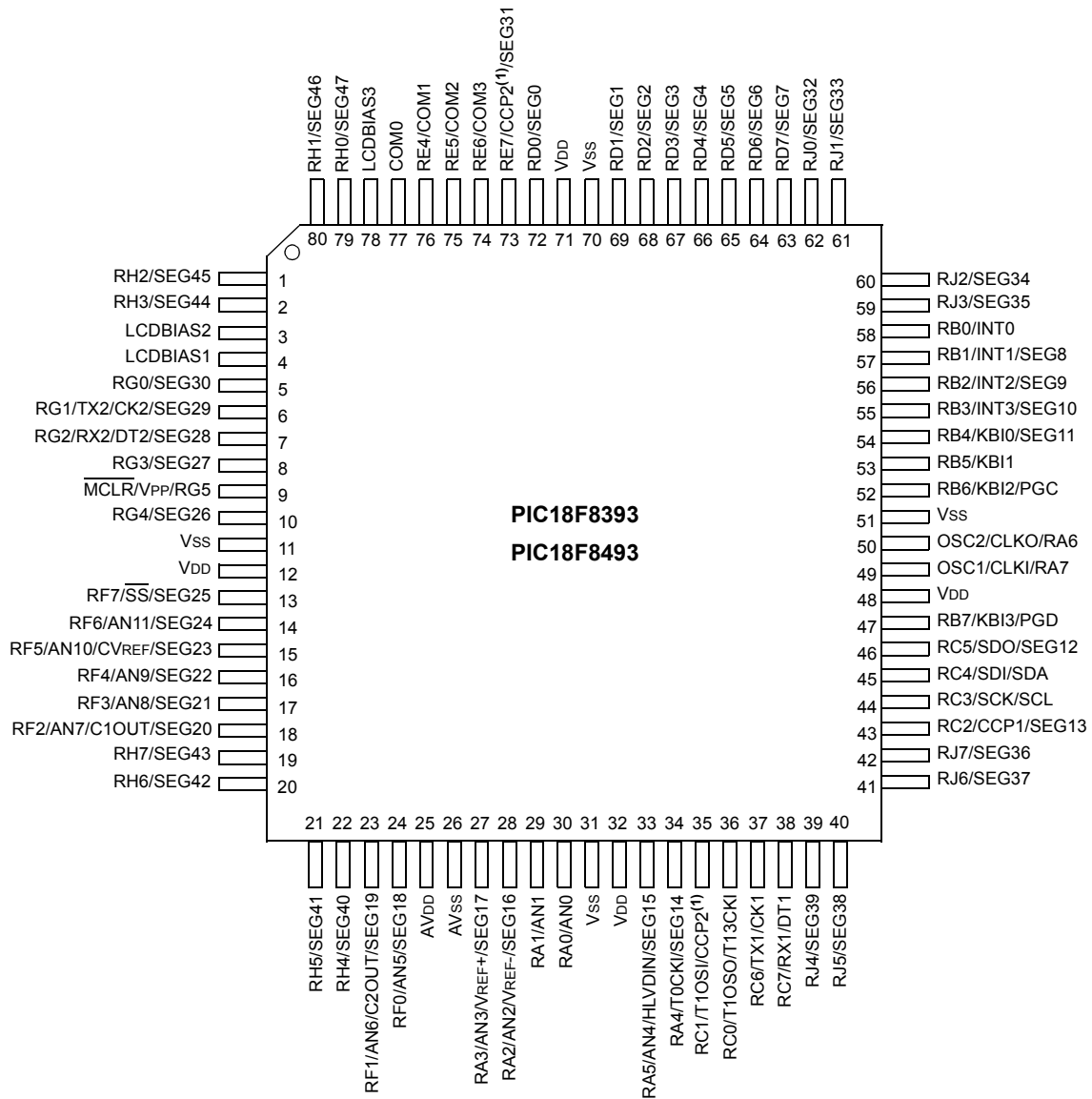
Note: This document is supplemented by the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629). See **Section 1.0 "Device Overview"**.

Device	Program Memory		Data Memory	I/O	LCD (pixel)	12-Bit A/D (channels)	CCP (PWM)	MSSP		EUSART/ AUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)					SPI	Master I ² C™			
PIC18F6393	8K	4096	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F6493	16K	8192	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F8393	8K	4096	768	66	192	12	2	Y	Y	1/1	2	1/3
PIC18F8493	16K	8192	768	66	192	12	2	Y	Y	1/1	2	1/3

PIC18F6393/6493/8393/8493

Pin Diagrams (Continued)

80-Pin TQFP



Note 1: RE7 is the alternate pin for CCP2 multiplexing.

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PIC18F6393/6493/8393/8493

NOTES:

PIC18F6393/6493/8393/8493

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6393
- PIC18F8393
- PIC18F6493
- PIC18F8493

Note: This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F6390/6490/8390/8490 devices. For information on the features and specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price. In addition to these features, the PIC18F6393/6493/8393/8493 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

1.1 Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduces code overhead.

1.2 Details on Individual Family Members

Devices in the PIC18F6393/6493/8393/8493 family are available in 64-pin (PIC18F6X93) and 80-pin (PIC18F8X93) packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2, respectively.

The devices are differentiated from each other in the following ways:

- I/O Ports:
 - 64-pin devices – 7 bidirectional ports
 - 80-pin devices – 9 bidirectional ports
- LCD Pixels:
 - 64-pin devices – 128 (32 SEGs x 4 COMs) pixels can be driven
 - 80-pin devices – 192 (48 SEGs x 4 COMs) pixels can be driven
- Flash Program Memory:
 - PIC18FX393 devices – 8 Kbytes
 - PIC18FX493 devices – 16 Kbytes

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F6393/6493/8393/8493 family are available as both standard and low-voltage devices. Standard devices with Flash memory, designated with an "F" in the part number (such as PIC18F6393), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF6490), function over an extended VDD range of 2.0V to 5.5V.

PIC18F6393/6493/8393/8493

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
MCLR/VPP/RG5 MCLR VPP RG5	7	I P I	ST ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input. Digital input.
OSC1/CLKI/RA7 OSC1 CLKI RA7	39	I I I/O	ST CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2 CLKO RA6	40	O O I/O	— — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RA0/AN0	24	I/O	TTL	PORTA is a bidirectional I/O port.
RA0		I	Analog	Digital I/O.
AN0				Analog Input 0.
RA1/AN1	23	I/O	TTL	Digital I/O.
RA1		I	Analog	Analog Input 1.
AN1				
RA2/AN2/VREF-/SEG16	22	I/O	TTL	Digital I/O.
RA2		I	Analog	Analog Input 2.
AN2		I	Analog	A/D reference voltage (Low) input.
VREF-		I	Analog	SEG16 output for LCD.
SEG16		O	Analog	
RA3/AN3/VREF+/SEG17	21	I/O	TTL	Digital I/O.
RA3		I	Analog	Analog Input 3.
AN3		I	Analog	A/D reference voltage (High) input.
VREF+		I	Analog	SEG17 output for LCD.
SEG17		O	Analog	
RA4/T0CKI/SEG14	28	I/O	ST	Digital I/O.
RA4		I	ST	Timer0 external clock input.
T0CKI		I	ST	SEG14 output for LCD.
SEG14		O	Analog	
RA5/AN4/HLVDIN/SEG15	27	I/O	TTL	Digital I/O.
RA5		I	Analog	Analog Input 4.
AN4		I	Analog	Low-Voltage Detect input.
HLVDIN		I	Analog	SEG15 output for LCD.
SEG15		O	Analog	
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
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Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0 RB0 INT0	48	I/O I	TTL ST	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. Digital I/O. External Interrupt 0.
RB1/INT1/SEG8 RB1 INT1 SEG8	47	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9 RB2 INT2 SEG9	46	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 2. SEG9 output for LCD.
RB3/INT3/SEG10 RB3 INT3 SEG10	45	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 3. SEG10 output for LCD.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	44	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1 RB5 KBI1	43	I/O I	TTL TTL	Digital I/O. Interrupt-on-change pin.
RB6/KBI2/PGC RB6 KBI2 PGC	42	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	37	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
PORTF is a bidirectional I/O port.				
RF0/AN5/SEG18	18	I/O	ST	Digital I/O.
RF0		I	Analog	Analog input 5.
AN5		O	Analog	SEG18 output for LCD.
SEG18				
RF1/AN6/C2OUT/SEG19	17	I/O	ST	Digital I/O.
RF1		I	Analog	Analog input 6.
AN6		O	—	Comparator 2 output.
C2OUT		O	Analog	SEG19 output for LCD.
SEG19				
RF2/AN7/C1OUT/SEG20	16	I/O	ST	Digital I/O.
RF2		I	Analog	Analog input 7.
AN7		O	—	Comparator 1 output.
C1OUT		O	Analog	SEG20 output for LCD.
SEG20				
RF3/AN8/SEG21	15	I/O	ST	Digital I/O.
RF3		I	Analog	Analog input 8.
AN8		O	Analog	SEG21 output for LCD.
SEG21				
RF4/AN9/SEG22	14	I/O	ST	Digital I/O.
RF4		I	Analog	Analog input 9.
AN9		O	Analog	SEG22 output for LCD.
SEG22				
RF5/AN10/CVREF/SEG23	13	I/O	ST	Digital I/O.
RF5		I	Analog	Analog input 10.
AN10		O	Analog	Comparator reference voltage output.
CVREF		O	Analog	SEG23 output for LCD.
SEG23				
RF6/AN11/SEG24	12	I/O	ST	Digital I/O.
RF6		I	Analog	Analog input 11.
AN11		O	Analog	SEG24 output for LCD.
SEG24				
RF7/ \overline{SS} /SEG25	11	I/O	ST	Digital I/O.
RF7		I	TTL	SPI™ slave select input.
\overline{SS}		O	Analog	SEG25 output for LCD.
SEG25				

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ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
MCLR/VPP/RG5 MCLR VPP RG5	9	I P I	ST ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input. Digital input.
OSC1/CLKI/RA7 OSC1 CLKI RA7	49	I I I/O	ST CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2 CLKO RA6	50	O O I/O	— — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	36			PORTC is a bidirectional I/O port.
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	35			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2 ⁽¹⁾		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/SEG13	43			
RC2		I/O	ST	Digital I/O.
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
SEG13		O	Analog	SEG13 output for LCD.
RC3/SCK/SCL	44			
RC3		I/O	ST	Digital I/O.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL		I/O	I ² C	Synchronous serial clock input/output for I ² C™ mode.
RC4/SDI/SDA	45			
RC4		I/O	ST	Digital I/O.
SDI		I	ST	SPI data in.
SDA		I/O	I ² C	I ² C data I/O.
RC5/SDO/SEG12	46			
RC5		I/O	ST	Digital I/O.
SDO		O	—	SPI data out.
SEG12		O	Analog	SEG12 output for LCD.
RC6/TX1/CK1	37			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	38			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C = ST with I²C™ or SMB levels

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the $\overline{\text{GO/DONE}}$ bit has been set and the $\text{ACQT}<2:0>$ bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the $\overline{\text{GO/DONE}}$ bit has been set, the $\text{ACQT}<2:0>$ bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the $\overline{\text{GO/DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will *not* be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note: The $\overline{\text{GO/DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2 μs after enabling the A/D before beginning an acquisition and conversion cycle.

2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

FIGURE 2-4: A/D CONVERSION TAD CYCLES ($\text{ACQT}<2:0> = 000$, $\text{Tacq} = 0$)

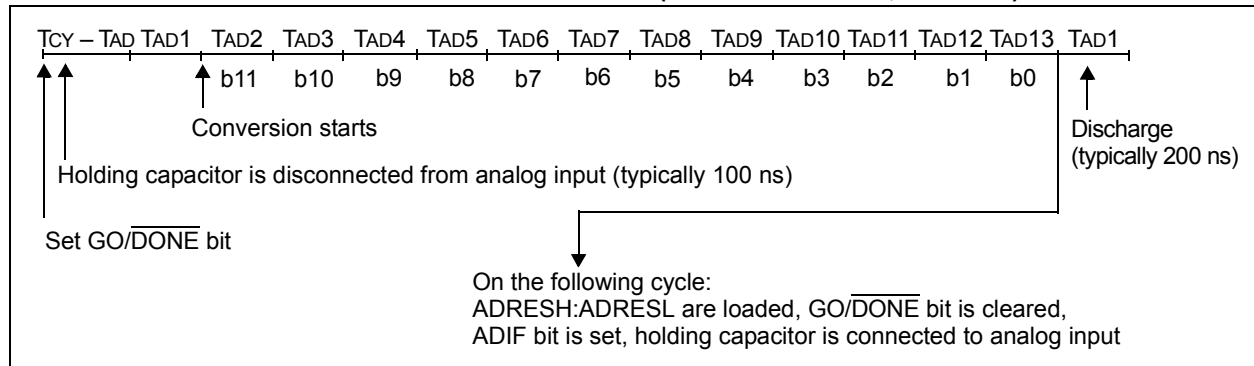
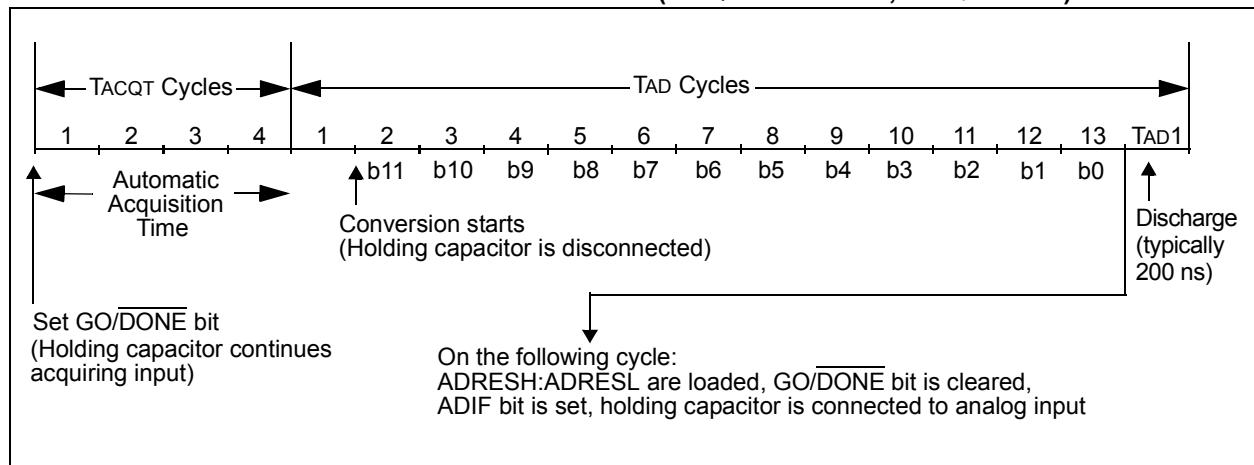


FIGURE 2-5: A/D CONVERSION TAD CYCLES ($\text{ACQT}<2:0> = 010$, $\text{Tacq} = 4 \text{ TAD}$)



PIC18F6393/6493/8393/8493

4.0 ELECTRICAL CHARACTERISTICS

Note: Other than some basic data, this section documents only the PIC18F6393/6493/8393/8493 devices' specifications that differ from those of the PIC18F6390/6490/8390/8490 devices. For detailed information on the electrical specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).

Absolute Maximum Ratings^(†)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V _{SS} (except V _{DD} and $\overline{\text{MCLR}}$)	-0.3V to (V _{DD} + 0.3V)
Voltage on V _{DD} with respect to V _{SS}	-0.3V to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS} (Note 2)	0V to +13.25V
Total power dissipation (Note 1)	1.0W
Maximum current out of V _{SS} pin	300 mA
Maximum current into V _{DD} pin	250 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports	200 mA

Note 1: Power dissipation is calculated as follows:

$$\text{PD}_{\text{IS}} = V_{\text{DD}} \times \{I_{\text{DD}} - \sum I_{\text{OH}}\} + \sum \{(V_{\text{DD}} - V_{\text{OH}}) \times I_{\text{OH}}\} + \sum (V_{\text{OL}} \times I_{\text{OL}})$$

- 2:** Voltage spikes below V_{SS} at the $\overline{\text{MCLR}}$ /V_{PP}/RG5 pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$ /V_{PP}/RG5 pin, rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC18F6393/6493/8393/8493

FIGURE 4-1: PIC18F6393/6493/8393/8493 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

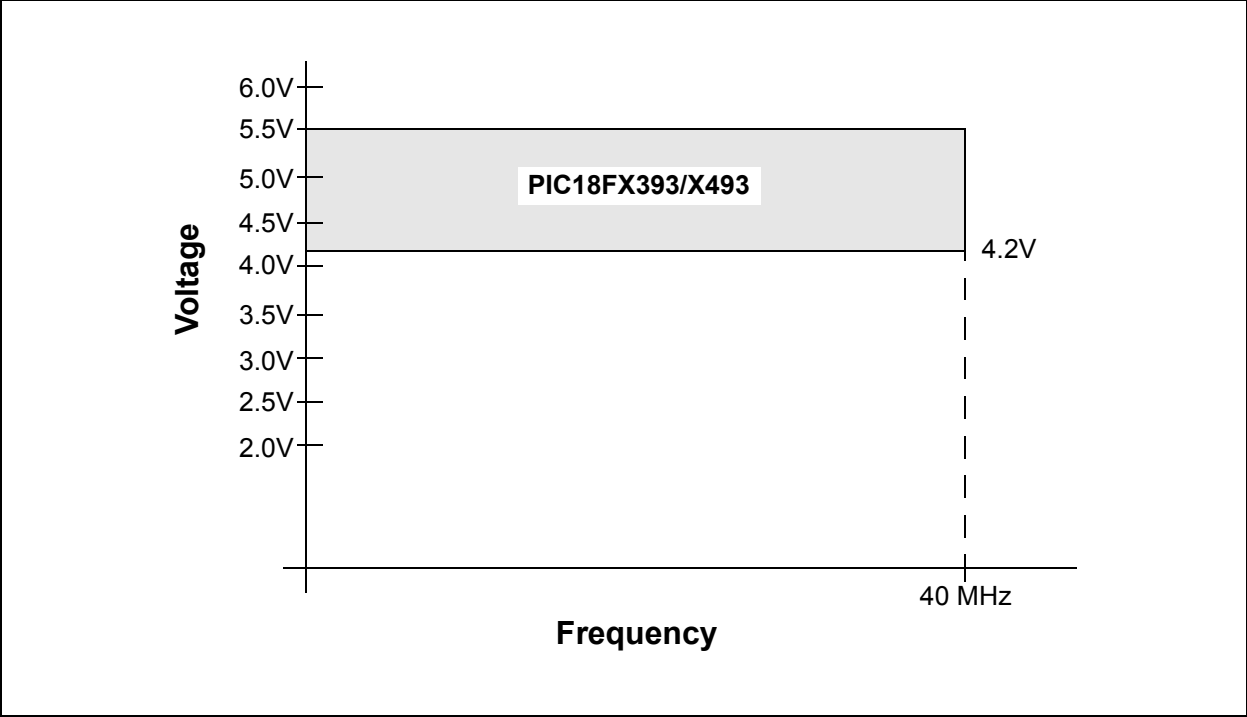
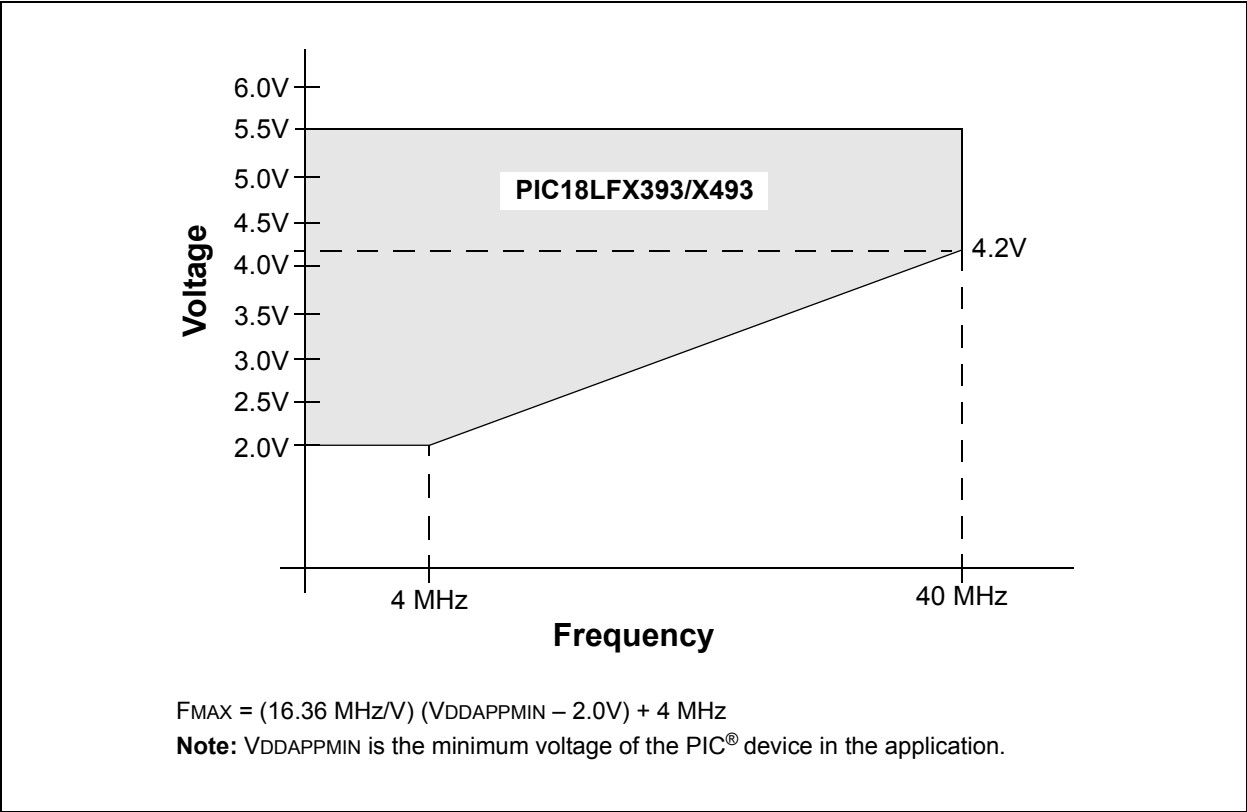


FIGURE 4-2: PIC18LF6393/6493/8393/8493 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



PIC18F6393/6493/8393/8493

TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F6393/6493/8393/8493 (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
A01	NR	Resolution	—	—	12	bit	$\Delta V_{REF} \geq 3.0V$
A03	EIL	Integral Linearity Error	—	$<\pm 1$	± 2.0	LSB	$V_{DD} = 3.0V$
			—	—	± 2.0	LSB	$V_{DD} = 5.0V$
A04	EDL	Differential Linearity Error	—	$<\pm 1$	$+1.5/-1.0$	LSB	$V_{DD} = 3.0V$
			—	—	$+1.5/-1.0$	LSB	$V_{DD} = 5.0V$
A06	EOFF	Offset Error	—	$<\pm 1$	± 5	LSB	$V_{DD} = 3.0V$
			—	—	± 3	LSB	$V_{DD} = 5.0V$
A07	EGN	Gain Error	—	$<\pm 1$	± 2.00	LSB	$V_{DD} = 3.0V$
			—	—	± 2.00	LSB	$V_{DD} = 5.0V$
A10	—	Monotonicity	Guaranteed ⁽¹⁾			—	$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	ΔV_{REF}	Reference Voltage Range ($V_{REFH} - V_{REFL}$)	3	—	$V_{DD} - V_{SS}$	V	For 12-bit resolution
A21	V_{REFH}	Reference Voltage High	$V_{SS} + \Delta V_{REF}$	—	V_{DD}	V	For 12-bit resolution
A22	V_{REFL}	Reference Voltage Low	V_{SS}	—	$V_{DD} - \Delta V_{REF}$	V	For 12-bit resolution
A25	V_{AIN}	Analog Input Voltage	V_{REFL}	—	V_{REFH}	V	
A30	Z_{AIN}	Recommended Impedance of Analog Voltage Source	—	—	2.5	k Ω	
A50	I _{REF}	V _{REF} Input Current ⁽²⁾	—	—	5	μA	During V _{AIN} acquisition. During A/D conversion cycle.
			—	—	150	μA	

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

Note 2: V_{REFH} current is from the RA3/AN3/ V_{REF+} /SEG17 pin or V_{DD} , whichever is selected as the V_{REFH} source. V_{REFL} current is from the RA2/AN2/ V_{REF-} /SEG16 pin or V_{SS} , whichever is selected as the V_{REFL} source.

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APPENDIX A: REVISION HISTORY

Revision A (September 2007)

Original data sheet for the PIC18F6393/6493/8393/8493 devices.

Revision B (October 2009)

Removed "Preliminary" marking.

Revision C (August 2010)

Changes and additions were made to the "**Power-Managed Modes**", "**Flexible Oscillator Structure**", "**Peripheral Highlights**" and "**Special Microcontroller Features**" sections. Changes were made to Figure 1-1, Figure 1-2, Table 1-2 and Table 1-3, including edits to the

legends of those tables. New text has replaced all in 2.4 "**Operation in Power-Managed Modes**". Corrections have been made to 4.0 "**Electrical Characteristics**". The extended temperature has been removed from the "**Product Identification System**" information. New packaging diagrams were added because the diagrams referenced in the document, "PIC18F6390/6490/8390/8490 *Data Sheet*" (DS39629), have not been updated. Minor typographical edits throughout the document.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features	PIC18F6393	PIC18F6493	PIC18F8393	PIC18F8493
Number of Pixels the LCD Driver Can Drive	128 (4 x 32)	128 (4 x 32)	192 (4 x 48)	192 (4 x 48)
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Flash Program Memory	8 Kbytes	16 Kbytes	8 Kbytes	16 Kbytes
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

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