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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 4x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f358cct6

- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.19 Inter-integrated circuit interface (I^2C)

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes. Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2) to wake up the MCU from Stop mode on address match.
The I2C interfaces can be served by the DMA controller.
Refer to *Table 7* for the features available in I2C1 and I2C2.

Table 7. STM32F358xC I^2C implementation

I2C features[(1)]	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

Table 10. Capacitive sensing GPIOs available on STM32F358xC devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
4	TSC_G4_IO1	PA9		TSC_G7_IO4	PE5
	TSC_G4_IO2	PA10	8	TSC_G8_IO1	PD12
	TSC_G4_IO3	PA13		TSC_G8_IO2	PD13
	TSC_G4_IO4	PA14		TSC_G8_IO3	PD14
				TSC_G8_IO4	PD15

Table 11. No. of capacitive sensing channels available on STM32F358xC devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F358xVx	STM32F358xRx	STM32F358xCx
G1	3	3	3
G2	3	3	3
G3	2	2	1
G4	3	3	3
G5	3	3	3
G6	3	3	3
G7	3	0	0
G8	3	0	0
Number of capacitive sensing channels	23	17	16

Figure 5. STM32F358xC LQFP64 pinout

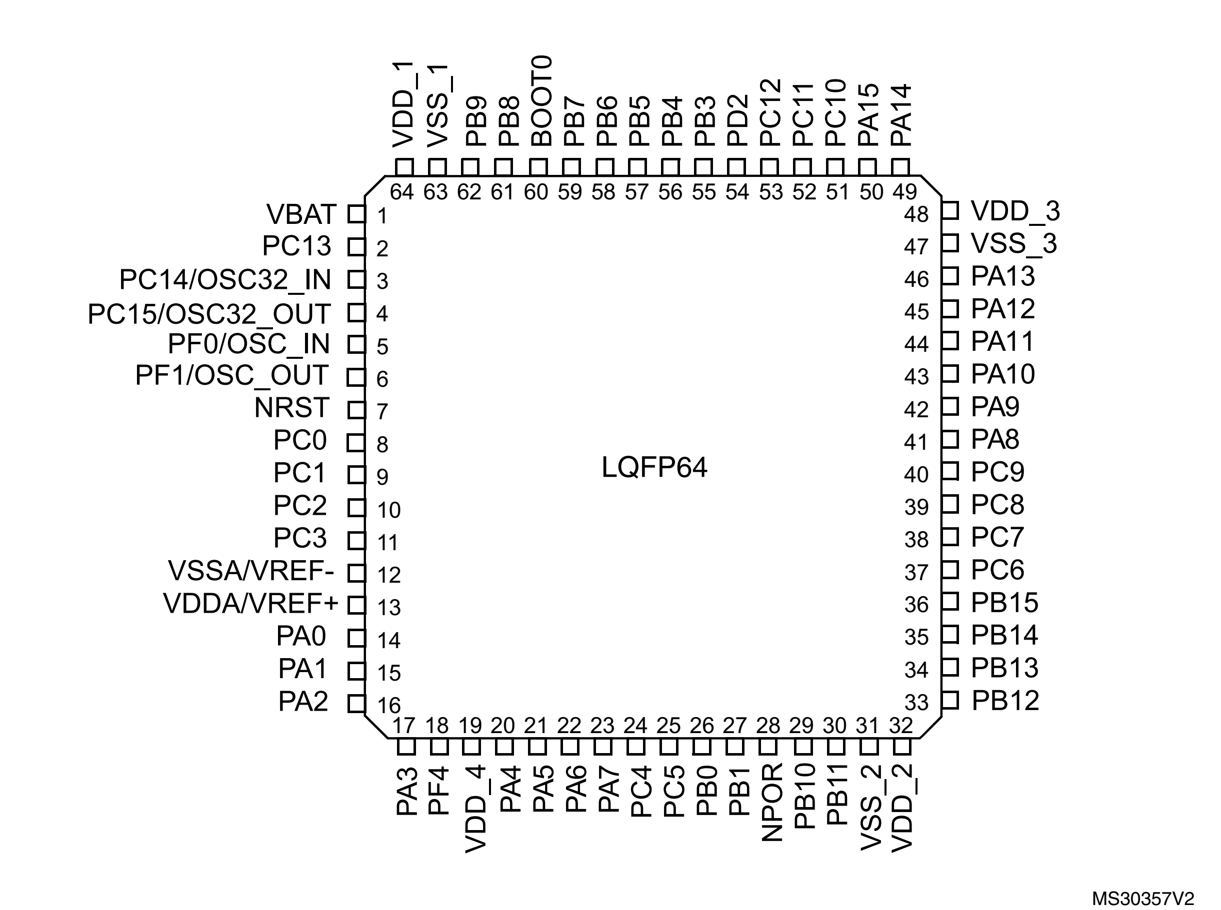


Table 13. STM32F358xC pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
32	23	17	PA7	I/O	TTa	-	SPI1_MOSI, TIM3_CH2, TIM17_CH1, TIM1_CH1N, TIM8_CH1N, TSC_G2_IO4, COMP2_OUT, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP2_VINP, OPAMP1_VINP
33	24	-	PC4	I/O	TTa	(1)	USART1_TX, EVENTOUT	ADC2_IN5
34	25	-	PC5	I/O	TTa	(1)	USART1_RX, TSC_G3_IO1, EVENTOUT	ADC2_IN11, OPAMP2_VINM, OPAMP1_VINM
35	26	18	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, TIM8_CH2N, TSC_G3_IO2, EVENTOUT	ADC3_IN12, COMP4_INP, OPAMP3_VINP, OPAMP2_VINP
36	27	19	PB1	I/O	TTa	(3)	TIM3_CH4, TIM1_CH3N, TIM8_CH3N, COMP4_OUT, TSC_G3_IO3, EVENTOUT	ADC3_IN1, OPAMP3_VOUT
37	28	20	NPOR	I	POR	(4)	Device power-on reset input	
38	-	-	PE7	I/O	TTa	(1)	TIM1_ETR, EVENTOUT	ADC3_IN13, COMP4_INP
39	-	-	PE8	I/O	TTa	(1)	TIM1_CH1N, EVENTOUT	COMP4_INM, ADC34_IN6
40	-	-	PE9	I/O	TTa	(1)	TIM1_CH1, EVENTOUT	ADC3_IN2
41	-	-	PE10	I/O	TTa	(1)	TIM1_CH2N, EVENTOUT	ADC3_IN14
42	-	-	PE11	I/O	TTa	(1)	TIM1_CH2, EVENTOUT	ADC3_IN15
43	-		PE12	I/O	TTa	(1)	TIM1_CH3N, EVENTOUT	ADC3_IN16
44	-	-	PE13	I/O	TTa	(1)	TIM1_CH3, EVENTOUT	ADC3_IN3
45	-	-	PE14	I/O	TTa	(1)	TIM1_CH4, TIM1_BKIN2, EVENTOUT	ADC4_IN1
46	-	-	PE15	I/O	TTa	(1)	USART3_RX, TIM1_BKIN, EVENTOUT	ADC4_IN2
47	29	21	PB10	I/O	TTa	-	USART3_TX, TIM2_CH3, TSC_SYNC, EVENTOUT	COMP5_INM, OPAMP4_VINM, OPAMP3_VINM
48	30	22	PB11	I/O	TTa	-	USART3_RX, TIM2_CH4, TSC_G6_IO1, EVENTOUT	COMP6_INP, OPAMP4_VINP
49	31	23	VSS_2	S	-	-	Digital ground	
50	32	24	VDD_2	S	-	-	Digital power supply	
51	33	25	PB12	I/O	TTa	(3)	SPI2_NSS, I2S2_WS, I2C2_SMBA, USART3_CK, TIM1_BKIN, TSC_G6_IO2, EVENTOUT	ADC4_IN3, COMP3_INM, OPAMP4_VOUT,

Table 13. STM32F358xC pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
67	41	29	PA8	I/O	FT	-	I2C2_SMBA, I2S2_MCK, USART1_CK, TIM1_CH1, TIM4_ETR, MCO, COMP3_OUT, EVENTOUT	-
68	42	30	PA9	I/O	FTf	-	I2C2_SCL, I2S3_MCK, USART1_TX, TIM1_CH2, TIM2_CH3, TIM15_BKIN, TSC_G4_IO1, COMP5_OUT, EVENTOUT	-
69	43	31	PA10	I/O	FTf	-	I2C2_SDA, USART1_RX, TIM1_CH3, TIM2_CH4, TIM8_BKIN, TIM17_BKIN, TSC_G4_IO2, COMP6_OUT, EVENTOUT	-
70	44	32	PA11	I/O	FT	-	USART1_CTS, CAN_RX, TIM1_CH1N, TIM1_CH4, TIM1_BKIN2, TIM4_CH1, COMP1_OUT, EVENTOUT	-
71	45	33	PA12	I/O	FT	-	USART1_RTS_DE, CAN_TX, TIM1_CH2N, TIM1_ETR, TIM4_CH2, TIM16_CH1, COMP2_OUT, EVENTOUT	-
72	46	34	PA13	I/O	FT	-	USART3_CTS, TIM4_CH3, TIM16_CH1N, TSC_G4_IO3, IR_OUT, SWDIO-JTMS, EVENTOUT	-
73	-	-	PF6	I/O	FTf	(1)	I2C2_SCL, USART3_RTS_DE, TIM4_CH4, EVENTOUT	-
74	47	35	VSS_3	S	-	-	Ground	
75	48	36	VDD_3	S	-	-	Digital power supply	
76	49	37	PA14	I/O	FTf	-	I2C1_SDA, USART2_TX, TIM8_CH2, TIM1_BKIN, TSC_G4_IO4, SWCLK-JTCK, EVENTOUT	-
77	50	38	PA15	I/O	FTf	-	I2C1_SCL, SPI1_NSS, SPI3_NSS, I2S3_WS, JTDI, USART2_RX, TIM1_BKIN, TIM2_CH1_ETR, TIM8_CH1, EVENTOUT	-

Table 13. STM32F358xC pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
78	51	-	PC10	I/O	FT	(1)	SPI3_SCK, I2S3_CK, USART3_TX, UART4_TX, TIM8_CH1N, EVENTOUT	-
79	52	-	PC11	I/O	FT	(1)	SPI3_MISO, I2S3ext_SD, USART3_RX, UART4_RX, TIM8_CH2N, EVENTOUT	-
80	53	-	PC12	I/O	FT	(1)	SPI3_MOSI, I2S3_SD, USART3_CK, UART5_TX, TIM8_CH3N, EVENTOUT	-
81	-	-	PD0	I/O	FT	(1)	CAN_RX, EVENTOUT	-
82	-	-	PD1	I/O	FT	(1)	CAN_TX, TIM8_CH4, TIM8_BKIN2, EVENTOUT	-
83	54	-	PD2	I/O	FT	(1)	UART5_RX, TIM3_ETR, TIM8_BKIN, EVENTOUT	-
84	-	-	PD3	I/O	FT	(1)	USART2_CTS, TIM2_CH1_ETR, EVENTOUT	-
85	-	-	PD4	I/O	FT	(1)	USART2_RTS_DE, TIM2_CH2, EVENTOUT	-
86	-	-	PD5	I/O	FT	(1)	USART2_TX, EVENTOUT	-
87	-	-	PD6	I/O	FT	(1)	USART2_RX, TIM2_CH4, EVENTOUT	-
88	-	-	PD7	I/O	FT	(1)	USART2_CK, TIM2_CH3, EVENTOUT	-
89	55	39	PB3	I/O	FT	-	SPI3_SCK, I2S3_CK, SPI1_SCK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM8_CH1N, TSC_G5_IO1, JTDO-TRACESWO, EVENTOUT	-
90	56	40	PB4	I/O	FT	-	SPI3_MISO, I2S3ext_SD, SPI1_MISO, USART2_RX, TIM3_CH1, TIM16_CH1, TIM17_BKIN, TIM8_CH2N, TSC_G5_IO2, NJTRST, EVENTOUT	-
91	57	41	PB5	I/O	FT	-	SPI3_MOSI, SPI1_MOSI, I2S3_SD, I2C1_SMBA, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM8_CH3N, TIM17_CH1, EVENTOUT	-

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When $f_{HCLK} > 8$ MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in *Table 28* to *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24*.

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 1.8 V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	44.2	48.2	49.4	50.5	6.6	7.2	7.8	8.4	mA
			64 MHz	39.5	43.1	44.3	45.2	5.8	6.5	7.0	7.6	
			48 MHz	29.9	32.7	33.8	34.6	4.4	4.9	5.5	6.0	
			32 MHz	20.2	22.1	23.0	23.7	3.0	3.3	3.9	4.5	
			24 MHz	15.2	16.7	17.5	18.2	2.3	2.5	3.0	3.7	
			8 MHz	4.9	5.6	6.1	6.7	0.6	0.8	1.2	2.0	
			1 MHz	0.5	0.7	1.0	1.8	0.1	0.0	0.4	1.2	
		Internal clock (HSI)	64 MHz	34.5	37.7	38.9	39.7	5.5	6.2	6.6	7.2	
			48 MHz	26.1	28.6	29.7	30.4	4.1	4.6	5.1	5.7	
			32 MHz	17.6	19.3	20.2	20.8	2.7	3.0	3.5	4.2	
			24 MHz	13.3	14.7	15.4	16.0	1.3	1.6	2.0	2.7	
			8 MHz	4.4	4.9	5.5	6.1	0.5	0.7	1.0	1.9	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

Table 29. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run/Sleep mode, code executing from Flash or RAM	HSE bypass	72 MHz	225	276	289	297	245	302	319	329	µA
			64 MHz	198	249	261	268	216	270	284	293	
			48 MHz	149	195	204	211	159	209	222	230	
			32 MHz	102	145	152	157	110	154	162	169	
			24 MHz	80	119	124	128	86	126	131	135	
			8 MHz	2	3	4	6	3	4	5	9	
			1 MHz	2	3	5	7	3	4	6	9	
		HSI clock	64 MHz	270	323	337	344	299	354	371	381	
			48 MHz	220	269	280	286	244	293	309	318	
			32 MHz	173	218	228	233	193	239	251	257	
			24 MHz	151	194	200	204	169	211	219	225	
			8 MHz	73	97	99	103	88	105	110	116	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.

2. Data based on characterization results, not tested in production.

Table 30. Typical and maximum V_{DD} consumption in Stop mode

Symbol	Parameter	Conditions	Typ@V_{DD} (V_{DD}=V_{DDA}=1.8V)	Max(1)			Unit
				T_A=25 °C	T_A=85 °C	T_A=105 °C	
I_{DD}	Supply current in Stop mode	All oscillators OFF	6.6	31.1(2)	560.5	1225.8(2)	µA

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production.

Table 31. Typical and maximum V_{DDA} consumption in Stop mode

Symbol	Parameter	Conditions	Typ@V_{DDA}(V_{DD} = 1.8V)							Max(1)			Unit
			1.8 V	2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DDA}	Supply current in Stop mode	All oscillators OFF	0.76	0.78	0.80	0.83	0.87	0.94	1.01	3.2	5.3	7.9	µA

1. Data based on characterization results and tested in production.

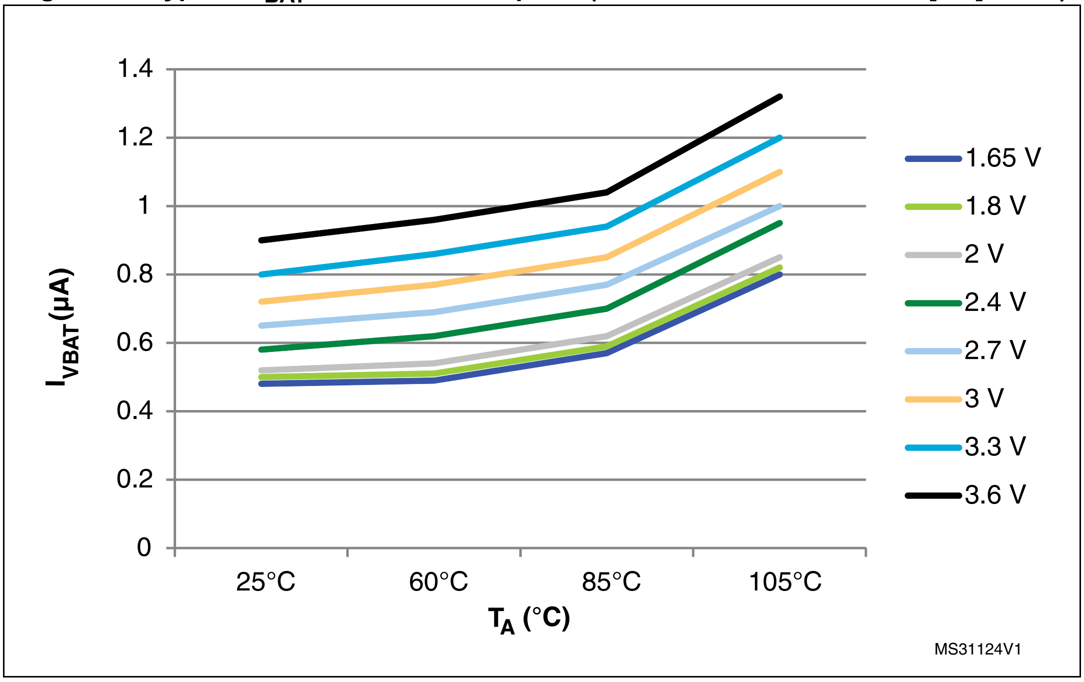
Note: The total current consumption is the sum of IDD and IDDA

Table 32. Typical and maximum current consumption from V_{BAT} supply

Symbol	Para meter	Conditions (1)	Typ @V_{BAT}								Max @V_{BAT} = 3.6 V(2)			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A = 25°C	T_A = 85°C	T_A = 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.48	0.50	0.52	0.58	0.65	0.72	0.80	0.90	1.1	1.5	2.0	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.83	0.86	0.90	0.98	1.03	1.10	1.20	1.30	1.5	2.2	2.9	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Data based on characterization results, not tested in production.

Figure 12. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = ’00’)



Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = 1.8 V, V_{DDA} = 3.3 V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ: Peripherals enabled	Typ: Peripherals disabled	Unit
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	58.6	26.5	mA
			64 MHz	52.6	23.7	
			48 MHz	40.6	18.5	
			32 MHz	27.6	12.7	
			24 MHz	21.1	9.9	
			16 MHz	14.3	6.8	
			8 MHz	7.2	3.5	
			4 MHz	4.1	2.1	
			2 MHz	2.3	1.3	
			1 MHz	1.5	0.9	
			500 kHz	1.0	0.7	
			125 kHz	0.7	0.5	
I_{DDA} (1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	239.0		µA
			64 MHz	210.3		
			48 MHz	157.0		
			32 MHz	108.1		
			24 MHz	84.4		
			16 MHz	60.8		
			8 MHz	1.0		
			4 MHz	1.0		
			2 MHz	1.0		
			1 MHz	1.0		
			500 kHz	1.0		
			125 kHz	1.0		

1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 35. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 1.8 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.10	mA
			4 MHz	0.17	
			8 MHz	0.40	
			18 MHz	0.78	
			36 MHz	1.51	
			48 MHz	2.06	
		V_{DD} = 1.8 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.14	
			4 MHz	0.25	
			8 MHz	0.57	
			18 MHz	1.16	
			36 MHz	2.45	
			48 MHz	3.03	
		V_{DD} = 1.8 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.19	
			4 MHz	0.36	
			8 MHz	0.75	
			18 MHz	1.59	
			36 MHz	3.25	
		V_{DD} = 1.8 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.23	
			4 MHz	0.45	
			8 MHz	0.94	
			18 MHz	1.97	
			36 MHz	3.62	
		V_{DD} = 1.8 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.28	
			4 MHz	0.55	
			8 MHz	1.15	
			18 MHz	2.42	

1. CS = 5 pF (estimated value).

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 48. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 1.8 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	**7**	dBµV
			30 to 130 MHz	**16**	
			130 MHz to 1GHz	**23**	
			SAE EMI Level	**4**	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 49. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	II	500	

1. Data based on characterization results, not tested in production.

6.3.13 I/O port characteristics

General input/output characteristics

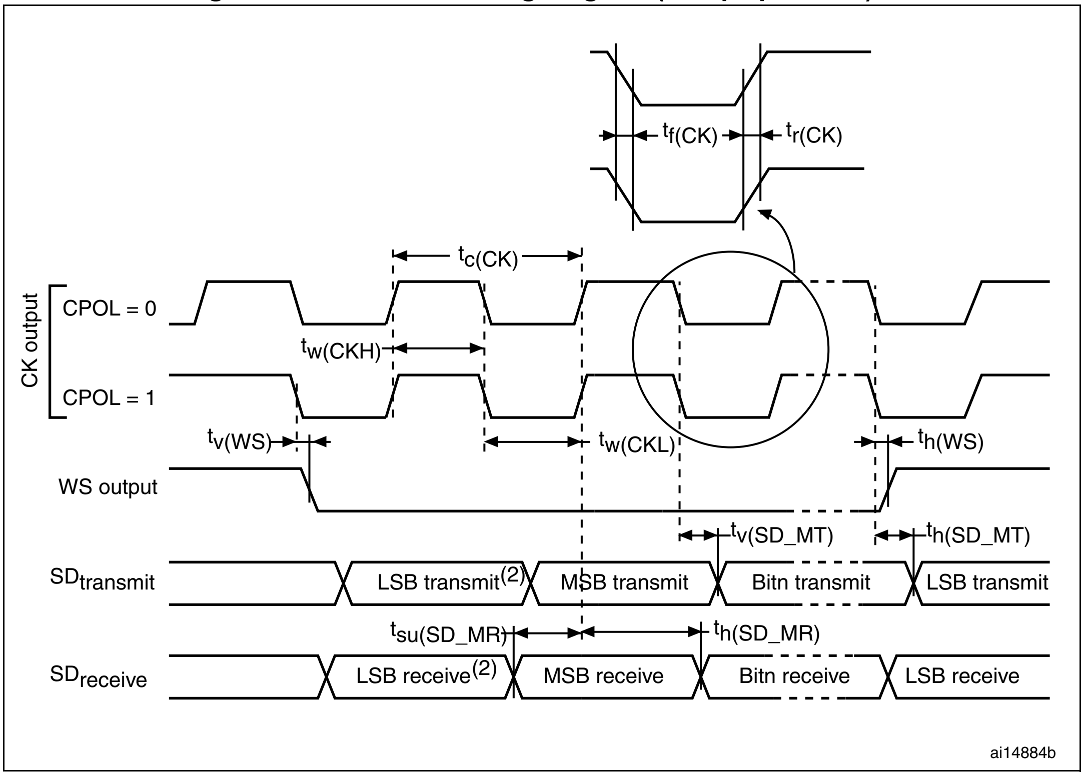
Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the conditions summarized in *Table 24*. All I/Os are CMOS and TTL compliant.

Table 52. I/O static characteristics

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="4">V_{IL}</td><td rowspan="4">Low level input voltage</td><td>TC and TTa I/O</td><td>-</td><td>-</td><td>0.3 V_{DD}+0.07 (1)</td><td rowspan="8">V</td></tr>
<tr><td>FT and FTf I/O</td><td>-</td><td>-</td><td>0.475 V_{DD}-0.2 (1)</td></tr>
<tr><td>BOOT0</td><td>-</td><td>-</td><td>0.3 V_{DD}–0.3 (1)</td></tr>
<tr><td>All I/Os except BOOT0</td><td>-</td><td>-</td><td>0.3 V_{DD} (2)</td></tr>
<tr><td rowspan="4">V_{IH}</td><td rowspan="4">High level input voltage</td><td>TC and TTa I/O</td><td>0.445 V_{DD}+0.398 (1)</td><td>-</td><td>-</td></tr>
<tr><td>FT and FTf I/O</td><td>0.5 V_{DD}+0.2 (1)</td><td>-</td><td>-</td></tr>
<tr><td>BOOT0</td><td>0.2 V_{DD}+0.95 (1)</td><td>-</td><td>-</td></tr>
<tr><td>All I/Os except BOOT0</td><td>0.7 V_{DD} (2)</td><td>-</td><td>-</td></tr>
<tr><td rowspan="3">V_{hys}</td><td rowspan="3">Schmitt trigger hysteresis</td><td>TC and TTa I/O</td><td>-</td><td>200 (1)</td><td>-</td><td rowspan="3">mV</td></tr>
<tr><td>FT and FTf I/O</td><td>-</td><td>100 (1)</td><td>-</td></tr>
<tr><td>BOOT0</td><td>-</td><td>300 (1)</td><td>-</td></tr>
<tr><td rowspan="5">I_{lkg}</td><td rowspan="5">Input leakage current (3)</td><td>TC, FT, FTf and POR I/O
TTa I/O in digital mode
$V_{SS} \leq V_{IN} \leq V_{DD}$</td><td>-</td><td>-</td><td>±0.1</td><td rowspan="5">µA</td></tr>
<tr><td>TTa I/O in digital mode
$V_{DD} \leq V_{IN} \leq V_{DDA}$</td><td>-</td><td>-</td><td>1</td></tr>
<tr><td>TTa I/O in analog mode
$V_{SS} \leq V_{IN} \leq V_{DDA}$</td><td>-</td><td>-</td><td>±0.2</td></tr>
<tr><td>FT and FTf I/O(4)
$V_{DD} \leq V_{IN} \leq 5$ V</td><td>-</td><td>-</td><td>10</td></tr>
<tr><td>POR
$V_{DDA} \leq V_{IN} \leq 5$ V</td><td>-</td><td>-</td><td>10</td></tr>
<tr><td>R_{PU}</td><td>Weak pull-up equivalent resistor(5)</td><td>$V_{IN} = V_{SS}$</td><td>25</td><td>40</td><td>55</td><td>kΩ</td></tr>
<tr><td>R_{PD}</td><td>Weak pull-down equivalent resistor(5)</td><td>$V_{IN} = V_{DD}$</td><td>25</td><td>40</td><td>55</td><td>kΩ</td></tr>
<tr><td>C_{IO}</td><td>I/O pin capacitance</td><td>-</td><td>-</td><td>5</td><td>-</td><td>pF</td></tr>
</table>

1. Data based on design simulation.
2. Tested in production.
3. Leakage could be higher than the maximum value. if negative current is injected on adjacent pins. Refer to *Table 51: I/O current injection susceptibility*.
4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.

Figure 27. I²S master timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

CAN (controller area network) interface

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

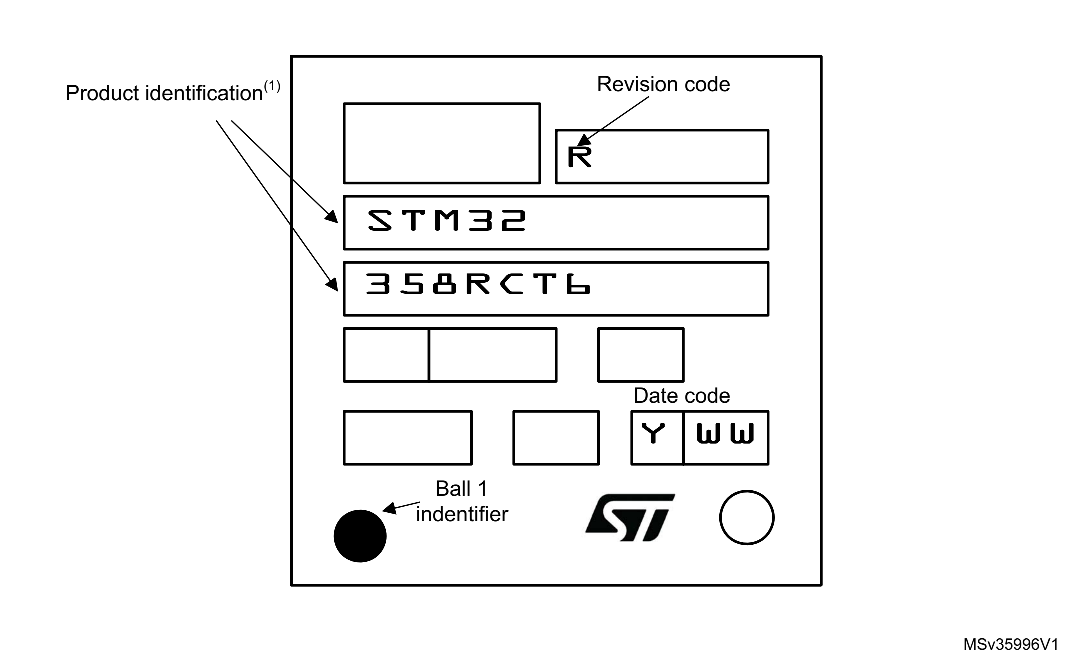
Table 69. ADC accuracy, 64-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min(4)	Max(4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps $1.8V \leq V_{DDA}$, $V_{REF+} \leq 3.6$ V 64-pin package	Single Ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4.5	
EO	Offset error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2.5	
				Slow channel 4.8 Ms	-	±2.5	
EG	Gain error		Single Ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	
				Slow channel 4.8 Ms	-	±4	
ED	Differential linearity error		Single Ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB	Effective number of bits		Single Ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. LQFP64 – 10 x 10 mm, low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.