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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 4x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f358rct6

3.7 Power management

3.7.1 Power supply schemes

- V_{SS}, V_{DD} = 1.8 V+/- 8%: external power supply for I/Os and core. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supply for ADC, DACs, comparators operational amplifiers, reset blocks, RCs and PLL. The minimum voltage to be applied to V_{DDA} differs from one analog peripheral to another. *Table 3* provides the summary of the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT}= 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch which is guaranteed in the full range of VDD) when VDD is not present.

Table 3. External analog supply values for analog peripherals

Analog peripheral	Minimum V_{DDA} supply	Maximum V_{DDA} supply
ADC	1.8 V	3.6 V
COMP	1.65 V	3.6 V
DAC / OPAMP	2.4 V	3.6V

3.7.2 Power supply supervision

The device power on reset is controlled through the external NPOR pin. The device remains in reset state when NPOR pin is held low.

To guarantee a proper power-on reset, the NPOR pin must be held low when VDDA is applied. Then, when VDD is stable, the reset state can be exited by:

- either putting the NPOR pin in high impedance. NPOR pin has an internal pull up.
- or forcing the pin to high level by connecting it to V_{DDA}.

3.7.3 Low-power modes

The STM32F358xC devices support two low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- Sleep mode

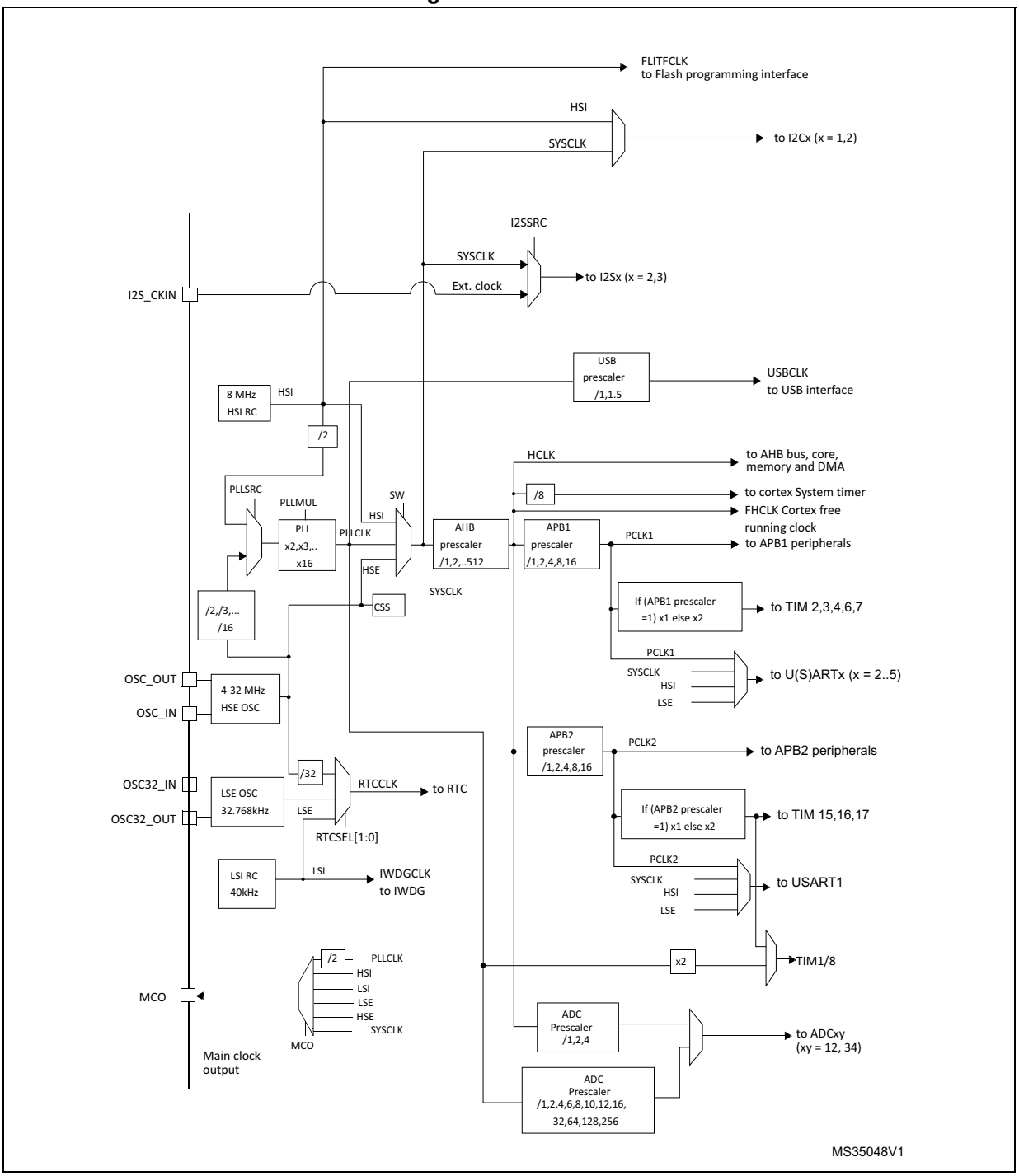
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop mode.

Figure 2. Clock tree



- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.19 Inter-integrated circuit interface (I^2C)

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes. Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2) to wake up the MCU from Stop mode on address match. The I2C interfaces can be served by the DMA controller.
Refer to *Table 7* for the features available in I2C1 and I2C2.

Table 7. STM32F358xC I^2C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

Table 13. STM32F358xC pin definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
1	-	-	PE2	I/O	FT	(1)	TRACECK, TIM3_CH1, TSC_G7_IO1, EVENTOUT	-
2	-	-	PE3	I/O	FT	(1)	TRACED0, TIM3_CH2, TSC_G7_IO2, EVENTOUT	-
3	-	-	PE4	I/O	FT	(1)	TRACED1, TIM3_CH3, TSC_G7_IO3, EVENTOUT	-
4	-	-	PE5	I/O	FT	(1)	TRACED2, TIM3_CH4, TSC_G7_IO4, EVENTOUT	-
5	-	-	PE6	I/O	FT	(1)	TRACED3, EVENTOUT	WKUP3, RTC_TAMP3
6	1	1	V_{BAT}	S	-	-	Backup power supply	
7	2	2	PC13(2)	I/O	TC	-	TIM1_CH1N	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
8	3	3	PC14(2) OSC32_IN (PC14)	I/O	TC	-	-	OSC32_IN
9	4	4	PC15(2) OSC32_ OUT (PC15)	I/O	TC	-	-	OSC32_OUT
10	-	-	PF9	I/O	FT	(1)	TIM15_CH1, SPI2_SCK, EVENTOUT	-
11	-	-	PF10	I/O	FT	(1)	TIM15_CH2, SPI2_SCK, EVENTOUT	-
12	5	5	PF0- OSC_IN (PF0)	I/O	FTf	-	TIM1_CH3N, I2C2_SDA,	OSC_IN
13	6	6	PF1- OSC_OUT (PF1)	I/O	FTf	-	I2C2_SCL	OSC_OUT
14	7	7	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
15	8	-	PC0	I/O	TTa	(1)	EVENTOUT	ADC12_IN6, COMP7_INM
16	9	-	PC1	I/O	TTa	(1)	EVENTOUT	ADC12_IN7, COMP7_INP
17	10	-	PC2	I/O	TTa	(1)	COMP7_OUT, EVENTOUT	ADC12_IN8
18	11	-	PC3	I/O	TTa	(1)	TIM1_BKIN2, EVENTOUT	ADC12_IN9
19	-	-	PF2	I/O	TTa	(1)	EVENTOUT	ADC12_IN10
20	12	8	VSSA/ VREF-	S	-	-	Analog ground/Negative reference voltage	

Table 13. STM32F358xC pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
78	51	-	PC10	I/O	FT	(1)	SPI3_SCK, I2S3_CK, USART3_TX, UART4_TX, TIM8_CH1N, EVENTOUT	-
79	52	-	PC11	I/O	FT	(1)	SPI3_MISO, I2S3ext_SD, USART3_RX, UART4_RX, TIM8_CH2N, EVENTOUT	-
80	53	-	PC12	I/O	FT	(1)	SPI3_MOSI, I2S3_SD, USART3_CK, UART5_TX, TIM8_CH3N, EVENTOUT	-
81	-	-	PD0	I/O	FT	(1)	CAN_RX, EVENTOUT	-
82	-	-	PD1	I/O	FT	(1)	CAN_TX, TIM8_CH4, TIM8_BKIN2, EVENTOUT	-
83	54	-	PD2	I/O	FT	(1)	UART5_RX, TIM3_ETR, TIM8_BKIN, EVENTOUT	-
84	-	-	PD3	I/O	FT	(1)	USART2_CTS, TIM2_CH1_ETR, EVENTOUT	-
85	-	-	PD4	I/O	FT	(1)	USART2_RTS_DE, TIM2_CH2, EVENTOUT	-
86	-	-	PD5	I/O	FT	(1)	USART2_TX, EVENTOUT	-
87	-	-	PD6	I/O	FT	(1)	USART2_RX, TIM2_CH4, EVENTOUT	-
88	-	-	PD7	I/O	FT	(1)	USART2_CK, TIM2_CH3, EVENTOUT	-
89	55	39	PB3	I/O	FT	-	SPI3_SCK, I2S3_CK, SPI1_SCK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM8_CH1N, TSC_G5_IO1, JTDO-TRACESWO, EVENTOUT	-
90	56	40	PB4	I/O	FT	-	SPI3_MISO, I2S3ext_SD, SPI1_MISO, USART2_RX, TIM3_CH1, TIM16_CH1, TIM17_BKIN, TIM8_CH2N, TSC_G5_IO2, NJTRST, EVENTOUT	-
91	57	41	PB5	I/O	FT	-	SPI3_MOSI, SPI1_MOSI, I2S3_SD, I2C1_SMBA, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM8_CH3N, TIM17_CH1, EVENTOUT	-

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 21: Voltage characteristics*, *Table 22: Current characteristics*, and *Table 23: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 21. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}– V_{SS}	External digital supply voltage (including V_{DD} and V_{BAT})	-0.3	1.95	V
V_{DDA}– V_{SS}	External analog supply voltage	-0.3	4.0	
V_{DD}– V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	
V_{REF+}–V_{DDA}(2)	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	
V_{IN}(3)	Input voltage on FT and FTf pins	V_{SS} – 0.3	V_{DD} + 4.0	
	Input voltage on TTa pins	V_{SS} – 0.3	4.0	
	Input voltage on any other pin	V_{SS} – 0.3	4.0	
	Input voltage on POR pin	V_{SS} – 0.3	V_{DDA} + 4.0	
	Input Voltage on B Pin	0	9	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
V_{DDA} must be greater than or equal to V_{DD}.
2. V_{REF+} must be always lower or equal than V_{DDA} ($V_{REF+} \leq V_{DDA}$). If unused then it must be connected to V_{DDA}.
3. V_{IN} maximum must always be respected. Refer to *Table 22: Current characteristics* for the maximum allowed injected current values.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and V_{DD} = 1.8 V, V_{DDA} = 3.3 V.

Table 36. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	12.6	µA/MHz
DMA1	7.6	
DMA2	6.1	
CRC	2.1	
GPIOA	10.0	
GPIOB	10.3	
GPIOC	2.2	
GPIOD	8.8	
GPIOE	3.3	
GPIOF	3.0	
TSC	5.5	
ADC1&2	17.3	
ADC3&4	18.8	
APB2-Bridge (3)	3.6	
SYSCFG	7.3	
TIM1	40.0	
SPI1	8.8	
TIM8	36.4	
USART1	23.3	
TIM15	17.1	
TIM16	10.1	
TIM17	11.0	
APB1-Bridge (3)	6.1	
TIM2	49.1	
TIM3	38.8	
TIM4	38.3	

Table 36. Peripheral current consumption (continued)

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
TIM6	9.7	µA/MHz
TIM7	12.1	
WWDG	6.4	
SPI2	40.4	
SPI3	40.0	
USART2	41.9	
USART3	40.2	
UART4	36.5	
UART5	30.8	
I2C1	10.5	
I2C2	10.4	
CAN	33.4	
PWR	5.7	
DAC	15.4	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

6.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 45. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 46. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 50. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

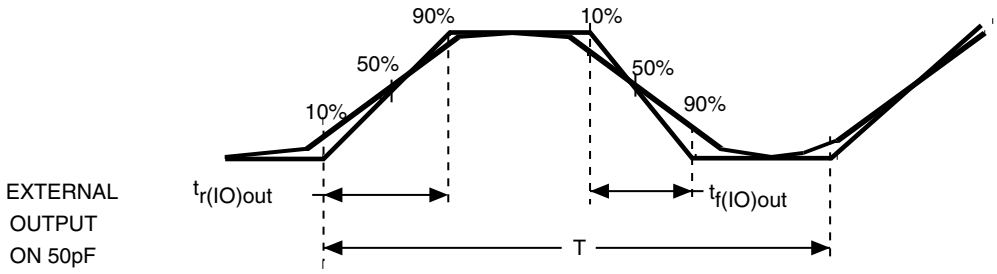
Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 51*

Figure 20. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

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6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 52*).

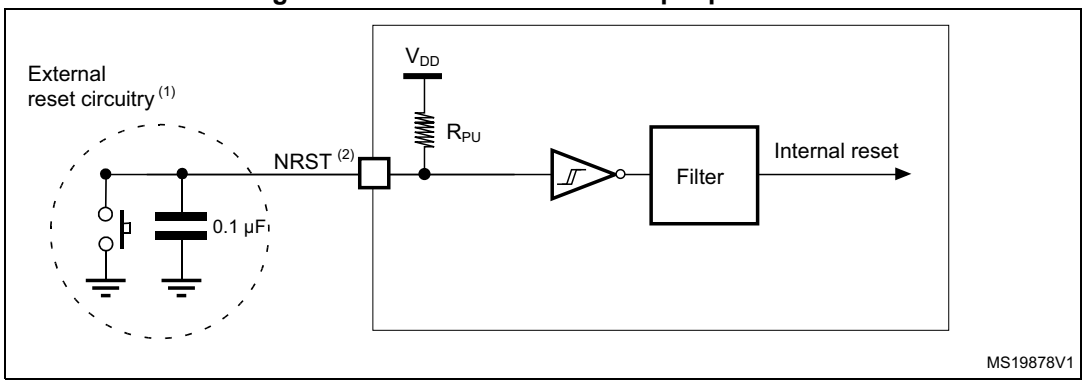
Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 55. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}$+ 0.07(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	$0.445V_{DD}$+ 0.398(1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	700(1)	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 21. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 55*. Otherwise the reset will not be taken into account by the device.

6.3.15 NPOR pin characteristics

The NPOR pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, Rpu (see *Table 56*) connected to V_{DDA} supply.

Unless otherwise specified, the parameters given in *Table 56* are derived from tests performed under ambient temperature and V_{DDA} supply voltage conditions summarized in *Table 24*.

Table 56. NPOR pin characteristics

Symbol(1)	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NPOR)}$	NPOR Input low level voltage	-	-	-	$0.475V_{DDA}$ - 0.2	V
$V_{IH(NPOR)}$	NPOR Input high level voltage	-	$0.5V_{DDA}$ + 0.2	-	-	
$V_{hys(NPOR)}$	NPOR Schmitt trigger voltage hysteresis	-	-	100	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.16 Timer characteristics

The parameters given in *Table 57* are guaranteed by design.

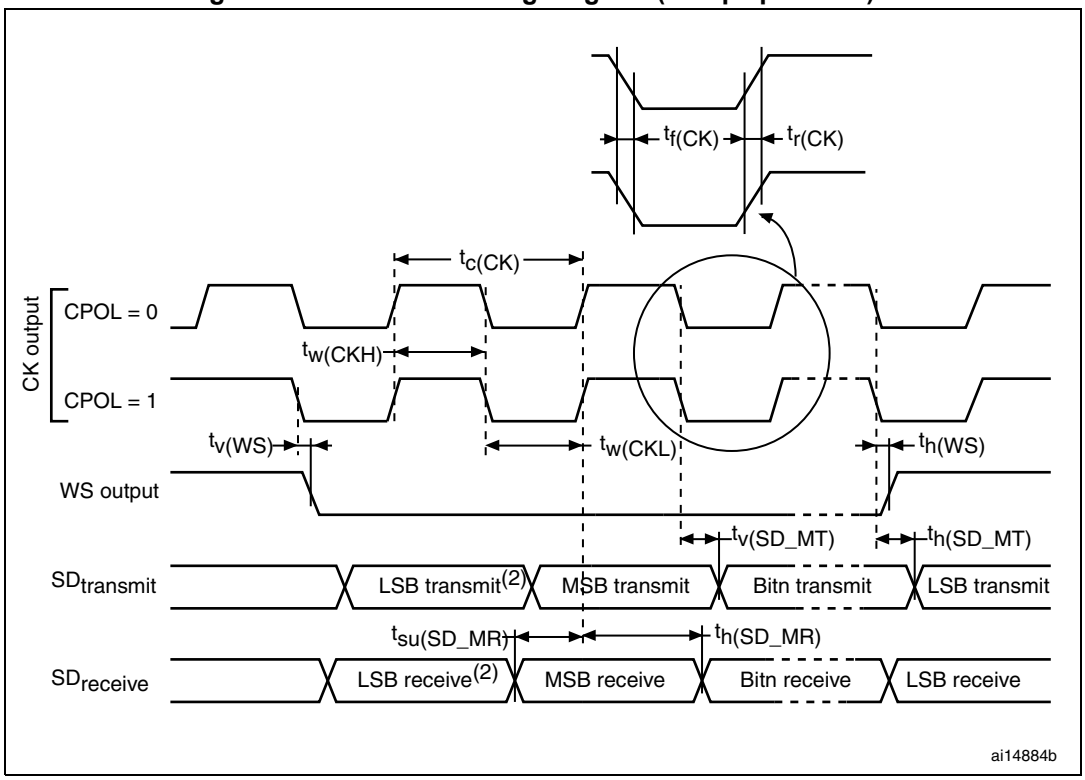
Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 57. TIMx(1)(2) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
		$f_{TIMxCLK}$ = 144 MHz, x= 1.8	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
		$f_{TIMxCLK}$ = 144 MHz, x= 1.8	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIMxCLK}$ = 144 MHz, x= 1.8	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM6, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.

Figure 27. I²S master timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

CAN (controller area network) interface

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.18 ADC characteristics

Unless otherwise specified, the parameters given in *Table 64* to *Table 67* are guaranteed by design, with conditions summarized in *Table 24*.

Table 64. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	1.8	-	3.6	V
I_{DDA}	ADC current consumption on VDDA pin (see *Figure 28*)	Single-ended mode, 5 MSPS	-	907	1033.0	µA
		Single-ended mode, 1 MSPS	-	194	285.5	
		Single-ended mode, 200 KSPS	-	51.5	70	
		Differential mode, 5 MSPS	-	887.5	1009	
		Differential mode, 1 MSPS	-	212	285	
		Differential mode, 200 KSPS	-	51	69.5	
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
I_{REF}	ADC current consumption on VREF+ pin (see *Figure 29*)	Single-ended mode, 5 MSPS	-	104	139	µA
		Single-ended mode, 1 MSPS	-	20.4	37	
		Single-ended mode, 200 KSPS	-	3.3	11.3	
		Differential mode, 5 MSPS	-	174	235	
		Differential mode, 1 MSPS	-	34.6	52.6	
		Differential mode, 200 KSPS	-	6	13.6	
f_{ADC}	ADC clock frequency		0.14	-	72	MHz
f_S (1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	

Table 66. ADC accuracy - limited test conditions 100-pin packages(1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps $V_{DDA} = V_{REF+} = 3.3$ V 25°C 100-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-76	-76	
				Slow channel 4.8 Ms	-	-76	-76	
			Differential	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-80	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Table 69. ADC accuracy, 64-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min(4)	Max(4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 1.8V ≤ V_{DDA} , V_{REF+} ≤ 3.6 V 64-pin package	Single Ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4.5	
EO	Offset error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2.5	
				Slow channel 4.8 Ms	-	±2.5	
EG	Gain error		Single Ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	
				Slow channel 4.8 Ms	-	±4	
ED	Differential linearity error		Single Ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB	Effective number of bits		Single Ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	

Figure 30. ADC accuracy characteristics

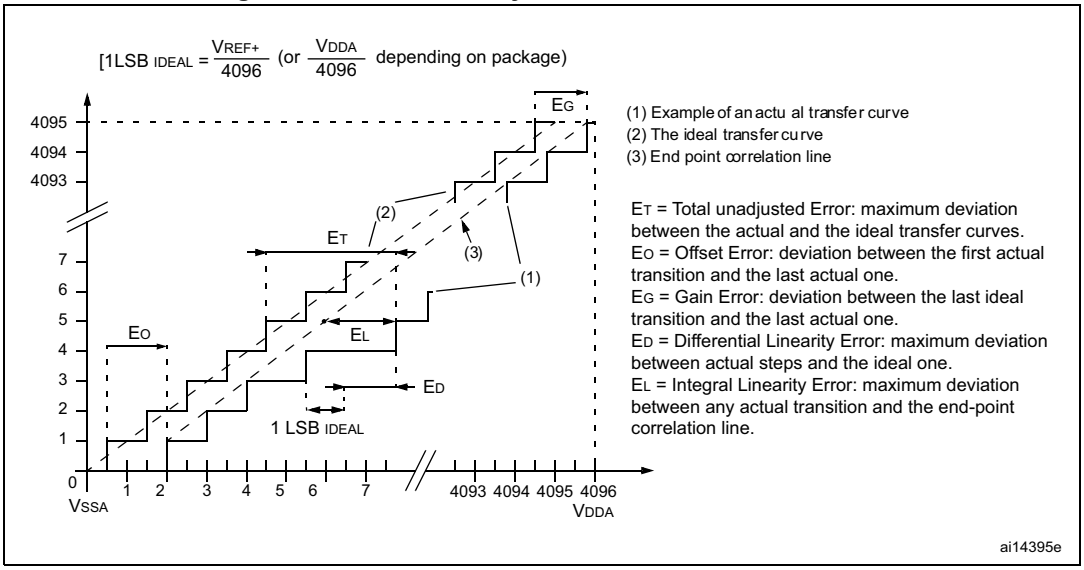
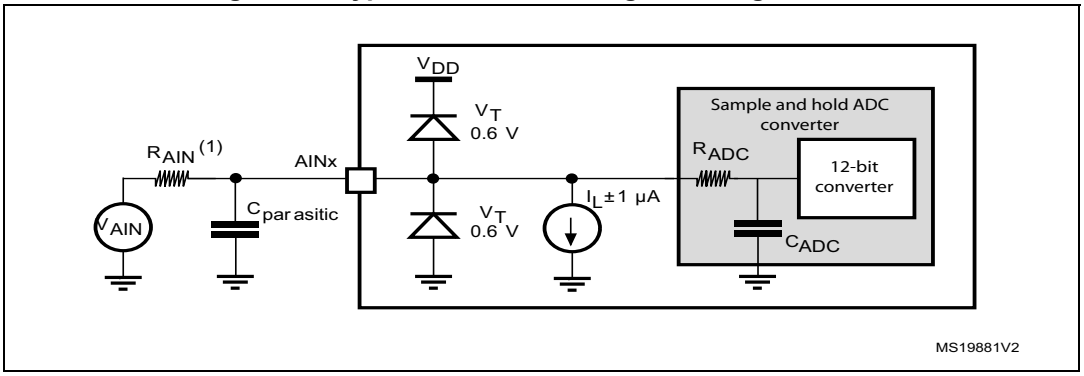


Figure 31. Typical connection diagram using the ADC



1. Refer to *Table 64* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.21 Operational amplifier characteristics

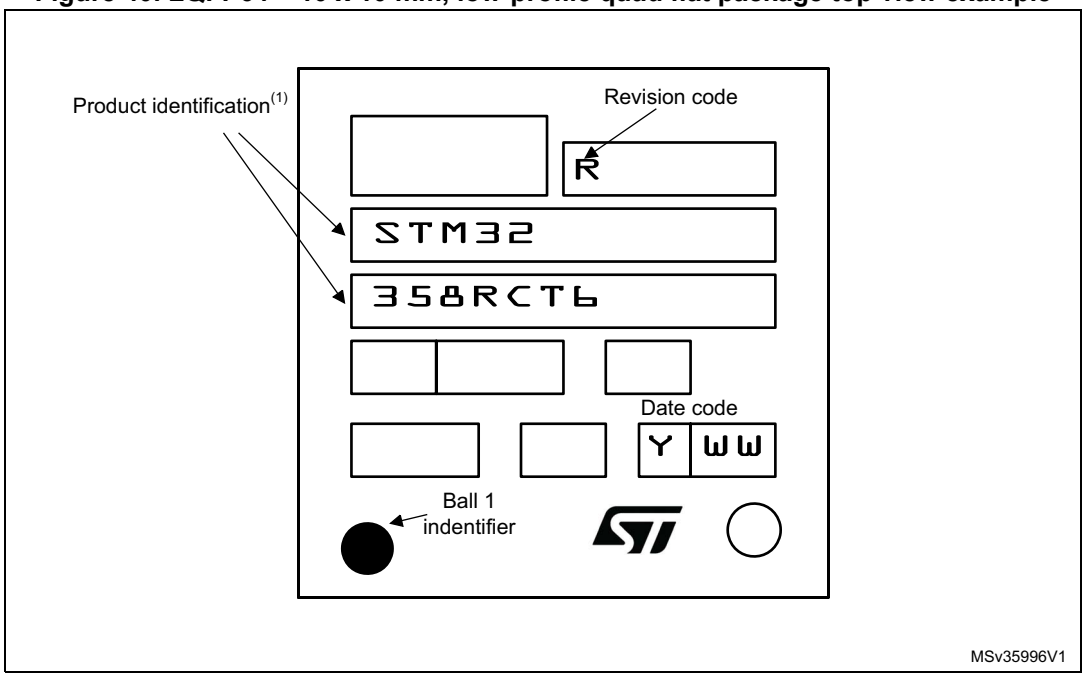
Table 73. Operational amplifier characteristics(1)

Symbol	Parameter		Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	Maximum calibration range	25°C, No Load on output.	-	-	4	mV
			All voltage/Temp.	-	-	6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	-	-	3	
ΔVI_{OFFSET}	Input offset voltage drift		-	-	5	-	µV/°C
I_{LOAD}	Drive current		-	-	-	500	µA
IDDOPAMP	Consumption		No load, quiescent mode	-	690	1450	µA
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/µs
R_{LOAD}	Resistive load		-	4	-	-	kΩ
C_{LOAD}	Capacitive load		-	-	-	50	pF
VOH_{SAT}	High saturation voltage		R_{load} = min, Input at V_{DDA}.	-	-	100	mV
			R_{load} = 20K, Input at V_{DDA}.	-	-	20	
VOL_{SAT}	Low saturation voltage		Rload = min, input at 0V	-	-	100	
			Rload = 20K, input at 0V.	-	-	20	
φm	Phase margin		-	-	62	-	°
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy		-	-	-	2	ms
t_{WAKEUP}	Wake up time from OFF state.		C_{LOAD} ≤50 pf, R_{LOAD} ≥ 4 kΩ, Follower configuration	-	2.8	5	µs

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. LQFP64 – 10 x 10 mm, low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.