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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	86
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 4x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f358vct6

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2 Description

The STM32F358xC family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbytes of Flash memory, up to 48 Kbytes of SRAM) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer up to four fast 12-bit ADCs (5 Msps), up to seven comparators, up to four operational amplifiers, up to two DAC channels, a low-power RTC, up to five general-purpose 16-bit timers, one general-purpose 32-bit timer, and two timers dedicated to motor control. They also feature standard and advanced communication interfaces: up to two I^2Cs, up to three SPIs (two SPIs are with multiplexed full-duplex I2Ss on STM32F358xC devices), three USARTs, up to two UARTs, and CAN. To achieve audio class accuracy, the I2S peripherals can be clocked via an external PLL.

The STM32F358xC family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F358xC family offers devices in three packages ranging from 48 pins to 100 pins.

The set of included peripherals changes with the device chosen.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 9* for the features available in SPI1, SPI2 and SPI3.

Table 9. STM32F358xC SPI/I2S implementation

SPI features(1)	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	-	X	X
TI mode	X	X	X

1. X = supported.

3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.24 Infrared Transmitter

The STM32F358xC devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below. TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		POR	External power on reset pin with embedded weak pull-up resistor, powered from VDDA
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 18. Alternate functions for port E

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF6	AF7
PE0	-	EVENTOUT	TIM4_ETR	-	TIM16_CH1	-	USART1_TX
PE1	-	EVENTOUT	-	-	TIM17_CH1	-	USART1_RX
PE2	TRACECK	EVENTOUT	TIM3_CH1	TSC_G7_IO1	-	-	-
PE3	TRACED0	EVENTOUT	TIM3_CH2	TSC_G7_IO2	-	-	-
PE4	TRACED1	EVENTOUT	TIM3_CH3	TSC_G7_IO3	-	-	-
PE5	TRACED2	EVENTOUT	TIM3_CH4	TSC_G7_IO4	-	-	-
PE6	TRACED3	EVENTOUT	-	-	-	-	-
PE7	-	EVENTOUT	TIM1_ETR	-	-	-	-
PE8	-	EVENTOUT	TIM1_CH1N	-	-	-	-
PE9	-	EVENTOUT	TIM1_CH1	-	-	-	-
PE10	-	EVENTOUT	TIM1_CH2N	-	-	-	-
PE11	-	EVENTOUT	TIM1_CH2	-	-	-	-
PE12	-	EVENTOUT	TIM1_CH3N	-	-	-	-
PE13	-	EVENTOUT	TIM1_CH3	-	-	-	-
PE14	-	EVENTOUT	TIM1_CH4	-	-	TIM1_BKIN2	-
PE15	-	EVENTOUT	TIM1_BKIN	-	-	-	USART3_RX

5 Memory mapping

Figure 7. STM32F358xC memory map

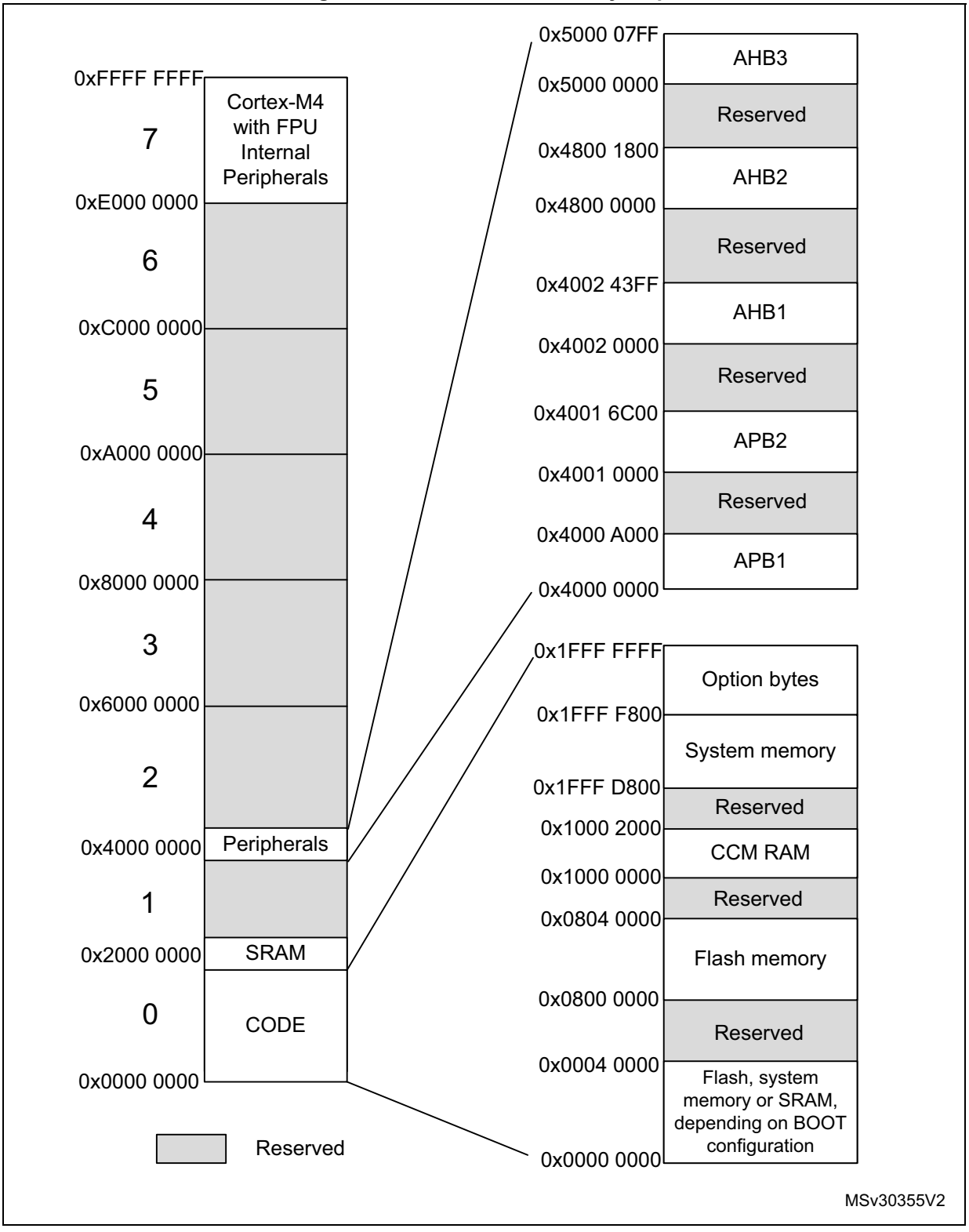


Table 20. STM32F358xC memory map and peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
	0x4000 8000 - 0x4000 FFFF	32 K	Reserved
APB1	0x4000 7800 - 0x4000 7FFF	2 K	Reserved
	0x4000 7400 - 0x4000 77FF	1 K	DAC (dual)
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6C00 - 0x4000 6FFF	1 K	Reserved
	0x4000 6800 - 0x4000 6BFF	1 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 5C00 - 0x4000 63FF	2 K	Reserved
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1400 - 0x4000 17FF	1 K	TIM7
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 1.8 V, V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

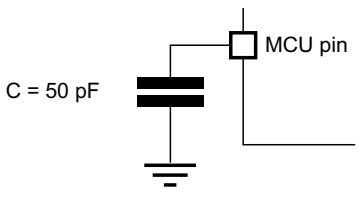


Figure 9. Pin input voltage

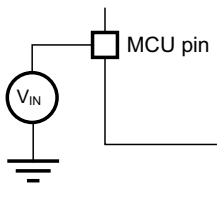


Table 22. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)	160	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)	–160	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	–100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	–25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	–80	
$I_{INJ(PIN)}$	Injected current on FT, FTf, POR and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 21: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 66*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

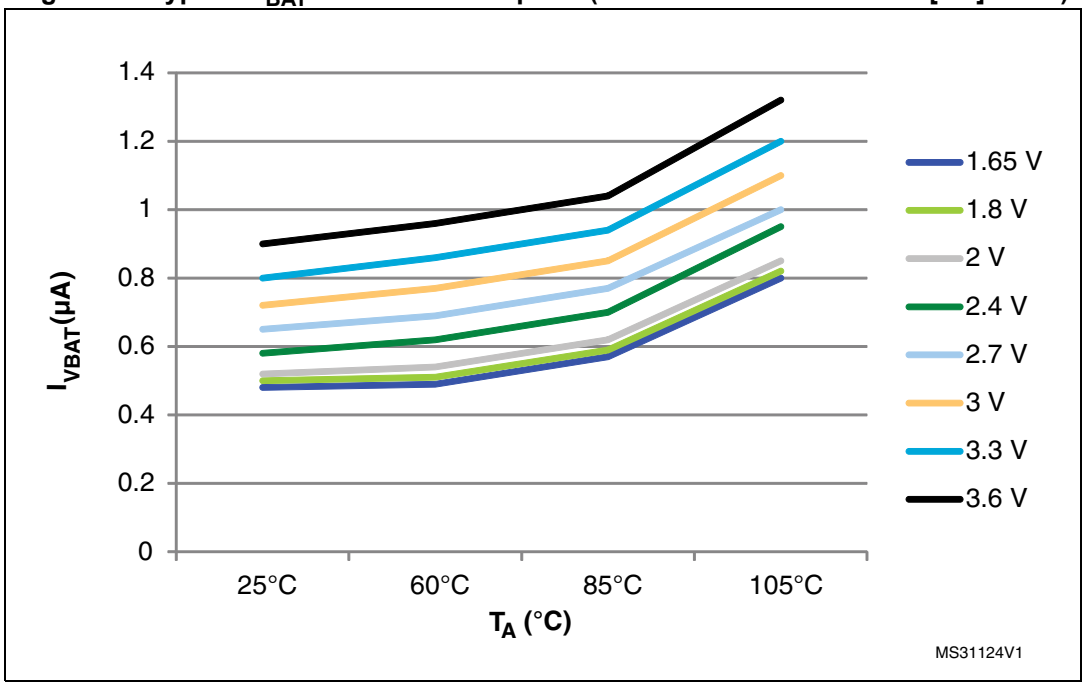
Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 1.8 V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	60.4	65.4	66.6	67.8	27.3	29.6	30.3	31.0	mA
			64 MHz	54.1	58.6	59.8	60.9	24.5	26.5	27.3	27.9	
			48 MHz	41.5	45.0	46.1	47.0	18.8	20.4	21.0	21.7	
			32 MHz	28.2	30.6	31.6	32.4	12.9	14.0	14.5	15.1	
			24 MHz	21.5	23.4	24.2	24.9	9.8	10.8	11.3	11.8	
			8 MHz	7.2	8.0	8.6	9.1	3.3	3.8	4.1	4.8	
			1 MHz	1.1	1.4	1.6	2.4	0.6	0.8	1.1	1.9	
		Internal clock (HSI)	64 MHz	49.4	53.6	54.6	55.7	24.3	26.3	27.0	27.6	
			48 MHz	37.9	41.2	42.1	43.0	18.6	20.3	20.8	21.4	
			32 MHz	25.8	28.1	29.0	29.7	12.7	13.9	14.4	14.9	
			24 MHz	19.7	21.4	22.3	22.9	6.6	7.3	7.8	8.3	
			8 MHz	6.8	7.5	8.0	8.6	3.3	3.7	4.1	4.8	
	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	61.3	66,5(2)	67.6	68,9(2)	28.3	30,6(2)	31.5	32,2(2)	
			64 MHz	54.9	59.5	60.6	61.9	25.3	27.4	28.1	28.8	
			48 MHz	41.7	45.3	46.4	47.3	19.1	20.7	21.3	22.0	
			32 MHz	28.2	30.7	31.7	32.4	12.8	14.0	14.6	15.1	
			24 MHz	21.3	23.2	24.0	24.7	9.7	10.6	11.1	11.6	
			8 MHz	7.0	7.8	8.3	8.9	3.1	3.4	4.0	4.6	
			1 MHz	0.7	0.9	1.3	2.1	0.2	0.4	0.8	1.5	
		Internal clock (HSI)	64 MHz	50.0	54.2	55.4	56.5	24.9	27.0	27.7	28.3	
			48 MHz	38.0	41.3	42.3	43.2	18.7	20.4	21.0	21.6	
			32 MHz	25.7	27.9	28.8	29.6	12.6	13.7	14.2	14.8	
			24 MHz	19.4	21.1	22.0	22.6	6.3	7.0	7.4	8.0	
			8 MHz	6.4	7.2	7.7	8.2	3.0	3.3	3.9	4.4	

Figure 12. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')



Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = 1.8 V, V_{DDA} = 3.3 V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

6.3.7 Internal clock source characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24*.

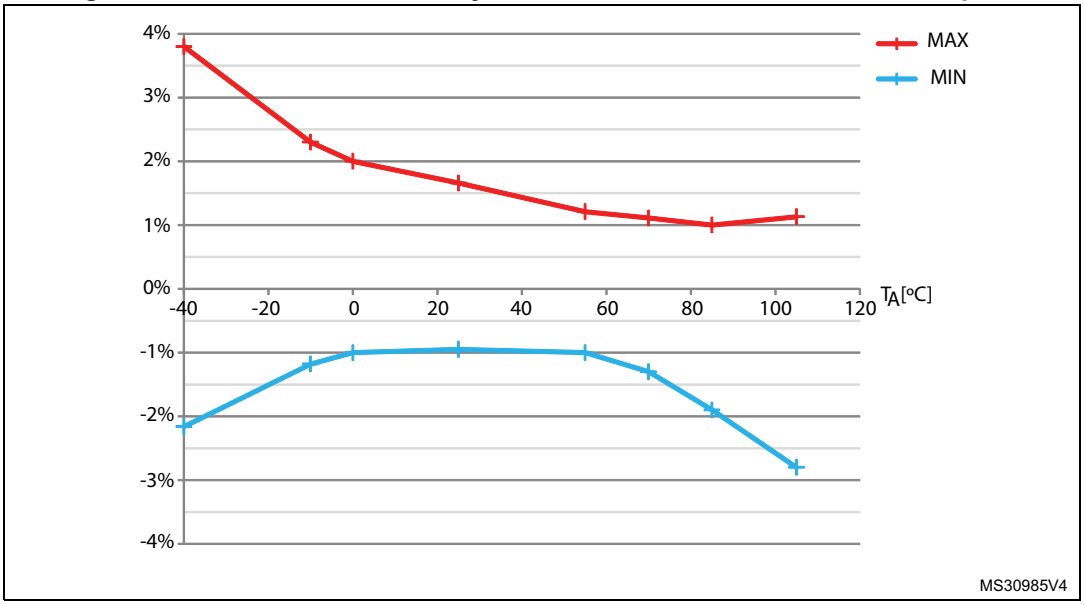
High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 17. HSI oscillator accuracy characterization results for soldered parts



Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 50. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 51*

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 20* and *Table 54*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 54. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	1	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	4(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	62.5(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	62.5(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	10(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	25(3)	
FM+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	0.5(4)(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	16(4)(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	44(4)(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0316 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 20*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the RM0316 STM32F303xx, STM32F358xC and STM32F328x4/6/8 reference manual (RM0316) for a description of FM+ I/O mode configuration.

Table 57. TIMx(1)(2) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
		$f_{TIMxCLK}$ = 144 MHz, x= 1.8	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
		$f_{TIMxCLK}$ = 144 MHz, x= 1.8	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIMxCLK}$ = 144 MHz, x= 1.8	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM6, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.

6.3.18 ADC characteristics

Unless otherwise specified, the parameters given in *Table 64* to *Table 67* are guaranteed by design, with conditions summarized in *Table 24*.

Table 64. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	1.8	-	3.6	V
I_{DDA}	ADC current consumption on VDDA pin (see *Figure 28*)	Single-ended mode, 5 MSPS	-	907	1033.0	µA
		Single-ended mode, 1 MSPS	-	194	285.5	
		Single-ended mode, 200 KSPS	-	51.5	70	
		Differential mode, 5 MSPS	-	887.5	1009	
		Differential mode, 1 MSPS	-	212	285	
		Differential mode, 200 KSPS	-	51	69.5	
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
I_{REF}	ADC current consumption on VREF+ pin (see *Figure 29*)	Single-ended mode, 5 MSPS	-	104	139	µA
		Single-ended mode, 1 MSPS	-	20.4	37	
		Single-ended mode, 200 KSPS	-	3.3	11.3	
		Differential mode, 5 MSPS	-	174	235	
		Differential mode, 1 MSPS	-	34.6	52.6	
		Differential mode, 200 KSPS	-	6	13.6	
f_{ADC}	ADC clock frequency		0.14	-	72	MHz
f_S (1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	

Table 67. ADC accuracy, 100-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min(4)	Max(4)	Unit
SINAD	Signal-to-noise and distortion ratio	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps, 1.8V ≤ V_{DDA}, V_{REF+} ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	-	64	dB
				Slow channel 4.8 Ms	-	63	
			Differential	Fast channel 5.1 Ms	-	67	
				Slow channel 4.8 Ms	-	67	
SNR	Signal-to-noise ratio		Single Ended	Fast channel 5.1 Ms	64	-	
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD	Total harmonic distortion		Single Ended	Fast channel 5.1 Ms	-	-74	
				Slow channel 4.8 Ms	-	-74	
			Differential	Fast channel 5.1 Ms	-	-78	
				Slow channel 4.8 Ms	-	-76	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

6.3.20 Comparator characteristics

Table 72. Comparator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	V_{REFINT} scaler not in use		1.65	-	3.6	V
		V_{REFINT} scaler in use		2	-	3.6	
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-		-	1.2	-	
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1(2)	s
		Next activations		-	-	0.2	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low-power mode		-	2	4.5	µs
		Low-power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low-power mode		-	2	7	µs
		Low-power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low-power mode		-	1.2	1.5	µA
		Low-power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

Table 72. Comparator characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

1. Data based on characterization results, not tested in production.
2. For more details and conditions, see *Figure 33* Maximum V_{REFINT} scaler startup time from power down.

Figure 33. Maximum V_{REFINT} scaler startup time from power down

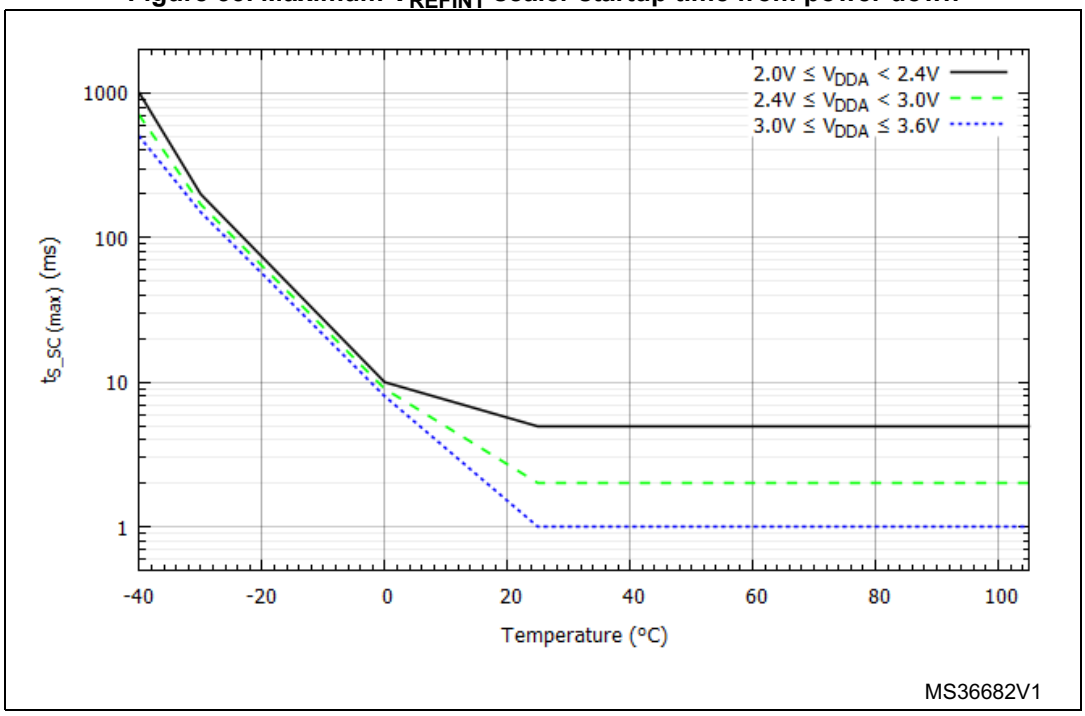
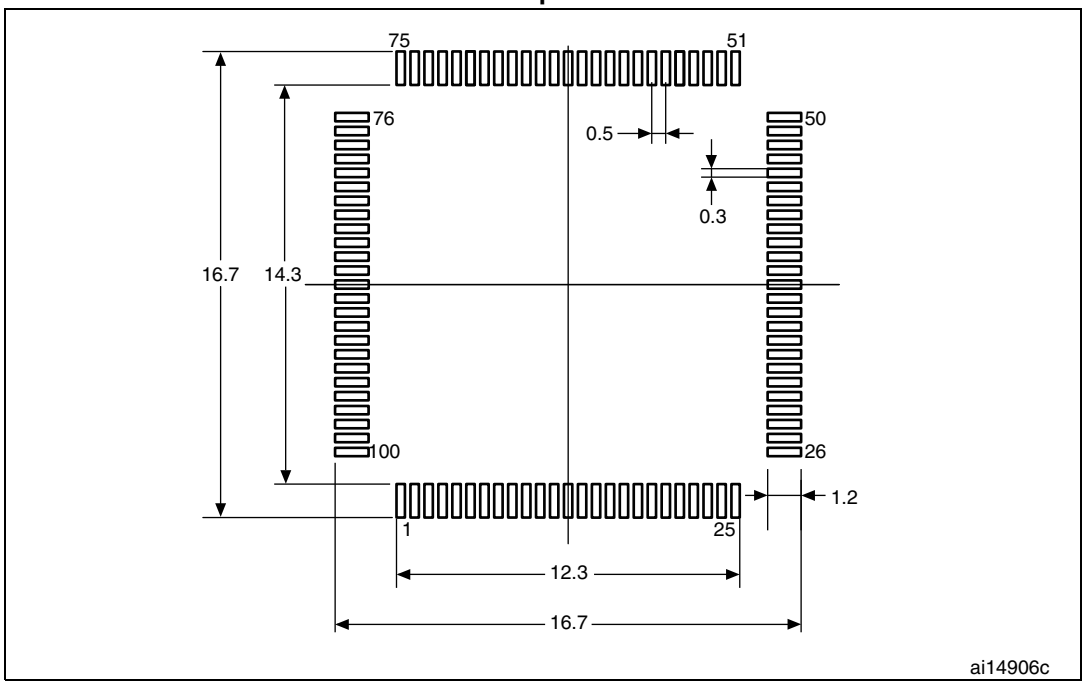


Table 77. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.2	0.0035	-	0.0079
D	15.80	16.00	16.2	0.622	0.6299	0.6378
D1	13.80	14.00	14.2	0.5433	0.5512	0.5591
D3	-	12.00	-	-	0.4724	-
E	15.80	16.00	16.2	0.622	0.6299	0.6378
E1	13.80	14.00	14.2	0.5433	0.5512	0.5591
E3	-	12.00	-	-	0.4724	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. LQFP100 – 14 x 14 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.