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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s912zvh64f2clq

Feature	MC9S12ZVH128		MC9S12ZVH64
Frequency modulated PLL	Yes		Yes
Internal 1 MHz RC oscillator	Yes		Yes
Autonomous window watchdog	1 (with independent clock source)		1 (with independent clock source)
Direct Battery Voltage sense pin	Yes		Yes
Vsup sense	Yes		Yes
Chip temperature sensor	1 General sensor		1 General sensor
VSUP Supply voltage	5.5 V – 18 V (normal operation) up to 40V (protected operation)		5.5 V – 18 V (normal operation) up to 40V (protected operation)
VDDX Output current	Determined by power dissipation of external ballast		Determined by power dissipation of external ballast
Maximum Bus Frequency	32 MHz		32 MHz
Package	100 pins (LQFP)	144 pins (LQFP)	144 pins (LQFP)

1. The channles show here just reflect the avaiable IOC pins, the timer are still 2 x 8 channles

1.3 Maskset 0N65E and 1N65E device compare

0N65E and 1N65E devices have difference on some module versions. Table 1-3 shows the difference.

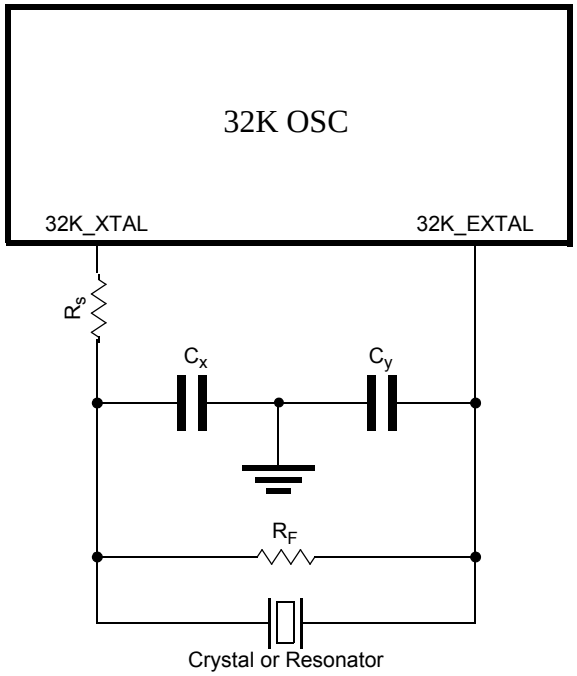


Figure 1-3. 32K OSC Crystal/Resonator Connection

1.8.2.32.3 API_EXTCLK

This signal is associated with the output of the API.

1.8.2.32.4 ECLK

This signal is associated with the output of the divided bus clock (ECLK).

NOTE

This feature is only intended for debug purposes at room temperature.
It must not be used for clocking external devices in an application.

1.8.2.33 BDC and Debug Signals

1.8.2.33.1 BKGD — Background Debug signal

The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. The BKGD signal has an internal pull-up device.

1.8.2.33.2 PDO — Profiling Data Output

This is the profiling data output signal used when the DBG module profiling feature is enabled. This signal is output only and provides a serial, encoded data stream that can be used by external development tools to reconstruct the internal CPU code flow.

2.3.2.4 ECLK Control Register (ECLKCTL)

Address 0x0208 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	NECLK	0	0	0	0	0	0	0
W								
Reset:	1	0	0	0	0	0	0	0

Figure 2-5. ECLK Control Register (ECLKCTL)

1. Read: Anytime
   Write: Anytime

Table 2-6. ECLKCTL Register Field Descriptions

Field	Description
7 NECLK	**No ECLK** — Disable ECLK output This bit controls the availability of a free-running clock on the ECLK pin. This clock has a fixed rate equivalent to the internal bus clock. 1 ECLK disabled 0 ECLK enabled

2.3.2.5 IRQ Control Register (IRQCR)

Address 0x0209 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	IRQE	IRQEN	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-6. IRQ Control Register (IRQCR)

1. Read: Anytime
   Write:
   IRQE: Once in normal mode, anytime in special mode
   IR QEN: Anytime

1. To use the digital input function the related bit in Digital Input Enable Register (DIENADx) must be set to logic level “1”. To use the digital input function the related bit in Slew Rate Register (SRRx) must be set to logic level “0”.

2.4.2.1 Data register (PTx)

This register holds the value driven out to the pin if the pin is used as a general-purpose I/O.

Writing to this register has only an effect on the pin if the pin is used as general-purpose output. When reading this address, the synchronized state of the pin is returned if the associated data direction register bits are configured as input.

If the data direction register bits are configured as output, the contents of the data register is returned. This is independent of any other configuration (Figure 2-23).

2.4.2.2 Input register (PTIx)

This register is read-only and always returns the synchronized state of the pin (Figure 2-23).

2.4.2.3 Data direction register (DDRx)

This register defines whether the pin is used as an general-purpose input or an output.

If a peripheral module controls the pin the contents of the data direction register is ignored (Figure 2-23).

Independent of the pin usage with a peripheral module this register determines the source of data when reading the associated data register address (Section 2.4.2.1, “Data register (PTx)”).

NOTE

Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on port data or port input registers, when changing the data direction register.

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x00001D	INT_CFDATA5	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x00001E	INT_CFDATA6	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x00001F	INT_CFDATA7	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								

= Unimplemented or Reserved

Figure 4-2. INT Register Summary

4.3.2.1 Interrupt Vector Base Register (IVBR)

Address: 0x000010

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IVB_ADDR[15:1]															0
W																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Figure 4-3. Interrupt Vector Base Register (IVBR)

Read: Anytime

Write: Anytime

Table 4-4. IVBR Field Descriptions

Field	Description
15–1 IVB_ADDR [15:1]	**Interrupt Vector Base Address Bits** — These bits represent the upper 15 bits of all vector addresses. Out of reset these bits are set to 0xFFFE (i.e., vectors are located at 0xFFFE00–0xFFFFFF). **Note:** A system reset will initialize the interrupt vector base register with “0xFFFE” before it is used to determine the reset vector address. Therefore, changing the IVBR has no effect on the location of the reset vector (0xFFFFFC–0xFFFFFF).

4.3.2.2 Interrupt Request Configuration Address Register (INT_CFADDR)

Address: 0x000017

	7	6	5	4	3	2	1	0
R	0	INT_CFADDR[6:3]				0	0	0
W								
Reset	0	0	0	0	1	0	0	0

= Unimplemented or Reserved

Figure 4-4. Interrupt Configuration Address Register (INT_CFADDR)

Read: Anytime

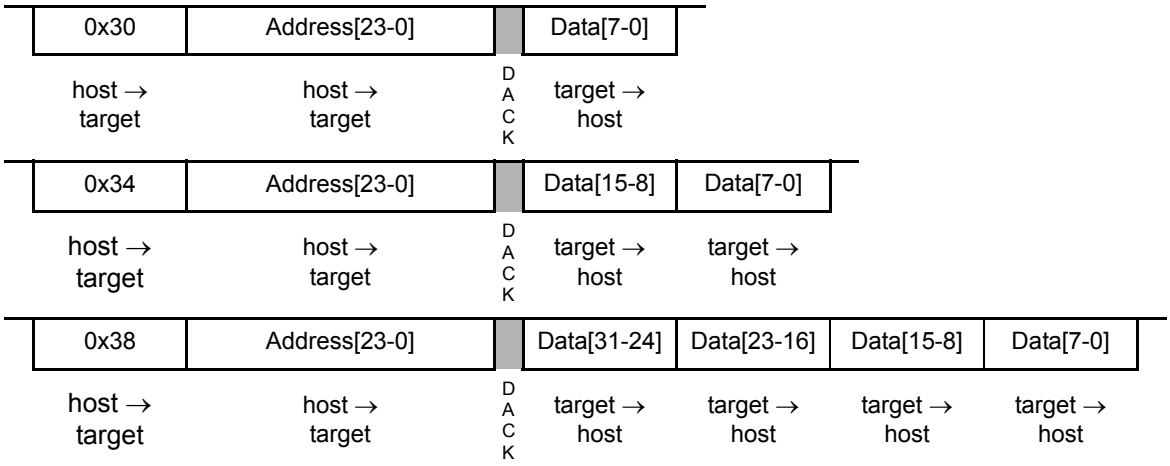
zero. The register is addressed through the CPU register number (CRN). See Section 5.4.5.1 for the CRN address decoding. If enabled, an ACK pulse is driven before the data bytes are transmitted.

If the device is not in active BDM, this command is illegal, the ILLCMD bit is set and no access is performed.

5.4.4.11 READ_MEM.sz, READ_MEM.sz_WS

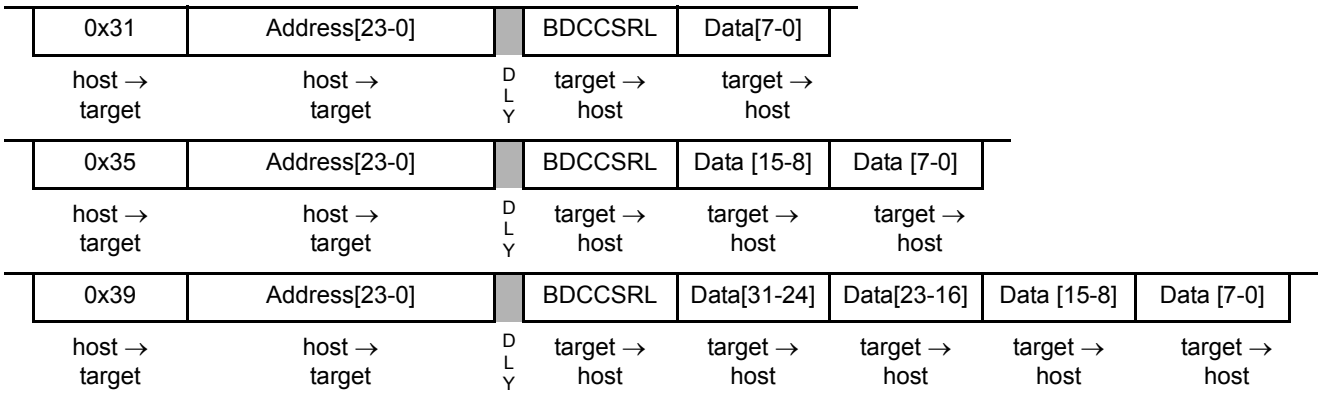
READ_MEM.sz

Read memory at the specified address **Non-intrusive**



READ_MEM.sz_WS

Read memory at the specified address with status **Non-intrusive**



Read data at the specified memory address. The address is transmitted as three 8-bit packets (msb to lsb) immediately after the command.

The hardware forces low-order address bits to zero longword accesses to ensure these accesses are on 0-modulo-size alignments. Byte alignment details are described in Section 5.4.5.2”. If the with-status option is specified, the BDCCSR status byte is returned before the read data. This status byte reflects the state

6.3.2.3 Debug Trace Control Register High (DBGTCRH)

Address: 0x0102

	7	6	5	4	3	2	1	0
R W	reserved	TSOURCE	TRANGE		TRCMOD		TALIGN	
Reset	0	0	0	0	0	0	0	0

Figure 6-5. Debug Trace Control Register (DBGTCRH)

Read: Anytime.

Write: Anytime the module is disarmed and PTACT is clear.

This register configures the trace buffer for tracing and profiling.

Table 6-8. DBGTCRH Field Descriptions

Field	Description
6 TSOURCE	**Trace Control Bits** — The TSOURCE enables the tracing session. 0 No CPU tracing/profiling selected 1 CPU tracing/profiling selected
5–4 TRANGE	**Trace Range Bits** — The TRANGE bits allow filtering of trace information from a selected address range when tracing from the CPU in Detail mode. These bits have no effect in other tracing modes. To use a comparator for range filtering, the corresponding COMPE bit must remain cleared. If the COMPE bit is set then the comparator is used to generate events and the TRANGE bits have no effect. See Table 6-9 for range boundary definition.
3–2 TRCMOD	**Trace Mode Bits** — See Section 6.4.5.2 for detailed Trace Mode descriptions. In Normal Mode, change of flow information is stored. In Loop1 Mode, change of flow information is stored but redundant entries into trace memory are inhibited. In Detail Mode, address and data for all memory and register accesses is stored. See Table 6-10.
1–0 TALIGN	**Trigger Align Bits** — These bits control whether the trigger is aligned to the beginning, end or the middle of a tracing or profiling session. See Table 6-11.

Table 6-9. TRANGE Trace Range Encoding

TRANGE	Tracing Range
00	Trace from all addresses (No filter)
01	Trace only in address range from $00000 to Comparator D
10	Trace only in address range from Comparator C to $FFFFFF
11	Trace only in range from Comparator C to Comparator D

Table 6-10. TRCMOD Trace Mode Bit Encoding

TRCMOD	Description
00	Normal
01	Loop1

Table 7-2. CPMURFLG Field Descriptions (continued)

Field	Description
1 OMRF	**Oscillator Clock Monitor Reset Flag** — OMRF is set to 1 when a loss of oscillator (crystal) clock occurs. Refer to7.5.3, “Oscillator Clock Monitor Reset for details.This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Loss of oscillator clock reset has not occurred. 1 Loss of oscillator clock reset has occurred.
0 PMRF	**PLL Clock Monitor Reset Flag** — PMRF is set to 1 when a loss of PLL clock occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Loss of PLL clock reset has not occurred. 1 Loss of PLL clock reset has occurred.

7.3.2.2 S12CPMU_UHV_V6 Synthesizer Register (CPMUSYNR)

The CPMUSYNR register controls the multiplication factor of the PLL and selects the VCO frequency range.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R W	VCOFRQ[1:0]				SYNDIV[5:0]			
Reset	0	1	0	1	1	0	0	0

Figure 7-5. S12CPMU_UHV_V6 Synthesizer Register (CPMUSYNR)

Read: Anytime

Write: If PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register), then write anytime. Else write has no effect.

NOTE

Writing to this register clears the LOCK and UPOSC status bits.

If PLL has locked (LOCK=1) $f_{VCO} = 2 \times f_{REF} \times (SYNDIV + 1)$

NOTE

f_{VCO} must be within the specified VCO frequency lock range. Bus frequency f_{bus} must not exceed the specified maximum.

The VCOFRQ[1:0] bits are used to configure the VCO gain for optimal stability and lock time. For correct PLL operation the VCOFRQ[1:0] bits have to be selected according to the actual target VCOCLK

Be aware that the output frequency varies with the TC trimming. A frequency trimming correction is therefore necessary. The values provided in Table 7-28 are typical values at ambient temperature which can vary from device to device.

7.3.2.22 S12CPMU_UHV_V6 Oscillator Register (CPMUOSC)

This registers configures the external oscillator (XOSCLCP).

Module Base + 0x001A

	7	6	5	4	3	2	1	0
R	OSCE	0	Reserved	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-31. S12CPMU_UHV_V6 Oscillator Register (CPMUOSC)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE.

Write to this register clears the LOCK and UPOSC status bits.

Module Base + 0x00006

	7	6	5	4	3	2	1	0
R W	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
Reset	0	0	0	0	0	0	0	0

Figure 9-9. PWM Clock Select Register (PWMCLK)

Read: Anytime

Write: Anytime

NOTE

Register bits PCLKAB0 to PCLKAB7 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Table 9-11. PWMCLK Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 PCLKAB7	**Pulse Width Channel 7 Clock A/B Select** 0 Clock B or SB is the clock source for PWM channel 7, as shown in Table 9-6. 1 Clock A or SA is the clock source for PWM channel 7, as shown in Table 9-6.
6 PCLKAB6	**Pulse Width Channel 6 Clock A/B Select** 0 Clock B or SB is the clock source for PWM channel 6, as shown in Table 9-6. 1 Clock A or SA is the clock source for PWM channel 6, as shown in Table 9-6.
5 PCLKAB5	**Pulse Width Channel 5 Clock A/B Select** 0 Clock A or SA is the clock source for PWM channel 5, as shown in Table 9-5. 1 Clock B or SB is the clock source for PWM channel 5, as shown in Table 9-5.
4 PCLKAB4	**Pulse Width Channel 4 Clock A/B Select** 0 Clock A or SA is the clock source for PWM channel 4, as shown in Table 9-5. 1 Clock B or SB is the clock source for PWM channel 4, as shown in Table 9-5.
3 PCLKAB3	**Pulse Width Channel 3 Clock A/B Select** 0 Clock B or SB is the clock source for PWM channel 3, as shown in Table 9-6. 1 Clock A or SA is the clock source for PWM channel 3, as shown in Table 9-6.
2 PCLKAB2	**Pulse Width Channel 2 Clock A/B Select** 0 Clock B or SB is the clock source for PWM channel 2, as shown in Table 9-6. 1 Clock A or SA is the clock source for PWM channel 2, as shown in Table 9-6.
1 PCLKAB1	**Pulse Width Channel 1 Clock A/B Select** 0 Clock A or SA is the clock source for PWM channel 1, as shown in Table 9-5. 1 Clock B or SB is the clock source for PWM channel 1, as shown in Table 9-5.
0 PCLKAB0	**Pulse Width Channel 0 Clock A/B Select** 0 Clock A or SA is the clock source for PWM channel 0, as shown in Table 9-5. 1 Clock B or SB is the clock source for PWM channel 0, as shown in Table 9-5.

The clock source of each PWM channel is determined by PCLKx bits in PWMCLK (see Section 9.3.2.3, “PWM Clock Select Register (PWMCLK)) and PCLKABx bits in PWMCLKAB as shown in Table 9-5 and Table 9-6.

9.3.2.8 PWM Scale A Register (PWMSCLA)

PWMSCLA is the programmable scale value used in scaling clock A to generate clock SA. Clock SA is generated by taking clock A, dividing it by the value in the PWMSCLA register and dividing that by two.

Clock SA = Clock A / (2 * PWMSCLA)

NOTE

When PWMSCLA = $00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLA).

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 9-10. PWM Scale A Register (PWMSCLA)

Read: Anytime

Write: Anytime (causes the scale counter to load the PWMSCLA value)

9.3.2.9 PWM Scale B Register (PWMSCLB)

PWMSCLB is the programmable scale value used in scaling clock B to generate clock SB. Clock SB is generated by taking clock B, dividing it by the value in the PWMSCLB register and dividing that by two.

Clock SB = Clock B / (2 * PWMSCLB)

NOTE

When PWMSCLB = $00, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLB).

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 9-11. PWM Scale B Register (PWMSCLB)

Read: Anytime

Write: Anytime (causes the scale counter to load the PWMSCLB value).

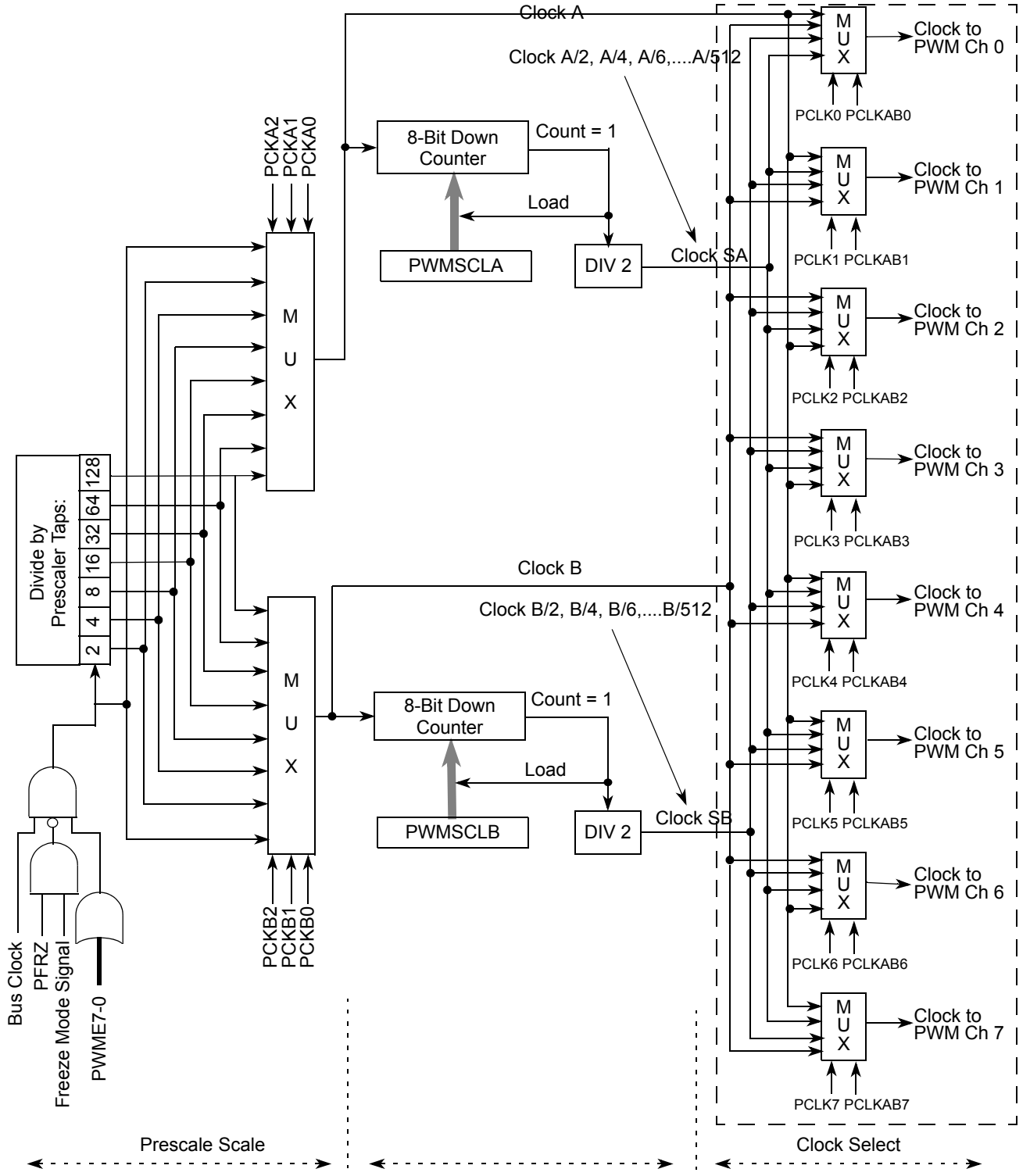


Figure 9-15. PWM Clock Select Block Diagram

10.4.2.11 ADC Conversion Interrupt Enable Register (ADCCONIE)

Module Base + 0x000A

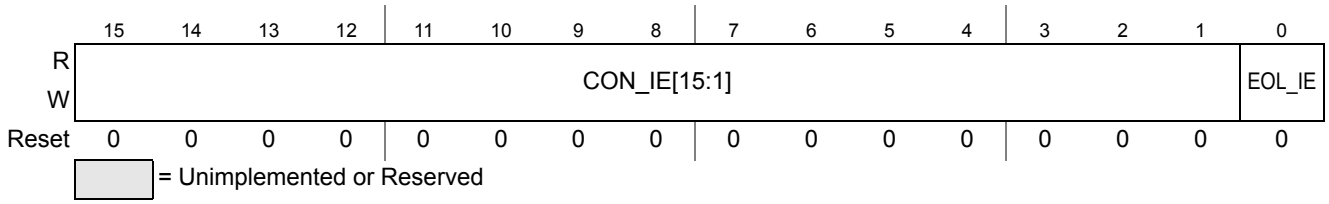


Figure 10-14. ADC Conversion Interrupt Enable Register (ADCCONIE)

Read: Anytime

Write: Anytime

Table 10-15. ADCCONIE Field Descriptions

Field	Description
15-1 CON_IE[15:1]	**Conversion Interrupt Enable Bits** — These bits enable the individual interrupts which can be triggered via interrupt flags CON_IF[15:1]. 0 ADC conversion interrupt disabled. 1 ADC conversion interrupt enabled.
0 EOL_IE	**End Of List Interrupt Enable Bit** — This bit enables the end of conversion sequence list interrupt. 0 End of list interrupt disabled. 1 End of list interrupt enabled.

11.2 External Signal Description

The MSCAN uses two external pins.

NOTE

On MCUs with an integrated CAN physical interface (transceiver) the MSCAN interface is connected internally to the transceiver interface. In these cases the external availability of signals TXCAN and RXCAN is optional.

11.2.1 RXCAN — CAN Receiver Input Pin

RXCAN is the MSCAN receiver input pin.

11.2.2 TXCAN — CAN Transmitter Output Pin

TXCAN is the MSCAN transmitter output pin. The TXCAN output pin represents the logic level on the CAN bus:

0 = Dominant state
1 = Recessive state

11.2.3 CAN System

A typical CAN system with MSCAN is shown in Figure 11-2. Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations.

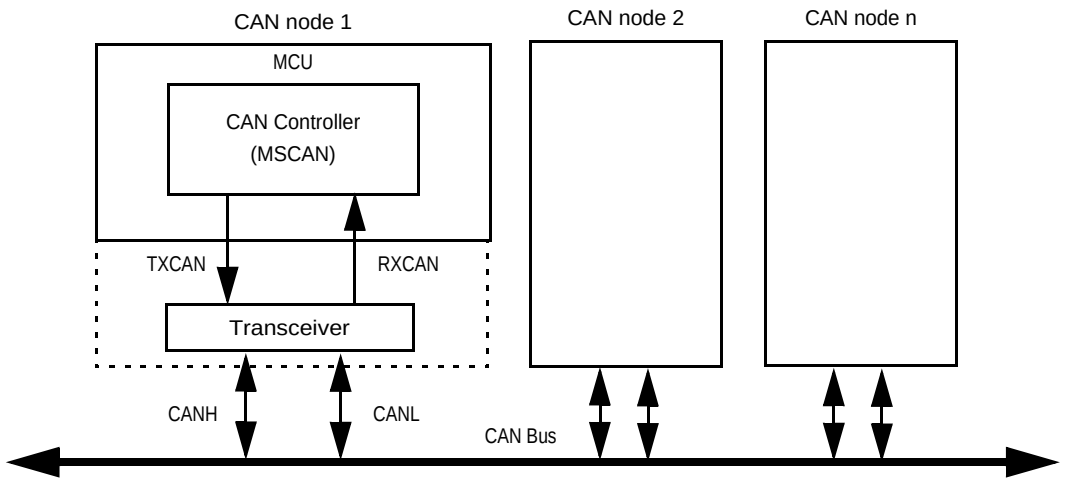


Figure 11-2. CAN System

15.5.3.1.6 RXEDGIF Description

The RXEDGIF interrupt is set when an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD pin is detected. Clear RXEDGIF by writing a “1” to the SCIASR1 SCI alternative status register 1.

15.5.3.1.7 BERRIF Description

The BERRIF interrupt is set when a mismatch between the transmitted and the received data in a single wire application like LIN was detected. Clear BERRIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if the bit error detect feature is disabled.

15.5.3.1.8 BKDIF Description

The BKDIF interrupt is set when a break signal was received. Clear BKDIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if break detect feature is disabled.

15.5.4 Recovery from Wait Mode

The SCI interrupt request can be used to bring the CPU out of wait mode.

15.5.5 Recovery from Stop Mode

An active edge on the receive input can be used to bring the CPU out of stop mode.

Chapter 17
Stepper Stall Detector (SSDV2) Block Description

Table 17-1. SSDV2 Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V02.00	1st Aug 2011		-remove the SMS bit in RTZCTL register

17.1 Introduction

The stepper stall detector (SSD) block provides a circuit to measure and integrate the induced voltage on the non-driven coil of a stepper motor using full steps when the gauge pointer is returning to zero (RTZ). During the RTZ event, the pointer is returned to zero using full steps in either clockwise or counter clockwise direction, where only one coil is driven at any point in time. The back electromotive force (EMF) signal present on the non-driven coil is integrated after a blanking time, and its results stored in a 16-bit accumulator. The 16-bit modulus down counter can be used to monitor the blanking time and the integration time. The value in the accumulator represents the change in linked flux (magnetic flux times the number of turns in the coil) and can be compared to a stored threshold. Values above the threshold indicate a moving motor, in which case the pointer can be advanced another full step in the same direction and integration be repeated. Values below the threshold indicate a stalled motor, thereby marking the cessation of the RTZ event.

17.1.1 Modes of Operation

- Return to zero modes
  - Blanking with no drive
  - Blanking with drive
  - Conversion
  - Integration
- Low-power modes

17.1.2 Features

- Programmable full step state
- Programmable integration polarity
- Blanking (recirculation) state
- 16-bit integration accumulator register

Table 17-11. SSDFLG Field Descriptions

Field	Description
7 MCZIF	**Modulus Counter Underflow Interrupt Flag** — This flag is set when the modulus down-counter reaches 0x0000. If not masked (MCZIE = 1), a modulus counter underflow interrupt is pending while this flag is set. This flag is cleared by writing a '1' to the bit. A write of '0' has no effect.
0 AOVIF	**Accumulator Overflow Interrupt Flag** — This flag is set when the Integration Accumulator has a positive or negative overflow. If not masked (AOVIE = 1), an accumulator overflow interrupt is pending while this flag is set. This flag is cleared by writing a '1' to the bit. A write of '0' has no effect.

17.3.2.5 Modulus Down-Counter Count Register (MDCCNT)

Module Base + 0x0004

	15	14	13	12	11	10	9	8
R W	MDCCNT							
Reset	1	1	1	1	1	1	1	1

Figure 17-6. Modulus Down-Counter Count Register High (MDCCNT)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R W	MDCCNT							
Reset	1	1	1	1	1	1	1	1

Figure 17-7. Modulus Down-Counter Count Register Low (MDCCNT)

Read: anytime

Write: anytime.

NOTE

A separate read/write for high byte and low byte gives a different result than accessing the register as a word.

If the RDMCL bit in the MDCCTL register is cleared, reads of the MDCCNT register will return the present value of the count register. If the RDMCL bit is set, reads of the MDCCNT register will return the contents of the load register.

With a 0x0000 write to the MDCCNT register, the modulus counter stays at zero and does not set the MCZIF flag in the SSDFLG register.

If modulus mode is not enabled (MODMC = 0), a write to the MDCCNT register immediately updates the load register and the counter register with the value written to it. The modulus counter will count down from this value and will stop at 0x0000.

If modulus mode is enabled (MODMC = 1), a write to the MDCCNT register updates the load register with the value written to it. The count register will not be updated with the new value until the next counter

20.2.2.3 ECC Interrupt Flag Register (ECCIF)

Module Base + 0x0002 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	SBEEIF
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime, write 1 to clear

Figure 20-4. ECC Interrupt Flag Register (ECCIF)

Table 20-4. ECCIF Field Description

Field	Description
0 SBEEIF	**Single bit ECC Error Interrupt Flag** — The flag is set to 1 when a single bit ECC error occurs. 0 No occurrences of single bit ECC error since the last clearing of the flag 1 Single bit ECC error occurs since the last clearing of the flag

Table 21-57. Valid Set User Margin Level Settings

FCCOB2	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level(1)
0x0002	User Margin-0 Level(2)

1. Read margin to the erased state
2. Read margin to the programmed state

Table 21-58. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 21-29)
		Set if an invalid global address [23:0] is supplied see Table 21-3)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

NOTE

User margin levels can be used to check that Flash memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking Flash memory contents at user margin levels, a potential loss of information has been detected.

21.4.7.13 Set Field Margin Level Command

The Set Field Margin Level command, valid in special modes only, causes the Memory Controller to set the margin level specified for future read operations of the P-Flash or EEPROM block.

Table 21-59. Set Field Margin Level Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0E	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] to identify Flash block	
FCCOB2	Margin level setting.	

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the field margin level for the targeted block and then set the CCIF flag.

comparator via an analog multiplexer. The pin itself is protected against reverse battery connections. To protect the pin from external fast transients an external resistor (R_{VSENSE_R}) is needed for protection.

23.2.2 VSUP — Voltage Supply Pin

This pin is the chip supply. It can be internally connected for voltage measurement. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC or to a comparator via an analog multiplexer.

23.3 Memory Map and Register Definition

This section provides the detailed information of all registers for the BATS module.

23.3.1 Register Summary

Figure 23-2 shows the summary of all implemented registers inside the BATS module.