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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvh64f2vlq

Chapter 1
Device Overview MC9S12ZVH-Family

Table 1-11. Interrupt Vector Locations (Sheet 2 of 3)

Vector Address[1]	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wake up from WAIT
Vector base + 0x18C	ADC0 Error	I bit	ADC0EIE(IA_EIE,CMD_EIE, EOL_EIE,TRIG_EIE,RSTAR_ EIE,LDOK_EIE) ADC0IE(CONIF_OIE)	No	Yes
Vector base + 0x188	ADC0 conversion sequence abort	I bit	ADC0IE(SEQAR_IE)	No	Yes
Vector base + 0x184	ADC0 conversion complete	I bit	ADC0CONIE[15:0]	No	Yes
Vector base + 0x180	Oscillator status interrupt	I bit	CPMUINT (OSCIE)	No	Yes
Vector base + 0x17C	PLL lock interrupt	I bit	CPMUINT (LOCKIE)	No	Yes
Vector base + 0x178 to Vector base + 0x174	Reserved				
Vector base + 0x170	RAM error	I bit	ECCIE (SBEEIE)	No	Yes
Vector base + 0x16C to Vector base + 0x168	Reserved				
Vector base + 0x164	FLASH error	I bit	FERCNFG (SFDIE)	No	Yes
Vector base + 0x160	FLASH command	I bit	FCNFG (CCIE)	No	Yes
Vector base + 0x15C	CAN0 wake-up	I bit	CAN0RIER (WUPIE)	Yes	Yes
Vector base + 0x158	CAN0 errors	I bit	CAN0RIER (CSCIE, OVRIE)	No	Yes
Vector base + 0x154	CAN0 receive	I bit	CAN0RIER (RXFIE)	No	Yes
Vector base + 0x150	CAN0 transmit	I bit	CAN0RIER (TXEIE[2:0])	No	Yes
Vector base + 0x14C to Vector base + 0x144	Reserved				
Vector base + 0x140	BATS supply voltage monitor interrupt	I bit	BATIE (BVHIE,BVLIE)	No	Yes
Vector base + 0x13C to Vector base + 0x130	Reserved				
Vector base + 0x12C	Port T interrupt	I bit	PIET(PIET[7:0])	Yes	Yes
Vector base + 0x128	CANPHY0 Interrupt (CP0I)	I bit	CP0IE(CPVFIE, CPOCIE)	No	Yes
Vector base + 0x124	Port S interrupt	I bit	PIES(PIES[7:0])	Yes	Yes
Vector base + 0x120 to Vector base + 0x108	Reserved				
Vector base + 0x104	Low-voltage interrupt (LVI)	I bit	CPMUCTRL (LVIE)	No	Yes
Vector base + 0x100	Autonomous periodical interrupt (API)	I bit	CPMUAPICTRL (APIE)	Yes	Yes
Vector base + 0xFC	High temperature interrupt	I bit	CPMUHTCTL(HTIE)	No	Yes
Vector base + 0xF8	Reserved				

Table 1-13. Initial WCOP Configuration

NV[3] in FOPT Register	WCOP in COPCTL Register
1	0
0	1

1.14 ADC0 Internal Channels

Table 1-14 lists the internal sources which are connected to these special conversion channels.

Table 1-14. ADC0 Channel Assignment

ADC0CMD_1 CH_SEL[5:0]							
[5]	[4]	[3]	[2]	[1]	[0]	**Analog Input Channel**	**Usage**
0	0	1	0	0	0	Internal_0	ADC temperature sensor
0	0	1	0	0	1	Internal_1	Bandgap Voltage V_{BG} or Vreg temperature sensor V_{HT}(see Chapter 7, “S12 Clock, Reset and Power Management Unit (S12CPMU_UHV_V6)“ on how to config)
0	0	1	0	1	0	Internal_2	RESERVED
0	0	1	0	1	1	Internal_3	RESERVED
0	0	1	1	0	0	Internal_4	V_{SENSE} or V_{SUP} selectable in BATS module
0	0	1	1	0	1	Internal_5	RESERVED
0	0	1	1	1	0	Internal_6	RESERVED
0	0	1	1	1	1	Internal_7	RESERVED

1.15 The ADC0 VRH/VRL

The ADC0 offers two possible sources for both reference voltages VRH[1:0] and VRL[1:0]. On the MC9S12ZVH-Family only VRH[1], VRL[1] sources are connected at device level(to VDDA, VSSA respectively), the VRH[0], VRL[0] sources are not connected. Thus the application must set both VRH_SEL and VRL_SEL in the 10.4.2.16 ADC Command Register 1 (ADCCMD_1) to 1.

1.16 The ADC0 Conversion Resolution

The MC9S12ZVH-Family only support 10 and 8 bit conversion resolution, although ADC block guide still has 12 bit related descrition.

Port	Pin Name	Pin Function & Priority[1]	I/O	Description	Routing Register	Pin Function after Reset
AD	PAD7	AN0_7	I	ADC0 analog input 7		GPIO
		PTADL[7]/ KWADL[7]	I/O	General-purpose; with interrupt and wakeup		
	PAD6	AN0_6	I	ADC0 analog input 6		
		PTADL[6]/ KWADL[6]	I/O	General-purpose; with interrupt and wakeup		
	PAD5	AN0_5	I	ADC0 analog input 5		
		PTADL[5]/ KWADL[5]	I/O	General-purpose; with interrupt and wakeup		
	PAD4	AN0_4	I	ADC0 analog input 4		
		PTADL[4]/ KWADL[4]	I/O	General-purpose; with interrupt and wakeup		
	PAD3	AN0_3	I	ADC0 analog input 3		
		PTADL[3]/ KWADL[3]	I/O	General-purpose; with interrupt and wakeup		
	PAD2	AN0_2	I	ADC0 analog input 2		
		PTADL[2]/ KWADL[2]	I/O	General-purpose; with interrupt and wakeup		
	PAD1	AN0_1	I	ADC0 analog input 1		
		PTADL[1]/ KWADL[1]	I/O	General-purpose; with interrupt and wakeup		
	PAD0	AN0_0	I	ADC0 analog input 0		
		PTADL[0]/ KWADL[0]	I/O	General-purpose; with interrupt and wakeup		

Port	Pin Name	Pin Function & Priority(1)	I/O	Description	Routing Register	Pin Function after Reset
U	PU[7]	M1SINP	I/O	SSD1 Sine+ Node		GPIO
		M1C1P	O	Motor control output for motor 1		
		PTU[7]	I/O	General purpose		
	PU[6]	M1SINM	I/O	SSD1 Sine- Node		
		M1C1M	O	Motor control output for motor 1		
		IOC0_3	I/O	TIM0 channel 3		
		PTU[6]	I/O	General purpose		
	PU[5]	M1COSP	I/O	SSD1 Cosine+ Node		
		M1C0P	O	Motor control output for motor 1		
		PTU[5]	I/O	General purpose		
	PU[4]	M1COSM	I/O	SSD1 Cosine- Node		
		M1C0M	O	Motor control output for motor 1		
		IOC0_2 I/O		TIM0 channel2		
		PTU[4]	I/O	General purpose		
	PU[3]	M0SINP	I/O	SSD0 Sine+ Node		
		M0C1P	O	Motor control output for motor 0		
		PTU[3]	I/O	General purpose		
	PU[2]	M0SINM	I/O	SSD0 Sine- Node		
		M0C1M	O	Motor control output for motor 0		
		IOC0_1	I/O	TIM0 channel 1		
		PTU[2]	I/O	General purpose		
	PU[1]	M0COSP	I/O	SSD0 Cosine+ Node		
		M0C0P	O	Motor control output for motor 0		
		PTU[1]	I/O	General purpose		
	PU[0]	M0COSM	I/O	SSD0 Cosine- Node		
		M0C0M	O	Motor control output for motor 0		
		IOC0_0	I/O	TIM0 channel 0		
		PTU[0]	I/O	General purpose		

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0281	PTADL	R	PTADL7	PTADL6	PTADL5	PTADL4	PTADL3	PTADL2	PTADL1	PTADL0
		W								
0x0282	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0283	PTIADL	R	PTIADL7	PTIADL6	PTIADL5	PTIADL4	PTIADL3	PTIADL2	PTIADL1	PTIADL0
		W								
0x0284	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0285	DDRADL	R	DDRADL7	DDRADL6	DDRADL5	DDRADL4	DDRADL3	DDRADL2	DDRADL1	DDRADL0
		W								
0x0286	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0287	PERADL	R	PERADL7	PERADL6	PERADL5	PERADL4	PERADL3	PERADL2	PERADL1	PERADL0
		W								
0x0288	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0289	PPSADL	R	PPSADL7	PPSADL6	PPSADL5	PPSADL4	PPSADL3	PPSADL2	PPSADL1	PPSADL0
		W								
0x028A–0x028B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028D	PIEADL	R	PIEADL7	PIEADL6	PIEADL5	PIEADL4	PIEADL3	PIEADL2	PIEADL1	PIEADL0
		W								
0x028E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028F	PIFADL	R	PIFADL7	PIFADL6	PIFADL5	PIFADL4	PIFADL3	PIFADL2	PIFADL1	PIFADL0
		W								
0x0290–0x0298	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0299	DIENADL	R	DIENADL7	DIENADL6	DIENADL5	DIENADL4	DIENADL3	DIENADL2	DIENADL1	DIENADL0
		W								

Table 6-18. DBGSCR2 Field Descriptions (continued)

Field	Description
5–4 C2SC[1:0]	Channel 2 State Control. These bits select the targeted next state whilst in State2 following a match2.
7–6 C3SC[1:0]	Channel 3 State Control. If EEVE !=10, these bits select the targeted next state whilst in State2 following a match3. If EEVE =10, these bits select the targeted next state whilst in State2 following an external event.

Table 6-19. State2 Match State Sequencer Transitions

CxSC[1:0]	Function
00	Match has no effect
01	Match forces sequencer to State1
10	Match forces sequencer to State3
11	Match forces sequencer to Final State

In the case of simultaneous matches, the match on the higher channel number (3...0) has priority.

6.3.2.9 Debug State Control Register 3 (DBGSCR3)

Address: 0x0109

	7	6	5	4	3	2	1	0
R W	C3SC1	C3SC0	C2SC1	C2SC0	C1SC1	C1SC0	C0SC1	C0SC0
Reset	0	0	0	0	0	0	0	0

Figure 6-11. Debug State Control Register 3 (DBGSCR3)

Read: Anytime.

Write: If DBG is not armed and PTACT is clear.

The state control register three selects the targeted next state whilst in State3. The matches refer to the outputs of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.12”. Comparators must be enabled by setting the comparator enable bit in the associated DBGxCTL control register.

Table 6-20. DBGSCR3 Field Descriptions

Field	Description
1–0 C0SC[1:0]	Channel 0 State Control. These bits select the targeted next state whilst in State3 following a match0.
3–2 C1SC[1:0]	Channel 1 State Control. These bits select the targeted next state whilst in State3 following a match1.
5–4 C2SC[1:0]	Channel 2 State Control. These bits select the targeted next state whilst in State3 following a match2.

Table 6-47. Normal and Loop1 Mode Trace Buffer Format without Timestamp

CPU	CINF1	CPCH1	CPCM1	CPCL1	CINF0	CPCH0	CPCM0	CPCL0
	CINF3	CPCH3	CPCM3	CPCL3	CINF2	CPCH2	CPCM2	CPCL2

Table 6-48. Normal and Loop1 Mode Trace Buffer Format with Timestamp

Mode	8-Byte Wide Trace Buffer Line							
	7	6	5	4	3	2	1	0
CPU	Timestamp	Timestamp	Reserved	Reserved	CINF0	CPCH0	CPCM0	CPCL0
	Timestamp	Timestamp	Reserved	Reserved	CINF1	CPCH1	CPCM1	CPCL1

CINF contains information relating to the CPU.

CPU Information Byte CINF For Normal And Loop1 Modes

Bit 7	it 6 B	Bit 5	it 4 B	Bit 3	it 2 B	Bit 1	it 0 B
CET		0	0	CTI	EEVI	0	TOVF

Figure 6-27. CPU Information Byte CINF

Table 6-49. CINF Bit Descriptions

Field	Description
7–6 CET	**CPU Entry Type Field** — Indicates the type of stored address of the trace buffer entry as described in Table 6-50
3 CTI	**Comparator Timestamp Indicator** — This bit indicates if the trace buffer entry corresponds to a comparator timestamp. 0 Trace buffer entry initiated by trace mode specification conditions or timestamp counter overflow 1 Trace buffer entry initiated by comparator D match
2 EEVI	**External Event Indicator** — This bit indicates if the trace buffer entry corresponds to an external event. 0 Trace buffer entry not initiated by an external event 1 Trace buffer entry initiated by an external event
0 TOVF	**Timestamp Overflow Indicator** — Indicates if the trace buffer entry corresponds to a timestamp overflow 0 Trace buffer entry not initiated by a timestamp overflow 1 Trace buffer entry initiated by a timestamp overflow

Table 6-50. CET Encoding

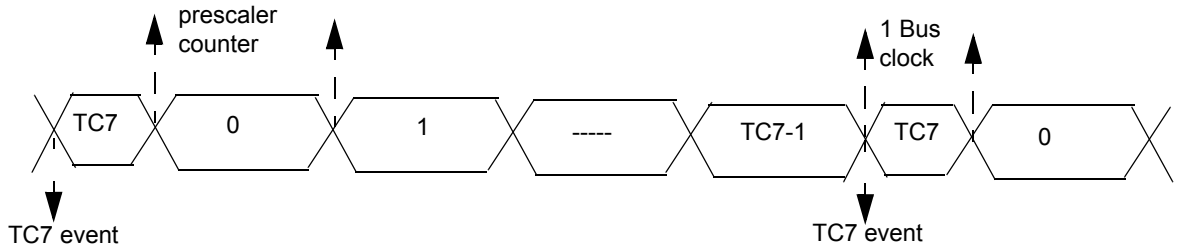
CET	Entry Type Description
00	Non COF opcode address (entry forced by an external event)
01	Vector destination address
10	Source address of COF opcode
11	Destination address of COF opcode

Writing to the timer port bit of an output compare pin does not affect the pin state. The value written is stored in an internal latch. When the pin becomes available for general-purpose output, the last value written to the bit appears at the pin.

When TCRE is set and TC7 is not equal to 0, then TCNT will cycle from 0 to TC7. When TCNT reaches TC7 value, it will last only one Bus cycle then reset to 0.

Note: in Figure 8-31,if PR[2:0] is equal to 0, one prescaler counter equal to one Bus clock

Figure 8-31. The TCNT cycle diagram under TCRE=1 condition



8.4.3.1 OC Channel Initialization

The internal register whose output drives OCx can be programmed before the timer drives OCx. The desired state can be programmed to this internal register by writing a one to CFORCx bit with TIOSx, OCPDx and TEN bits set to one.

Set OCx: Write a 1 to FOCx while TEN=1, IOSx=1, OMx=1, OLx=1 and OCPDx=1

Clear OCx: Write a 1 to FOCx while TEN=1, IOSx=1, OMx=1, OLx=0 and OCPDx=1

Setting OCPDx to zero allows the internal register to drive the programmed state to OCx. This allows a glitch free switch over of port from general purpose I/O to timer output once the OCPDx bit is set to zero.

8.4.4 Pulse Accumulator

The pulse accumulator (PACNT) is a 16-bit counter that can operate in two modes:

Event counter mode — Counting edges of selected polarity on the pulse accumulator input pin, PAI.

Gated time accumulation mode — Counting pulses from a divide-by-64 clock. The PAMOD bit selects the mode of operation.

The minimum pulse width for the PAI input is greater than two Bus clocks.

Table 10-2. ADCCTL_0 Field Descriptions (continued)

Field	Description
11-10 ACC_CFG[1:0]	**ADCFLWCTL Register Access Configuration** — These bits define if the register ADCFLWCTL is controlled via internal interface only or data bus only or both. See Table 10-3. for more details.
9 STR_SEQA	**Control Of Conversion Result Storage and RSTAR_EIF flag setting at Sequence Abort or Restart Event** — This bit controls conversion result storage and RSTAR_EIF flag setting when a Sequence Abort Event or Restart Event occurs as follows: *If STR_SEQA = 1'b0 and if a:* • Sequence Abort Event or Restart Event is issued during a conversion the data of this conversion is not stored and the respective conversion complete flag is not set • Restart Event only is issued before the last conversion of a CSL is finished and no Sequence Abort Event is in process (SEQA clear) causes the RSTA_EIF error flag to be asserted and bit SEQA gets set by hardware *If STR_SEQA = 1'b1 and if a:* • Sequence Abort Event or Restart Event is issued during a conversion the data of this conversion is stored and the respective conversion complete flag is set and Intermediate Result Information Register is updated. • Restart Event only occurs during the last conversion of a CSL and no Sequence Abort Event is in process (SEQA clear) does not set the RSTA_EIF error flag • Restart Event only is issued before the CSL is finished and no Sequence Abort Event is in process (SEQA clear) causes the RSTA_EIF error flag to be asserted and bit SEQA gets set by hardware
8 MOD_CFG	**(Conversion Flow Control) Mode Configuration** — This bit defines the conversion flow control after a Restart Event and after execution of the "End Of List" command type: - Restart Mode - Trigger Mode (For more details please see also section Section 10.5.3.2, "Introduction of the Programmer's Model and following.) 0 "Restart Mode" selected. 1 "Trigger Mode" selected.

Table 10-3. ADCFLWCTL Register Access Configurations

ACC_CFG[1]	ACC_CFG[0]	ADCFLWCTL Access Mode
0	0	None of the access paths is enabled (default / reset configuration)
0	1	Single Access Mode - Internal Interface (ADCFLWCTL access via internal interface only)
1	0	Single Access Mode - Data Bus (ADCFLWCTL access via data bus only)
1	1	Dual Access Mode (ADCFLWCTL register access via internal interface and data bus)

NOTE

Each conversion flow control bit (SEQA, RSTA, TRIG, LDOK) must be controlled by software or internal interface according to the requirements described in Section 10.5.3.2.4, "The two conversion flow control Mode Configurations and overview summary in Table 10-10.

Table 10-23. Analog Input Channel Select

CH_SEL[5]	CH_SEL[4]	CH_SEL[3]	CH_SEL[2]	CH_SEL[1]	CH_SEL[0]	Analog Input Channel
0	0	0	1	1	1	Reserved
0	0	1	0	0	0	Internal_0 (ADC temperature sense)
0	0	1	0	0	1	Internal_1 (Vreg_3v3 sense)
0	0	1	0	1	0	Internal_2
0	0	1	0	1	1	Internal_3
0	0	1	1	0	0	Internal_4
0	0	1	1	0	1	Internal_5
0	0	1	1	1	0	Internal_6
0	0	1	1	1	1	Internal_7
0	1	0	0	0	0	AN0
0	1	0	0	0	1	AN1
0	1	0	0	1	0	AN2
0	1	0	0	1	1	AN3
0	1	0	1	0	0	AN4
0	1	x	x	x	x	ANx
1	x	x	x	x	x	Reserved

NOTE

ANx in Table 10-23 is the maximum number of implemented analog input channels on the device. Please refer to the device overview of the reference manual for details regarding number of analog input channels.

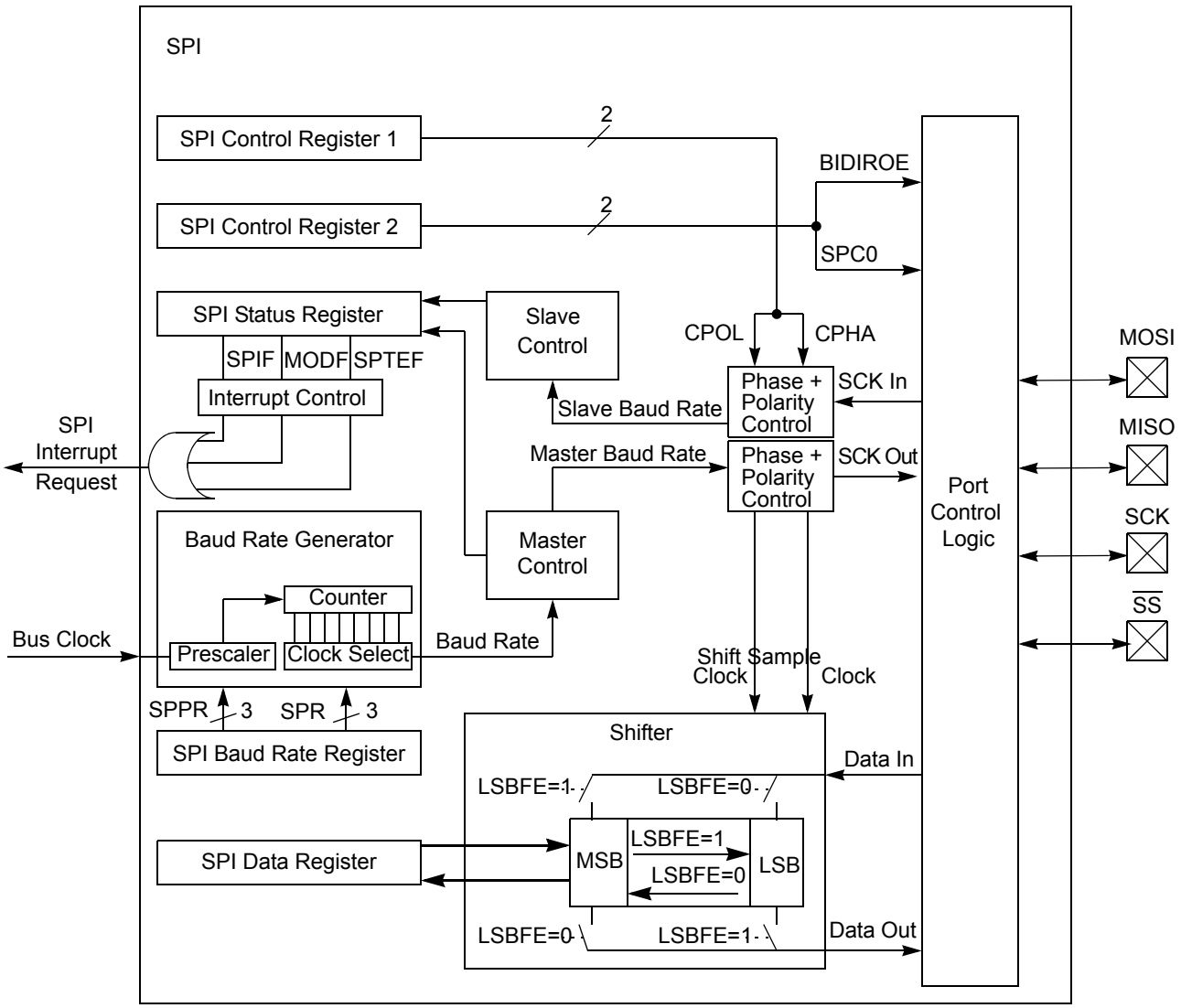


Figure 12-1. SPI Block Diagram

12.2 External Signal Description

This section lists the name and description of all ports including inputs and outputs that do, or may, connect off chip. The SPI module has a total of four external pins.

12.2.1 MOSI — Master Out/Slave In Pin

This pin is used to transmit data out of the SPI module when it is configured as a master and receive data when it is configured as slave.

12.2.2 MISO — Master In/Slave Out Pin

This pin is used to transmit data out of the SPI module when it is configured as a slave and receive data when it is configured as master.

14.3.2 Register Descriptions

This section consists of register descriptions. Each description includes a standard register diagram. Details of register bit and field function follow the register diagrams, in bit order.

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0000	LCDCR0	R W	LCDEN	0	0	LCLK1	LCLK0	BIAS	DUTY1	DUTY0
0x0001	LCDCR1	R W	0	0	0	0	0	0	LCDSWAI	LCDRSTP
0x0002	LCDFPENR0	R W	FP7EN	FP6EN	FP5EN	FP4EN	FP3EN	FP2EN	FP1EN	FP0EN
0x0003	LCDFPENR1	R W	FP15EN	FP14EN	FP13EN	FP12EN	FP11EN	FP10EN	FP9EN	FP8EN
0x0004	LCDFPENR2	R W	FP23EN	FP22EN	FP21EN	FP20EN	FP19EN	FP18EN	FP17EN	FP16EN
0x0005	LCDFPENR3	R W	FP31EN	FP30EN	FP29EN	FP28EN	FP27EN	FP26EN	FP25EN	FP24EN
0x0006	LCDFPENR4	R W	FP39EN	FP38EN	FP37EN	FP36EN	FP35EN	FP34EN	FP33EN	FP32EN
0x0007	Reserved	R W								
0x0008	LCDRAM0	R W	FP1BP3	FP1BP2	FP1BP1	FP1BP0	FP0BP3	FP0BP2	FP0BP1	FP0BP0
0x0009	LCDRAM1	R W	FP3BP3	FP3BP2	FP3BP1	FP3BP0	FP2BP3	FP2BP2	FP2BP1	FP2BP0
0x000A	LCDRAM2	R W	FP5BP3	FP5BP2	FP5BP1	FP5BP0	FP4BP3	FP4BP2	FP4BP1	FP4BP0
0x000B	LCDRAM3	R W	FP7BP3	FP7BP2	FP7BP1	FP7BP0	FP6BP3	FP6BP2	FP6BP1	FP6BP0
0x000C	LCDRAM4	R W	FP9BP3	FP9BP2	FP9BP1	FP9BP0	FP8BP3	FP8BP2	FP8BP1	FP8BP0
0x000D	LCDRAM5	R W	FP11BP3	FP11BP2	FP11BP1	FP11BP0	FP10BP3	FP10BP2	FP10BP1	FP10BP0
0x000E	LCDRAM6	R W	FP13BP3	FP13BP2	FP13BP1	FP13BP0	FP12BP3	FP12BP2	FP12BP1	FP12BP0
0x000F	LCDRAM7	R W	FP15BP3	FP15BP2	FP15BP1	FP15BP0	FP14BP3	FP14BP2	FP14BP1	FP14BP0

Figure 14-2. LCD40F4BV3 Register Summary

15.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Writes to a reserved register locations do not have any effect and reads of these locations return a zero. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 SCIBDH[1]	R	SBR15	SBR14	SBR13	SBR12	SBR11	SBR10	SBR9	SBR8
	W								
0x0001 SCIBDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
	W								
0x0002 SCICR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
	W								
0x0000 SCIASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
	W								
0x0001 SCIACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
	W								
0x0002 SCIACR2[2]	R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
	W								
0x0003 SCICR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
	W								
0x0004 SCISR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
	W								
0x0005 SCISR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
	W								
0x0006 SCIDRH	R	R8	T8	0	0	0	Reserved	Reserved	Reserved
	W								
0x0007 SCIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
	W	T7	T6	T5	T4	T3	T2	T1	T0

1.These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2,These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

= Unimplemented or Reserved

Figure 15-2. SCI Register Summary

When the transmit shift register is not transmitting a frame, the TXD pin goes to the idle condition, logic 1. If at any time software clears the TE bit in SCI control register 2 (SCICR2), the transmitter enable signal goes low and the transmit signal goes idle.

If software clears TE while a transmission is in progress (TC = 0), the frame in the transmit shift register continues to shift out. To avoid accidentally cutting off the last frame in a message, always wait for TDRE to go high after the last frame before clearing TE.

To separate messages with preambles with minimum idle line time, use this sequence between messages:

1. Write the last byte of the first message to SCIDRH/L.
2. Wait for the TDRE flag to go high, indicating the transfer of the last frame to the transmit shift register.
3. Queue a preamble by clearing and then setting the TE bit.
4. Write the first byte of the second message to SCIDRH/L.

15.4.5.3 Break Characters

Writing a logic 1 to the send break bit, SBK, in SCI control register 2 (SCICR2) loads the transmit shift register with a break character. A break character contains all logic 0s and has no start, stop, or parity bit. Break character length depends on the M bit in SCI control register 1 (SCICR1). As long as SBK is at logic 1, transmitter logic continuously loads break characters into the transmit shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character guarantees the recognition of the start bit of the next frame.

The SCI recognizes a break character when there are 10 or 11(M = 0 or M = 1) consecutive zero received. Depending if the break detect feature is enabled or not receiving a break character has these effects on SCI registers.

If the break detect feature is disabled (BKDFE = 0):

- Sets the framing error flag, FE
- Sets the receive data register full flag, RDRF
- Clears the SCI data registers (SCIDRH/L)
- May set the overrun flag, OR, noise flag, NF, parity error flag, PE, or the receiver active flag, RAF (see 3.4.4 and 3.4.5 SCI Status Register 1 and 2)

If the break detect feature is enabled (BKDFE = 1) there are two scenarios[1]

The break is detected right from a start bit or is detected during a byte reception.

- Sets the break detect interrupt flag, BKDIF
- Does not change the data register full flag, RDRF or overrun flag OR
- Does not change the framing error flag FE, parity error flag PE.
- Does not clear the SCI data registers (SCIDRH/L)
- May set noise flag NF, or receiver active flag RAF.

1. A Break character in this context are either 10 or 11 consecutive zero received bits

B.1.1.1 Port AD Output Drivers Switching

PortAD output drivers switching can adversely affect the ADC accuracy whilst converting the analog voltage on other PortAD pins because the output drivers are supplied from the VDDA/VSSA ADC supply pins. Although internal design measures are implemented to minimize the affect of output driver noise, it is recommended to configure PortAD pins as outputs only for low frequency, low load outputs. The impact on ADC accuracy is load dependent and not specified. The values specified are valid under condition that no PortAD output drivers switch during conversion.

B.1.1.2 Source Resistance

Due to the input pin leakage current as specified in conjunction with the source resistance there will be a voltage drop from the signal source to the ADC input. The maximum source resistance R_S specifies results in an error (10-bit resolution) of less than 1/2 LSB (2.5 mV) at the maximum leakage current.

B.1.1.3 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB (10-bit resilution), then the external filter capacitor, $C_f \geq 1024 * (C_{INS}–C_{INN})$.

B.1.1.4 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of 0x3FF (in 10-bit mode) for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

   The additional input voltage error on the converted channel can be calculated as:

   $$V_{ERR} = K * R_S * I_{INJ}$$

   with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table B-2. ADC Electrical Characteristics

Supply voltage 3.13 V < V_{DDA} < 5.5 V, -40°C < TJ < 150oC						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Max input source resistance	R_S	—	—	10	KΩ
2	Total input capacitance Non sampling Total input capacitance Sampling	C_{INN} C_{INS}	— —	— —	10 16	pF
3	Input internal Resistance	R_{INA}	-	5	15	kΩ
4	Disruptive analog input current	I_{NA}	-2.5	—	2.5	mA
5	Coupling ratio positive current injection	K_p	—	—	1E-4	A/A
6	Coupling ratio negative current injection	K_n	—	—	5E-3	A/A

Appendix J
S12CANPHY Electrical Specifications

J.1 Maximum Ratings

Table J-1. Maximum Ratings

Characteristics noted under conditions 5.5V <= VSUP <= 18 V, 4.75V <= VDDC <= 5.25V , -40°C < Tj < 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.				
Num	**Ratings**	**Symbol**	**Value**	**Unit**
1	DC voltage on CANL, CANH, SPLIT	V_{BUS}	-32 to +40	V
2	Continuous current on CANH and CANL	I_{LH}	200	mA
3	ESD on CANH, CANL and SPLIT (HBM)	V_{ESDCH}	± 2000	V
4	ESD on CANH, CANL (IEC61000-4, Czap = 150 pF, Rzap = 330 Ω)	V_{ESDIEC}	± 8000	V

J.2 Static Electrical Characteristics

Table J-2. Static Electrical Characteristics

Characteristics noted under conditions 5.5V <= VSUP <=18 V, 4.75V <= VDDC <= 5.25V >, -40°C <Tj < 150°C> unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
CAN TRANSCEIVER CURRENT						
1	Supply Current of canphy_ll18uhv Normal mode, Bus Recessive State Normal mode, Bus Dominant State without Bus Load Standby mode Shutdown mode	 I_{RES} I_{DOM} I_{STB} I_{SDN}		 1.7 2 0.022 0		mA
PINS (CANH AND CANL)						
2	Bus Pin Common Mode Voltage	V_{COM}	-12	-	12	V
3	Differential Input Voltage (after trim) Recessive State at RXD Dominant State at RXD	V_{CANH} - V_{CANL}	 -1.0 0.95	 - -	 0.55 5.0	V
4	Differential Input Hysteresis (RXD)	V_{HYS}		175		mV

0x0200–0x037F Port Integration Module(PIM)

0x02D8–0x02DE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02DF	WOMS	R	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		W								
0x02E0–0x02EF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F0	PTP	R	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		W								
0x02F1	PTIP	R	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		W								
0x02F2	DDRP	R	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		W								
0x02F3	PERP	R	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		W								
0x02F4	PPSP	R	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
		W								
0x02F5–0x02FF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0300	PTH	R	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		W								
0x0301	PTIH	R	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		W								
0x0302	DDRH	R	DDRH7	DDRH6	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		W								
0x0303	PERH	R	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
		W								
0x0304	PPSH	R	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
		W								
0x0305–0x030F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0310–0x031F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0320	PTG	R	PTG7	PTG6	PTG5	PTG4	PTG3	PTG2	PTG1	PTG0
		W								
0x0321	PTIG	R	PTIG7	PTIG6	PTIG5	PTIG4	PTIG3	PTIG2	PTIG1	PTIG0
		W								