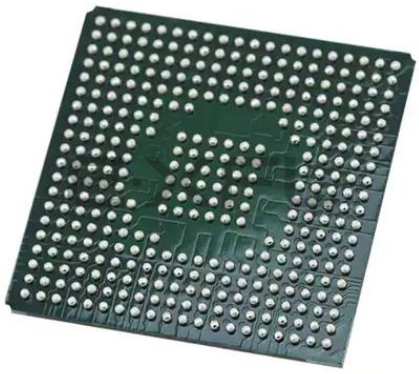


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Math Engine; MaverickCrunch™
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	352-BBGA
Supplier Device Package	352-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9312-cb

IDE Interface

The IDE Interface provides an industry-standard connection to two AT Advanced Packet Interface (ATAPI) compliant devices. The IDE port will attach to a master and a slave device. The internal DMA controller performs all data transfers using the Multiword DMA and Ultra DMA modes. The interface supports the following operating modes:

- PIO Modes 0 thru 4
- Ultra DMA Modes 0 thru 3

Table C. IDE Interface Pin Assignments

Pin Mnemonic	Pin Description
DD[15-0]	IDE Data bus
IDEDA[2-0]	IDE Device address
IDECSn[0,1]	IDE Chip Select 0 and 1
DIORn	IDE Read Strobe
DIOWn	IDE Write Strobe
DMACKn	IDE DMA acknowledge

Ethernet Media Access Controller (MAC)

The MAC subsystem is compliant with the ISO/TEC 802.3 topology for a single shared medium with several stations. Multiple MII-compliant PHYs are supported. Features include:

- Supports 1/10/100 Mbps transfer rates for home / small-business / large-business applications
- Interfaces to an off-chip PHY through industry standard Media Independent Interface (MII)

Table D. Ethernet Media Access Controller Pin Assignments

Pin Mnemonic	Pin Description
MDC	Management Data Clock
MDIO	Management Data I/O
RXCLK	Receive Clock
MIIRXD[3:0]	Receive Data
RXDVAL	Receive Data Valid
RXERR	Receive Data Error
TXCLK	Transmit Clock
MIITXD[3:0]	Transmit Data
TXEN	Transmit Enable
TXERR	Transmit Error
CRS	Carrier Sense
CLD	Collision Detect

Serial Interfaces (SPI, I^{2}S, and AC '97)

The SPI port can be configured as a master or a slave, supporting the National Semiconductor®, Motorola®, and Texas Instruments® signaling protocols.

The AC'97 port supports multiple codecs for multichannel audio output with a single stereo input. Three I^{2}S ports can be configured to support six-channel, 24-bit audio.

These ports are multiplexed so that I^{2}S port 0 will take over either the AC'97 pins or the SPI pins. The second and third I2S ports' serial input and serial output pins are multiplexed with EGPIO[4,5,6,13]. The clocks supplied in the first I2S port are also used for the second and third I2S ports.

- Normal Mode: One SPI Port and one AC'97 Port
- I^{2}S on SSP Mode: One AC'97 Port and up to three I^{2}S Ports
- I^{2}S on AC'97 Mode: One SPI Port and up to three I^{2}S Ports

Table E. Audio Interfaces Pin Assignment

Pin Name	Normal Mode	I2S on SSP Mode	I2S on AC'97 Mode
	Pin Description	Pin Description	Pin Description
SCLK1	SPI Bit Clock	I2S Serial Clock	SPI Bit Clock
SFRM1	SPI Frame Clock	I2S Frame Clock	SPI Frame Clock
SSPRX1	SPI Serial Input	I2S Serial Input	SPI Serial Input
SSPTX1	SPI Serial Output	I2S Serial Output	SPI Serial Output
		(No I2S Master Clock)	
ARSTn	AC'97 Reset	AC'97 Reset	I2S Master Clock
ABITCLK	AC'97 Bit Clock	AC'97 Bit Clock	I2S Serial Clock
ASYNC	AC'97 Frame Clock	AC'97 Frame Clock	I2S Frame Clock
ASDI	AC'97 Serial Input	AC'97 Serial Input	I2S Serial Input
ASDO	AC'97 Serial Output	AC'97 Serial Output	I2S Serial Output

Raster/LCD Interface

The Raster/LCD interface provides data and interface signals for a variety of display types. It features fully programmable video interface timing for non-interlaced flat panel or dual scan displays. Resolutions up to 1024 x 768 are supported from a unified SDRAM based frame buffer. A 16-bit PWM provides control for LCD panel contrast.

LCD-specific features include:

- Timing and interface signals for digital LCD and TFT displays
- Full programmability for either non-interlaced or dual-scan color and grayscale flat panel displays
- Dedicated data path to SDRAM controller for improved system performance
- Pixel depths of 4, 8, 16, or 24 bits per pixel or 256 levels of grayscale
- Hardware Cursor up to 64 x 64 pixels
- 256 x 18 Color Lookup Table
- Hardware Blinking
- 8-bit interface to low-end panel

Table F. LCD Interface Pin Assignments

Pin Mnemonic	Pin Description
SPCLK	Pixel Clock
P[17:0]	Pixel Data Bus [17:0]
HSYNC / LP	Horizontal Synchronization / Line Pulse
VCSYNC / FP	Vertical or Composite Synchronization / Frame Pulse
BLANK	Composite Blank
BRIGHT	Pulse Width Modulated Brightness

Touch Screen Interface with 12-bit Analog-to-digital Converter (ADC)

The touch screen interface performs all sampling, averaging, ADC range checking, and control for a wide variety of analog resistive touch screens. This controller only interrupts the processor when a meaningful change occurs. The touch screen hardware may be disabled and the switch matrix and ADC controlled directly if desired. Features include:

- Support for 4-, 5-, 7-, or 8-wire analog resistive touch screens.
- Flexibility - unused lines may be used for temperature sensing or other functions.
- Touch screen interrupt function.

Table G. Touch Screen Interface with 12-bit Analog-to-Digital Converter Pin Assignments

Pin Mnemonic	Pin Description
Xp, Xm	Touch screen ADC X Axis

Table G. Touch Screen Interface with 12-bit Analog-to-Digital Converter Pin Assignments

Pin Mnemonic	Pin Description
Yp, Ym	Touch screen ADC Y Axis
SXp, SXm	Touch screen ADC X Axis Voltage Feedback
SYp, SYm	Touch screen ADC Y Axis Voltage Feedback

64-Key Keypad Interface

The keypad circuitry scans an 8 x 8 array of 64 normally open, single-pole switches. Any one or two keys depressed will be de-bounced and decoded. An interrupt is generated whenever a stable set of depressed keys is detected. If the keypad is not utilized, the 16 column/row pins may be used as general purpose I/O. The Keypad interface:

- Provides scanning, debounce, and decoding for a 64-key switch array.
- Scans an 8-row by 8-column matrix.
- May decode 2 keys at once.
- Generates an interrupt when a new stable key is determined.
- Also generates a 3-key reset interrupt.

Table H. 64-Key Keypad Interface Pin Assignments

Pin Mnemonic	Pin Description	Alternative Usage
COL[7:0]	Key Matrix Column Inputs	General Purpose I/O
ROW[7:0]	Key Matrix Row Inputs	General Purpose I/O

Universal Asynchronous Receiver/Transmitters (UARTs)

Three 16550-compatible UARTs are supplied. Two provide asynchronous HDLC (High-level Data Link Control) protocol support for full duplex transmit and receive. The HDLC receiver handles framing, address matching, CRC checking, control-octet transparency, and optionally passes the CRC to the host at the end of the packet. The HDLC transmitter handles framing, CRC generation, and control-octet transparency. The host must assemble the frame in memory before transmission. The HDLC receiver and transmitter use the UART FIFOs to buffer the data streams. A third IrDA® compatible UART is also supplied.

- UART1 supports modem bit rates up to 115.2 Kbps, supports HDLC and includes a 16 byte FIFO for

receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx, Tx and modem status change.

- UART2 contains an IrDA encoder operating at either the slow (up to 115 Kbps), medium (0.576 or 1.152 Mbps), or fast (4 Mbps) IR data rates. It also has a 16 byte FIFO for receive and a 16 byte FIFO for transmit.
- UART3 supports HDLC and includes a 16 byte FIFO for receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx and Tx.

Table I. Universal Asynchronous Receiver/Transmitters Pin Assignments

Pin Mnemonic	Pin Name - Description
TXD0	UART1 Transmit
RXD0	UART1 Receive
CTSn	UART1 Clear To Send / Transmit Enable
DSRn / DCDn	UART1 Data Set Ready / Data Carrier Detect
DTRn	UART1 Data Terminal Ready
RTSn	UART1 Ready To Send
EGPIO[0] / RI	UART1 Ring Indicator
TXD1 / SIROUT	UART2 Transmit / IrDA Output
RXD1 / SIRIN	UART2 Receive / IrDA Input
TXD2	UART3 Transmit
RXD2	UART3 Receive
EGPIO[3] / TENn	HDLC3 Transmit Enable

Triple-port USB Host

The USB Open Host Controller Interface (Open HCI) provides full-speed serial communications ports at a baud rate of 12 Mbits/sec. Up to 127 USB devices (printer, mouse, camera, keyboard, etc.) and USB hubs can be connected to the USB host in the USB “tiered star” topology.

This includes the following features:

- Compliance with the USB 2.0 specification
- Compliance with the Open HCI Rev 1.0 specification
- Supports both low speed (1.5 Mbps) and full speed (12 Mbps) USB device connections
- Root HUB integrated with 3 downstream USB ports
- Transceiver buffers integrated, over-current protection on ports
- Supports power management
- Operates as a master on the bus

The Open HCI host controller initializes the master DMA transfer with the AHB bus:

- Fetches endpoint descriptors and transfer descriptors
- Accesses endpoint data from system memory
- Accesses the HC communication area
- Writes status and retire transfer descriptor

Table J. Triple Port USB Host Pin Assignments

Pin Mnemonic	Pin Name - Description
USBp[2:0]	USB Positive signals
USBm[2:0]	USB Negative Signals

Two-wire Interface

The two-wire interface provides communication and control for synchronous-serial-driven devices.

Table K. Two-Wire Port with EEPROM Support Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
EECLK	Two-wire Interface Clock	General Purpose I/O
EEDATA	Two-wire Interface Data	General Purpose I/O

Real-time Clock with Software Trim

The software trim feature on the real time clock (RTC) provides software controlled digital compensation of the 32.768 KHz input clock. This compensation is accurate to ± 1.24 sec/month.

Note: A real time clock must be connected to RTCXTALI or the EP9312 device will not boot.

Table L. Real-Time Clock with Pin Assignments

Pin Mnemonic	Pin Name - Description
RTCXTALI	Real-Time Clock Oscillator Input
RTCXTALO	Real-Time Clock Oscillator Output

PLL and Clocking

The Processor and the Peripheral Clocks operate from a single 14.7456 MHz crystal.

The Real Time Clock operates from a 32.768 KHz external oscillator.

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Table R. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

12-channel DMA Controller

The DMA module contains 12 separate DMA channels. Ten of these may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

Internal Boot ROM

The Internal 16 Kbyte ROM allows booting from FLASH memory, SPI or UART. Consult the EP93xx User's Guide for operational details.

Static Memory Single Word Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	0	-	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpw}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to RDn deassert time	t_{DAs}	$t_{HCLK} + 12$	-	-	ns
DA hold from RDn deassert time	t_{DAh}	0	-	-	ns

See “Timing Conditions” on page 14 for definition of HCLK.

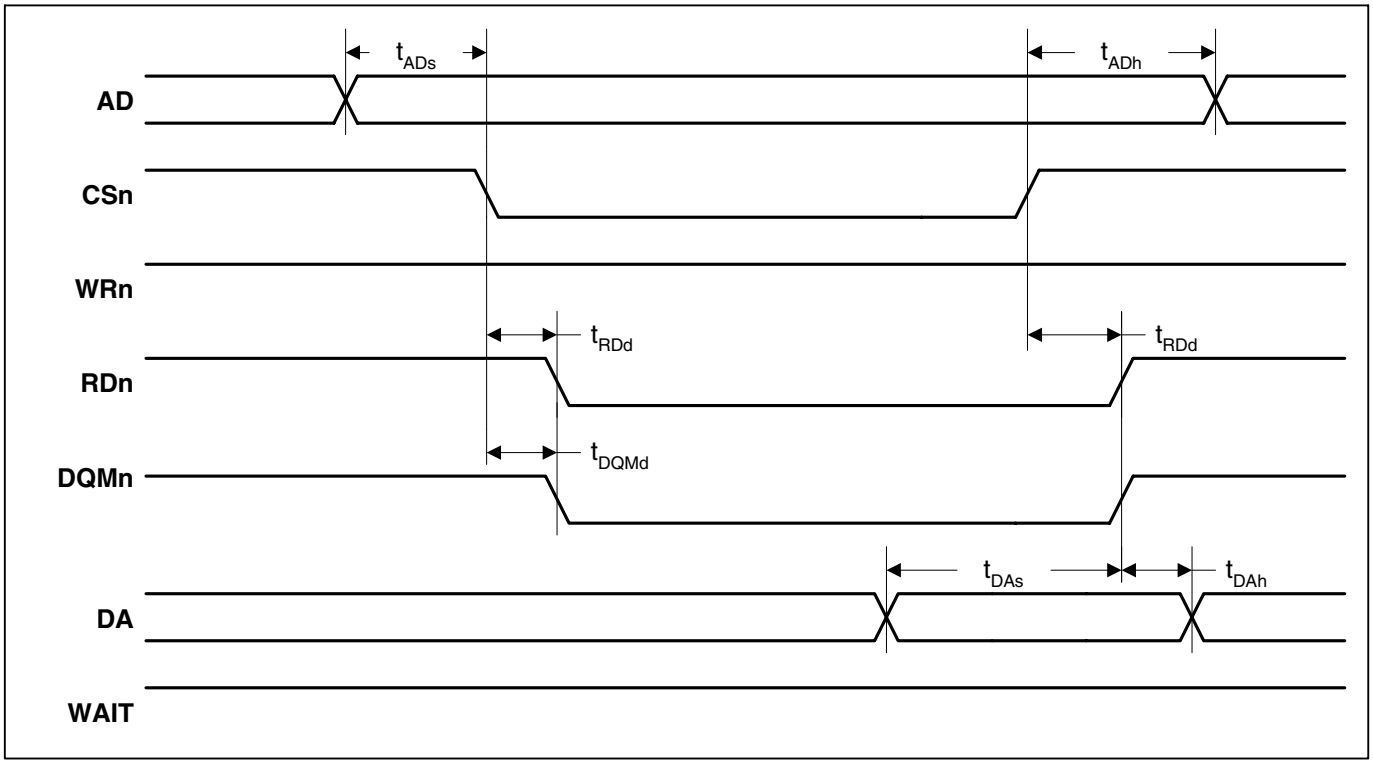


Figure 6. Static Memory Single Word Read Cycle Timing Measurement

Static Memory 32-bit Read on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to Address transition time	t_{AD1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{AD2}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{AD3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times (4 \times WST1 + 5)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

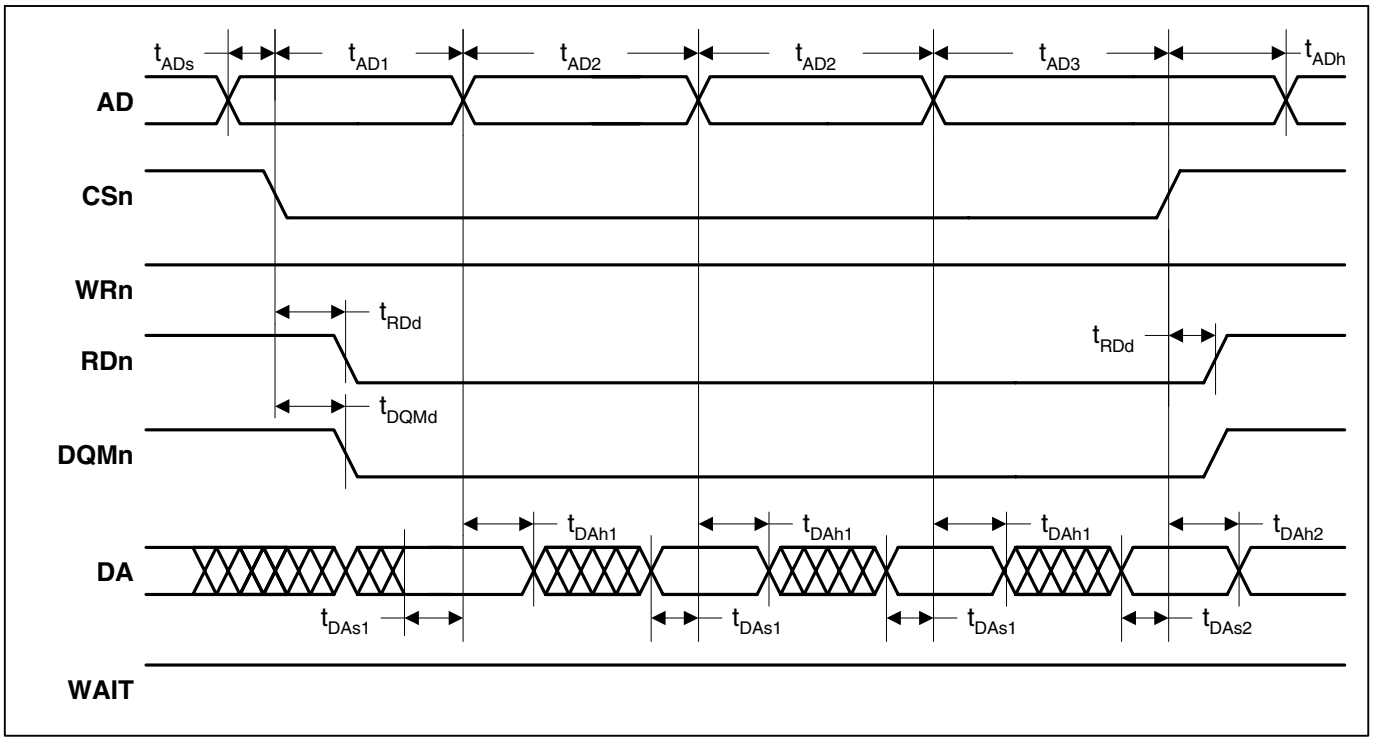


Figure 8. Static Memory Multiple Word Read 8-bit Cycle Timing Measurement

Static Memory 32-bit Read on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to AD transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd2}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times ((2 \times WST1) + 3)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

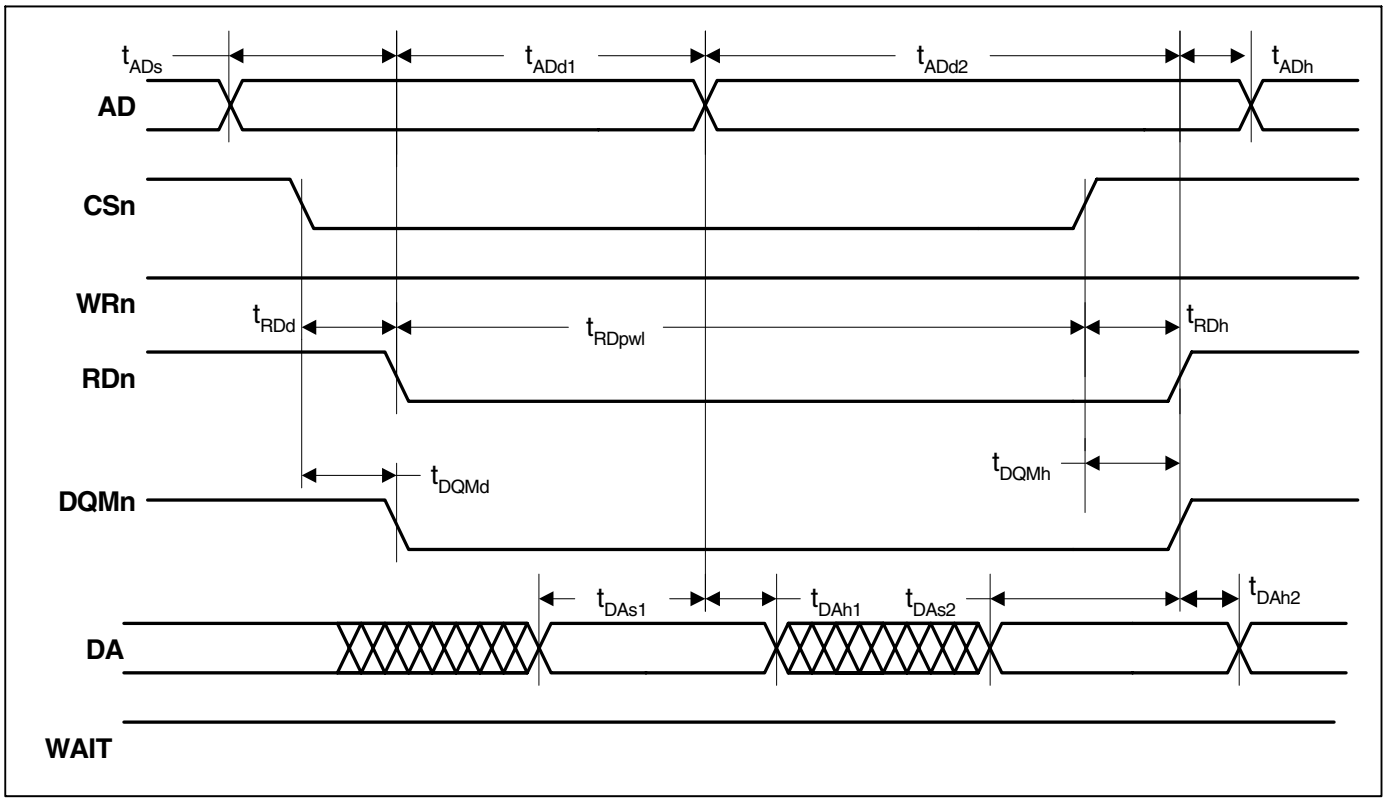


Figure 10. Static Memory Multiple Word Read 16-bit Cycle Timing Measurement

Static Memory Burst Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$			ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$			ns
WRN/DQMn deassert to AD transition time	t_{ADd}			$t_{HCLK} + 6$	ns
CSn hold from WRn deassert time	t_{CSh}	7			ns
CSn to WRn assert delay time	t_{WRd}			2	ns
CSn to DQMn assert delay time	t_{DQMd}			1	ns
DQMn assert time	t_{DQpwL}		$t_{HCLK} \times (WST1 + 1)$		ns
DQMn deassert time	t_{DQpwH}			$(t_{HCLK} \times 2) + 14$	ns
WRn assert time	t_{WRpwL}		$t_{HCLK} \times (WST1 + 11)$		ns
WRn deassert time	t_{WRpwH}			$(t_{HCLK} \times 2) + 7$	ns
WRn/DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}			ns
WRn/DQMn assert to DA valid time	t_{DAv}			8	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

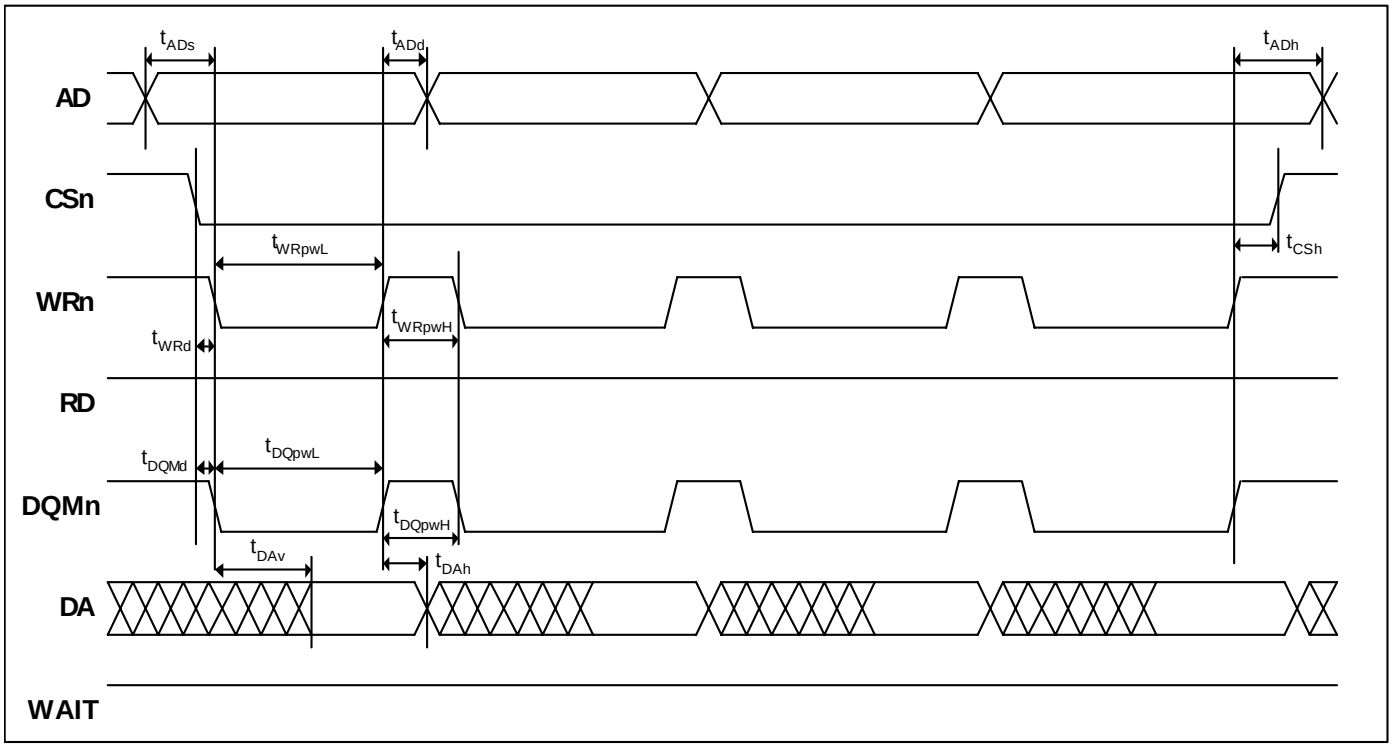
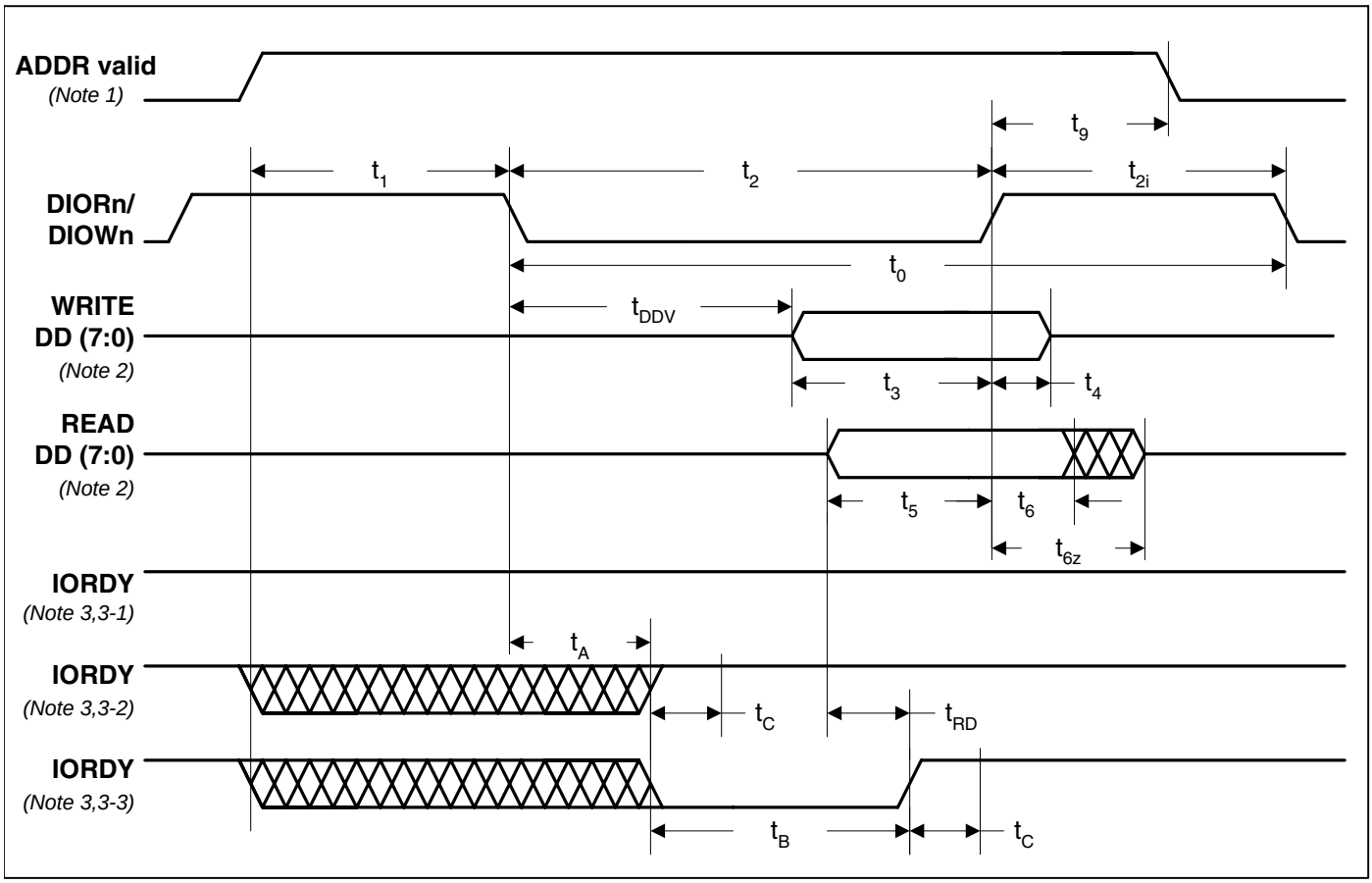


Figure 13. Static Memory Burst Write Cycle Timing Measurement



Note: 1. Device address consists of signals IDECS0n, IDECS1n and IDEDA (2:0)

2. Data consists of DD (7:0)

3. The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIORn or DIOWn. The assertion and negation or IORDY are described in the following three cases:

3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.

3-2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than t_C before release: no wait generated.

3-3 Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than t_C before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIORn is asserted, the device shall place read data on DD (7:0) for t_{RD} before asserting IORDY.

Figure 17. Register Transfer to/from Device

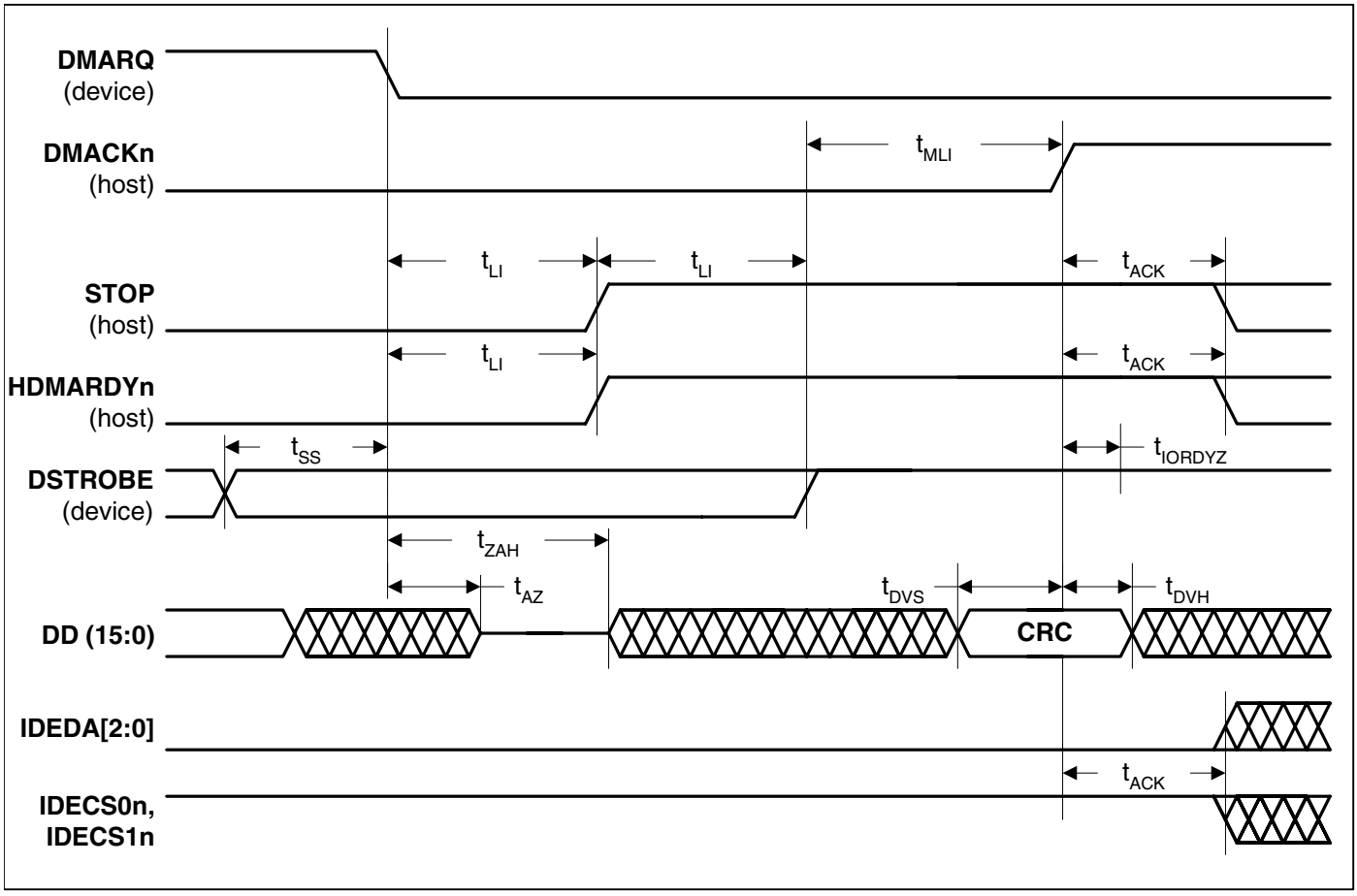
Ultra DMA Data Transfer

Figure 19 through Figure 28 define the timings associated with all phases of Ultra DMA bursts. The following table contains the values for the timings for each of the Ultra DMA modes.

Timing reference levels = 1.5 V

Parameter	Symbol	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)	
		min	max	min	max	min	max	min	max
Cycle time allowing for asymmetry and clock variations (from DSTROBE edge to DSTROBE edge)	t_{CYCRD}	112	-	73	-	54	-	39	-
Two-cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of DSTROBE)	t_{2CYCRD}	230	-	154	-	115	-	86	-
Cycle time allowing for asymmetry and clock variations (from HSTROBE edge to HSTROBE edge)	t_{CYCWR}	230	-	170	-	130	-	100	-
Two-cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of HSTROBE)	t_{2CYCWR}	460	-	340	-	260	-	200	-
Data setup time at recipient (Read)	t_{DS}	15	-	10	-	7	-	7	-
Data hold time at recipient (Read)	t_{DH}	8	-	8	-	8	-	8	-
Data valid setup time at sender (Write) (Note 2) (from data valid until STROBE edge)	t_{DVS}	70	-	48	-	30	-	20	-
Data valid hold time at sender (Write) (Note 2) (from STROBE edge until data may become invalid)	t_{DVH}	6	-	6	-	6	-	6	-
First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	t_{FS}	0	230	0	200	0	170	0	130
Limited interlock time (Note 3)	t_{LI}	0	150	0	150	0	150	0	100
Interlock time with minimum (Note 3)	t_{MLI}	20	-	20	-	20	-	20	-
Unlimited interlock time (Note 3)	t_{UI}	0	-	0	-	0	-	0	-
Maximum time allowed for output drivers to release (from asserted or negated)	t_{AZ}	-	10	-	10	-	10	-	10
Minimum delay time required for output	t_{ZAH}	20	-	20	-	20	-	20	-
Drivers to assert or negate (from released)	t_{ZAD}	0	-	0	-	0	-	0	-
Envelope time (from DMACKn to STOP and HDMARDYn during data in burst initiation and from DMACKn to STOP during data out burst initiation)	t_{ENV}	20	70	20	70	20	70	20	55
Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDYn)	t_{RFS}	-	75	-	70	-	60	-	60
Ready-to-pause time (that recipient shall wait to pause after negating DMARDYn)	t_{RP}	160	-	125	-	100	-	100	-
Maximum time before releasing IORDY	t_{IORDYZ}	-	20	-	20	-	20	-	20
Minimum time before driving STROBE (Note 4)	t_{ZIORDY}	0	-	0	-	0	-	0	-
Setup and hold times for DMACKn (before assertion or negation)	t_{ACK}	20	-	20	-	20	-	20	-
Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	t_{SS}	50	-	50	-	50	-	50	-

Note: 1. Timing parameters shall be measured at the connector of the sender or receiver to which the parameter applies.
2. The test load for t_{DVS} and t_{DVH} shall be a lumped capacitor load with no cable or receivers. Timing for t_{DVS} and t_{DVH} shall be met for all capacitive loads from 15 to 40 pf where all signals have the same capacitive load value.
3. t_{UI}, t_{MLI} and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., either sender or recipient is waiting for the other to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
4. t_{ZIORDY} may be greater than t_{ENV} since the device has a pull up on IORDYn giving it a known state when released.
5. All IDE timing is based upon HCLK = 100 MHz.



Note: The definitions for the DIOWn:STOP, DIORn:HDMARDYn:HSTROBE and IORDY:DDMARDYn:DSTROBE signal lines are no longer in effect after DMARQ and DMACKn are negated.

Figure 22. Device Terminating an Ultra DMA data-in Burst

Audio Interface

The following table contains the values for the timings of each of the SPI modes.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{clk_per}	-	tspix_clk	-	ns
SCLK high time	t_{clk_high}	-	(tspix_clk) / 2	-	ns
SCLK low time	t_{clk_low}	-	(tspix_clk) / 2	-	ns
SCLK rise/fall time	t_{clkrf}	1	-	8	ns
Data from master valid delay time	t_{DMd}	-	-	3	ns
Data from master setup time	t_{DMs}	20	-	-	ns
Data from master hold time	t_{DMh}	40	-	-	ns
Data from slave setup time	t_{DSs}	20	-	-	ns
Data from slave hold time	t_{DSh}	40	-	-	ns

Note: The tspix_clk is programmable by the user.

AC'97

Parameter	Symbol	Min	Typ	Max	Unit
ABITCLK input cycle time	t_{clk_per}	-	81.4	-	ns
ABITCLK input high time	t_{clk_high}	36	-	45	ns
ABITCLK input low time	t_{clk_low}	36	-	45	ns
ABITCLK input rise/fall time	t_{clkrf}	2	-	6	ns
ASDI setup to ABITCLK falling	t_s	10	-	-	ns
ASDI hold after ABITCLK falling	t_h	10	-	-	ns
ASDI input rise/fall time	t_{rfin}	2	-	6	ns
ABITCLK rising to ASDO / ASYNC valid, C_L = 55 pF	t_{co}	2	-	15	ns
ASYNC / ASDO rise/fall time, C_L = 55 pF	t_{rfout}	2	-	6	ns

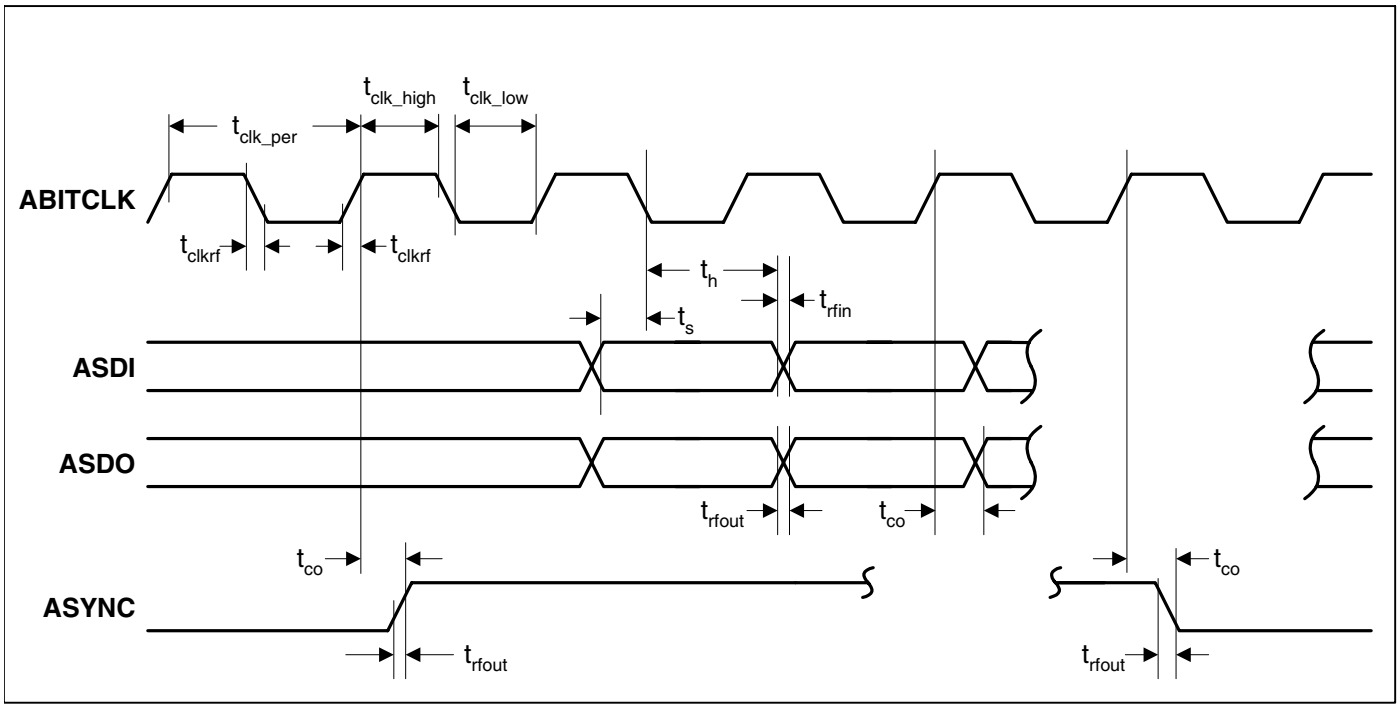


Figure 34. AC '97 Configuration Timing Measurement

LCD Interface

Parameter	Symbol	Min	Typ	Max	Unit
SPCLK rise/fall time	t_{clkr}	2	-	8	ns
SPCLK rising edge to control signal transition time	t_{CD}	-	-	3	ns
SPCLK rising edge to data transition time	t_{DD}	-	-	10	ns
Data valid time	t_{Dv}	t_{SPCLK}	-	-	ns

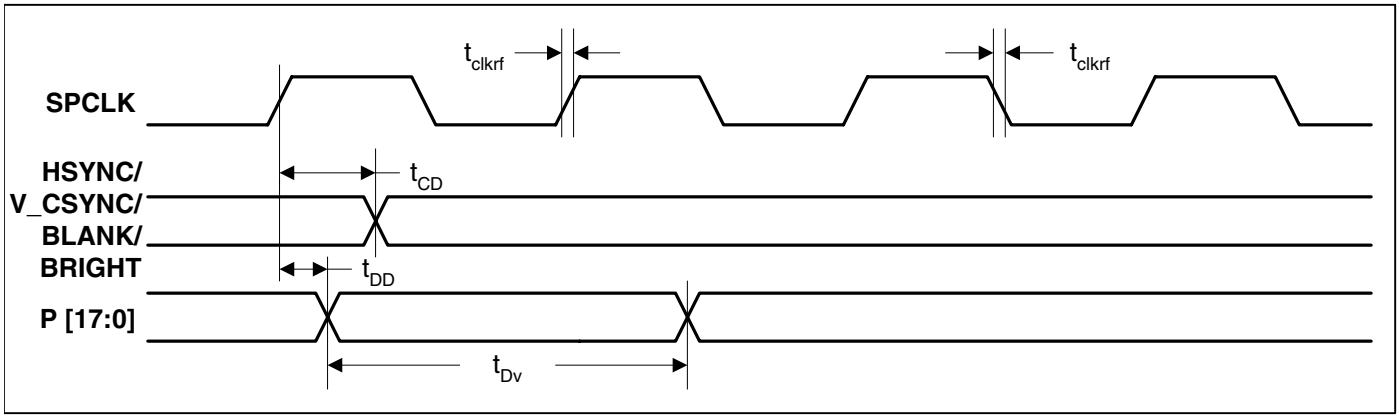
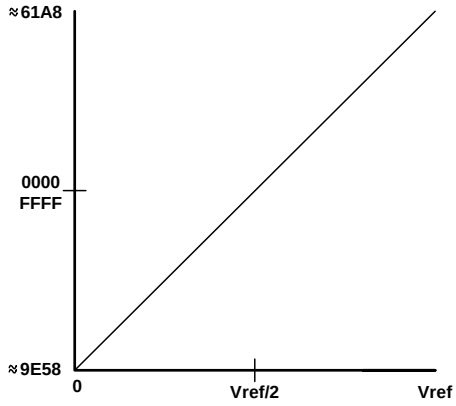


Figure 35. LCD Timing Measurement

ADC

Parameter	Comment	Value	Units
Resolution	No missing codes Range of 0 to 3.3 V	50K counts (approximate)	
Integral non-linearity		0.01%	
Offset error		±15	mV
Full scale error		0.2%	
Maximum sample rate	ADIV = 0 ADIV = 1	3750 925	Samples per second Samples per second
Channel switch settling time	ADIV = 0 ADIV = 1	500 2	µs ms
Noise (RMS) - typical		120	µV

Note: ADIV refers to bit 16 in the KeyTchClkDiv register.
ADIV = 0 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 4.
ADIV = 1 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 16.



A/D Converter Transfer Function
(approximately ±25,000 counts)

Figure 36. ADC Transfer Function

Using the ADC:

This ADC has a state-machine based conversion engine that automates the conversion process. The initiator for a conversion is the read access of the TSXYResult register by the CPU. The data returned from reading this register contains the result as well as the status bit indicating the state of the ADC. However, this peripheral requires a delay between each successful conversion and the issue of the next conversion command, or else the returned value of successive samples may not reflect the analog input. Since the state of the ADC state machine is returned through the same channel used to initiate the conversion process, there must be a delay inserted after every complete conversion. Note that reading TSXYResult during a conversion will not affect the result of the ongoing process.

The following is a recommended procedure for safely polling the ADC from software:

1. Read the TSXYResult register into a local variable to initiate a conversion.
2. If the value of bit 31 of the local variable is '0' then repeat step 1.
3. Delay long enough to meet the maximum sample rate as shown above.
4. Mask the local variable with 0xFFFF to remove extraneous data.
5. If signed mode is used, do a sign extend of the lower halfword.
6. Return the sampled value.

JTAG

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	100	-	ns
TCK clock high time	t_{clk_high}	50	-	ns
TCK clock low time	t_{clk_low}	50	-	ns
TMS / TDI to clock rising setup time	t_{JPs}	20	-	ns
Clock rising to TMS / TDI hold time	t_{JPh}	45	-	ns
JTAG port clock to output	t_{JPco}	-	30	ns
JTAG port high impedance to valid output	t_{JPzx}	-	30	ns
JTAG port valid output to high impedance	t_{JPxz}	-	30	ns

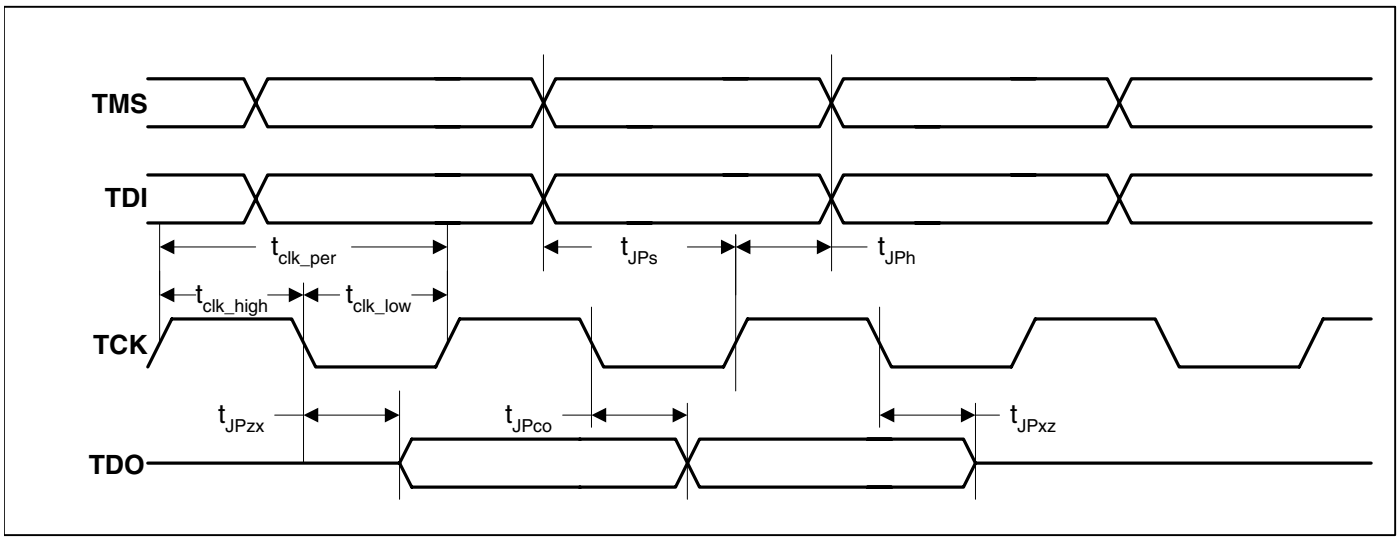


Figure 37. JTAG Timing Measurement

352 Pin BGA Package Outline

352-Ball PBGA Diagram

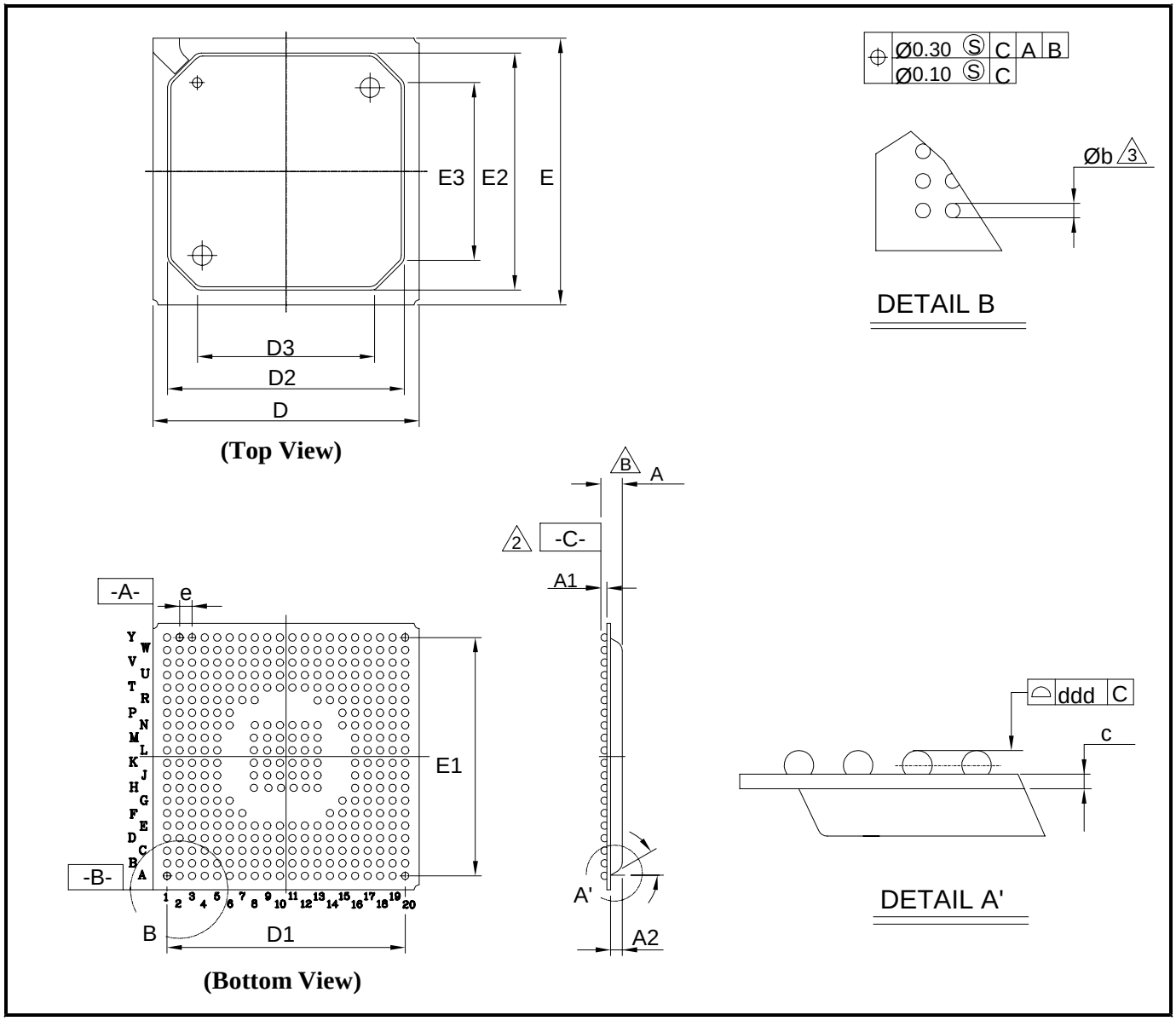


Figure 38. 352 Pin PBGA Pin Diagram

Figure 40. 352 PIN BGA PINOUT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
Y	HSYNC	DD[1]	DD[12]	P[2]	AD[15]	DA[6]	DA[4]	AD[10]	DA[1]	AD[8]	IDEDA[0]	DTRN	TDO	BOOT[0]	EEDAT	ASDO	SFRM1	RDLED	USBP[1]	ABITCLK	**Y**
W	P[12]	P[9]	DD[0]	P[5]	P[3]	DA[7]	DA[5]	AD[11]	AD[9]	IDECS1N	IDEDA[1]	TCK	TMS	EECLK	SCLK1	GRLED	INT[3]	SLA[1]	SLA[0]	RXD[2]	**W**
V	P[16]	P[11]	P[8]	DD[15]	DD[13]	P[1]	AD[14]	AD[12]	DA[2]	IDECS0N	IDEDA[2]	TDI	GND	ASYNC	SSPTX1	INT[2]	RTSN	USBP[0]	CTSN	TXD[0]	**V**
U	AD[0]	P[15]	P[10]	P[7]	P[6]	P[4]	P[0]	AD[13]	DA[3]	DA[0]	DSRN	BOOT[1]	NC	SSPRX1	INT[1]	PWMOUT	USBM[0]	RXD[1]	TXD[1]	ROW[1]	**U**
T	DA[8]	BLANK	P[13]	SPCLK	V_CSYNC	DD[14]	GND	CVDD	RVDD	GND	GND	RVDD	CVDD	GND	INT[0]	USBM[1]	RXD[0]	TXD[2]	ROW[2]	ROW[4]	**T**
R	AD[2]	AD[1]	P[17]	P[14]	RVDD	RVDD	GND	CVDD					CVDD	GND	RVDD	RVDD	ROW[0]	ROW[3]	PLL_GND	ROW[5]	**R**
P	AD[4]	DA[10]	DA[9]	BRIGHT	RVDD	RVDD									RVDD	RVDD	XTALI	PLL_VDD	ROW[6]	ROW[7]	**P**
N	DA[13]	DA[12]	DA[11]	AD[3]	CVDD	CVDD		GND	GND	GND	GND	GND	GND		GND	GND	XTALO	COL[0]	COL[1]	COL[2]	**N**
M	AD[7]	DA[14]	AD[6]	AD[5]	CVDD			GND	GND	GND	GND	GND	GND			GND	COL[4]	COL[3]	COL[6]	CSN[0]	**M**
L	DA[18]	DA[17]	DA[16]	DA[15]	GND			GND	GND	GND	GND	GND	GND			CVDD	COL[5]	COL[7]	RSTON	PRSTN	**L**
K	AD[22]	DA[20]	AD[21]	DA[19]	RVDD			GND	GND	GND	GND	GND	GND			CVDD	SYM	SYP	SXM	SXP	**K**
J	DA[21]	DQMN[0]	DQMN[1]	DQMN[2]	GND			GND	GND	GND	GND	GND	GND			CVDD	RTCXTALI	XM	YP	YM	**J**
H	DQMN[3]	CASN	RASN	SDCSN[2]	CVDD			GND	GND	GND	GND	GND	GND			RVDD	RTCXTALO	ADC_VDD	ADC_GND	XP	**H**
G	SDCSN[0]	SDCSN[1]	SDWEN	SDCLK	RVDD	RVDD									RVDD	RVDD	EGPIO[7]	EGPIO[9]	EGPIO[10]	EGPIO[11]	**G**
F	SDCSN[3]	DA[22]	DA[24]	AD[25]	RVDD	GND	CVDD							CVDD	GND	GND	EGPIO[2]	EGPIO[4]	EGPIO[6]	EGPIO[8]	**F**
E	AD[23]	DA[23]	DA[26]	CSN[6]	GND	GND	CVDD	CVDD	RVDD	GND	GND	RVDD	CVDD	CVDD	GND	ASDI	DIOWN	EGPIO[0]	EGPIO[3]	EGPIO[5]	**E**
D	AD[24]	DA[25]	DD[11]	SDCLKEN	AD[19]	DD[9]	DD[5]	AD[16]	MIIRXD[2]	MIITXD[3]	TXEN	NC	NC	NC	EGPIO[14]	NC	USBM[2]	ARSTN	DIORN	EGPIO[1]	**D**
C	CSN[1]	CSN[3]	AD[20]	DA[29]	DD[10]	DD[6]	DD[2]	MDC	MIIRXD[3]	TXCLK	MIITXD[0]	NC	NC	NC	NC	NC	NC	USBP[2]	IORDY	DMACKN	**C**
B	CSN[2]	DA[31]	DA[30]	DA[27]	DD[7]	DD[3]	WRN	MDIO	MIIRXD[1]	RXERR	MIITXD[1]	CRS	NC	NC	NC	NC	EGPIO[13]	NC	WAITN	TRSTN	**B**
A	CSN[7]	DA[28]	AD[18]	DD[8]	DD[4]	AD[17]	RDN	RXCLK	MIIRXD[0]	RXDVAL	MIITXD[2]	TXERR	CLD	NC	NC	NC	EGPIO[12]	EGPIO[15]	NC	NC	**A**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	

Pin List

The following Plastic Ball Grid Array (PBGA) ball assignment table is sorted in order of ball.

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A1	CSN[7]	E9	RVDD	L3	DA[16]	T13	CVDD
A2	DA[28]	E10	GND	L4	DA[15]	T14	GND
A3	AD[18]	E11	GND	L5	GND	T15	INT[0]
A4	DD[8]	E12	RVDD	L8	GND	T16	USBM[1]
A5	DD[4]	E13	CVDD	L9	GND	T17	RXD[0]
A6	AD[17]	E14	CVDD	L10	GND	T18	TXD[2]
A7	RDN	E15	GND	L11	GND	T19	ROW[2]
A8	RXCLK	E16	ASDI	L12	GND	T20	ROW[4]
A9	MIIRXD[0]	E17	DIOWN	L13	GND	U1	AD[0]
A10	RXDVAL	E18	EGPIO[0]	L16	CVDD	U2	P[15]
A11	MIITXD[2]	E19	EGPIO[3]	L17	COL[5]	U3	P[10]
A12	TXERR	E20	EGPIO[5]	L18	COL[7]	U4	P[7]
A13	CLD	F1	SDCSN[3]	L19	RSTON	U5	P[6]
A14	NC	F2	DA[22]	L20	PRSTN	U6	P[4]
A15	NC	F3	DA[24]	M1	AD[7]	U7	P[0]
A16	NC	F4	AD[25]	M2	DA[14]	U8	AD[13]
A17	EGPIO[12]	F5	RVDD	M3	AD[6]	U9	DA[3]
A18	EGPIO[15]	F6	GND	M4	AD[5]	U10	DA[0]
A19	NC	F7	CVDD	M5	CVDD	U11	DSRN
A20	NC	F14	CVDD	M8	GND	U12	BOOT[1]
B1	CSN[2]	F15	GND	M9	GND	U13	NC
B2	DA[31]	F16	GND	M10	GND	U14	SSPRX1
B3	DA[30]	F17	EGPIO[2]	M11	GND	U15	INT[1]
B4	DA[27]	F18	EGPIO[4]	M12	GND	U16	PWMOUT
B5	DD[7]	F19	EGPIO[6]	M13	GND	U17	USBM[0]
B6	DD[3]	F20	EGPIO[8]	M16	GND	U18	RXD[1]
B7	WRN	G1	SDCSN[0]	M17	COL[4]	U19	TXD[1]
B8	MDIO	G2	SDCSN[1]	M18	COL[3]	U20	ROW[1]
B9	MIIRXD[1]	G3	SDWEN	M19	COL[6]	V1	P[16]
B10	RXERR	G4	SDCLK	M20	CSN[0]	V2	P[11]
B11	MIITXD[1]	G5	RVDD	N1	DA[13]	V3	P[8]
B12	CRS	G6	RVDD	N2	DA[12]	V4	DD[15]
B13	NC	G15	RVDD	N3	DA[11]	V5	DD[13]
B14	NC	G16	RVDD	N4	AD[3]	V6	P[1]
B15	NC	G17	EGPIO[7]	N5	CVDD	V7	AD[14]
B16	NC	G18	EGPIO[9]	N6	CVDD	V8	AD[12]
B17	EGPIO[13]	G19	EGPIO[10]	N8	GND	V9	DA[2]
B18	NC	G20	EGPIO[11]	N9	GND	V10	IDECS0N
B19	WAITN	H1	DQMN[3]	N10	GND	V11	IDEDA[2]
B20	TRSTN	H2	CASN	N11	GND	V12	TDI
C1	CSN[1]	H3	RASN	N12	GND	V13	GND
C2	CSN[3]	H4	SDCSN[2]	N13	GND	V14	ASYNC

The following section focuses on the EP9312 pin signals from two viewpoints - the pin usage and pad characteristics, and the pin multiplexing usage. The first table (Table S) is a summary of all the EP9312 pin signals. The second table (Table T) illustrates the pin signal multiplexing and configuration options.

Table S is a summary of the EP9312 pin signals, which illustrates the pad type and pad pull type (if any). The symbols used in the table are defined as follows. (Note: A blank box means Not Applicable (NA) or, for Pull Type, No Pull (NP).)

Under the Pad Type column:

- A - Analog pad
- P - Power pad
- G - Ground pad
- I - Pin is an input only
- I/O - Pin is input/output
- 4mA - Pin is a 4 mA output driver
- 8mA - Pin is an 8 mA output driver
- 12mA - Pin is an 12 mA output driver

See the text description for additional information about bi-directional pins.

Under the Pull Type Column:

- PU - Resistor is a pull up to the RVDD supply
- PD - Resistor is a pull down to the RGND supply