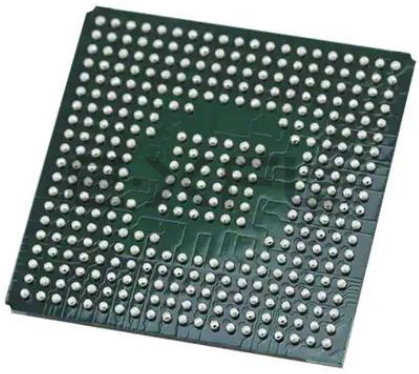


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Math Engine; MaverickCrunch™
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	352-BBGA
Supplier Device Package	352-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9312-ib

List of Tables

receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx, Tx and modem status change.

- UART2 contains an IrDA encoder operating at either the slow (up to 115 Kbps), medium (0.576 or 1.152 Mbps), or fast (4 Mbps) IR data rates. It also has a 16 byte FIFO for receive and a 16 byte FIFO for transmit.
- UART3 supports HDLC and includes a 16 byte FIFO for receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx and Tx.

Table I. Universal Asynchronous Receiver/Transmitters Pin Assignments

Pin Mnemonic	Pin Name - Description
TXD0	UART1 Transmit
RXD0	UART1 Receive
CTSn	UART1 Clear To Send / Transmit Enable
DSRn / DCDn	UART1 Data Set Ready / Data Carrier Detect
DTRn	UART1 Data Terminal Ready
RTSn	UART1 Ready To Send
EGPIO[0] / RI	UART1 Ring Indicator
TXD1 / SIROUT	UART2 Transmit / IrDA Output
RXD1 / SIRIN	UART2 Receive / IrDA Input
TXD2	UART3 Transmit
RXD2	UART3 Receive
EGPIO[3] / TENn	HDLC3 Transmit Enable

Triple-port USB Host

The USB Open Host Controller Interface (Open HCI) provides full-speed serial communications ports at a baud rate of 12 Mbits/sec. Up to 127 USB devices (printer, mouse, camera, keyboard, etc.) and USB hubs can be connected to the USB host in the USB “tiered star” topology.

This includes the following features:

- Compliance with the USB 2.0 specification
- Compliance with the Open HCI Rev 1.0 specification
- Supports both low speed (1.5 Mbps) and full speed (12 Mbps) USB device connections
- Root HUB integrated with 3 downstream USB ports
- Transceiver buffers integrated, over-current protection on ports
- Supports power management
- Operates as a master on the bus

The Open HCI host controller initializes the master DMA transfer with the AHB bus:

- Fetches endpoint descriptors and transfer descriptors
- Accesses endpoint data from system memory
- Accesses the HC communication area
- Writes status and retire transfer descriptor

Table J. Triple Port USB Host Pin Assignments

Pin Mnemonic	Pin Name - Description
USBp[2:0]	USB Positive signals
USBm[2:0]	USB Negative Signals

Two-wire Interface

The two-wire interface provides communication and control for synchronous-serial-driven devices.

Table K. Two-Wire Port with EEPROM Support Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
EECLK	Two-wire Interface Clock	General Purpose I/O
EEDATA	Two-wire Interface Data	General Purpose I/O

Real-time Clock with Software Trim

The software trim feature on the real time clock (RTC) provides software controlled digital compensation of the 32.768 KHz input clock. This compensation is accurate to ± 1.24 sec/month.

Note: A real time clock must be connected to RTCXTALI or the EP9312 device will not boot.

Table L. Real-Time Clock with Pin Assignments

Pin Mnemonic	Pin Name - Description
RTCXTALI	Real-Time Clock Oscillator Input
RTCXTALO	Real-Time Clock Oscillator Output

PLL and Clocking

The Processor and the Peripheral Clocks operate from a single 14.7456 MHz crystal.

The Real Time Clock operates from a 32.768 KHz external oscillator.

Memory Interface

Figure 2 through Figure 5 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK high time	t_{clk_high}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK low time	t_{clk_low}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK rise/fall time	t_{clkrf}	-	2	4	ns
Signal delay from SDCLK rising edge time	t_d	-	-	8	ns
Signal hold from SDCLK rising edge time	t_h	1	-	-	ns
DQMn delay from SDCLK rising edge time	t_{DQd}	-	-	8	ns
DQMn hold from SDCLK rising edge time	t_{DQh}	1	-	-	ns
DA valid setup to SDCLK rising edge time	t_{DAs}	2	-	-	ns
DA valid hold from SDCLK rising edge time	t_{DAh}	3	-	-	ns

SDRAM Load Mode Register Cycle

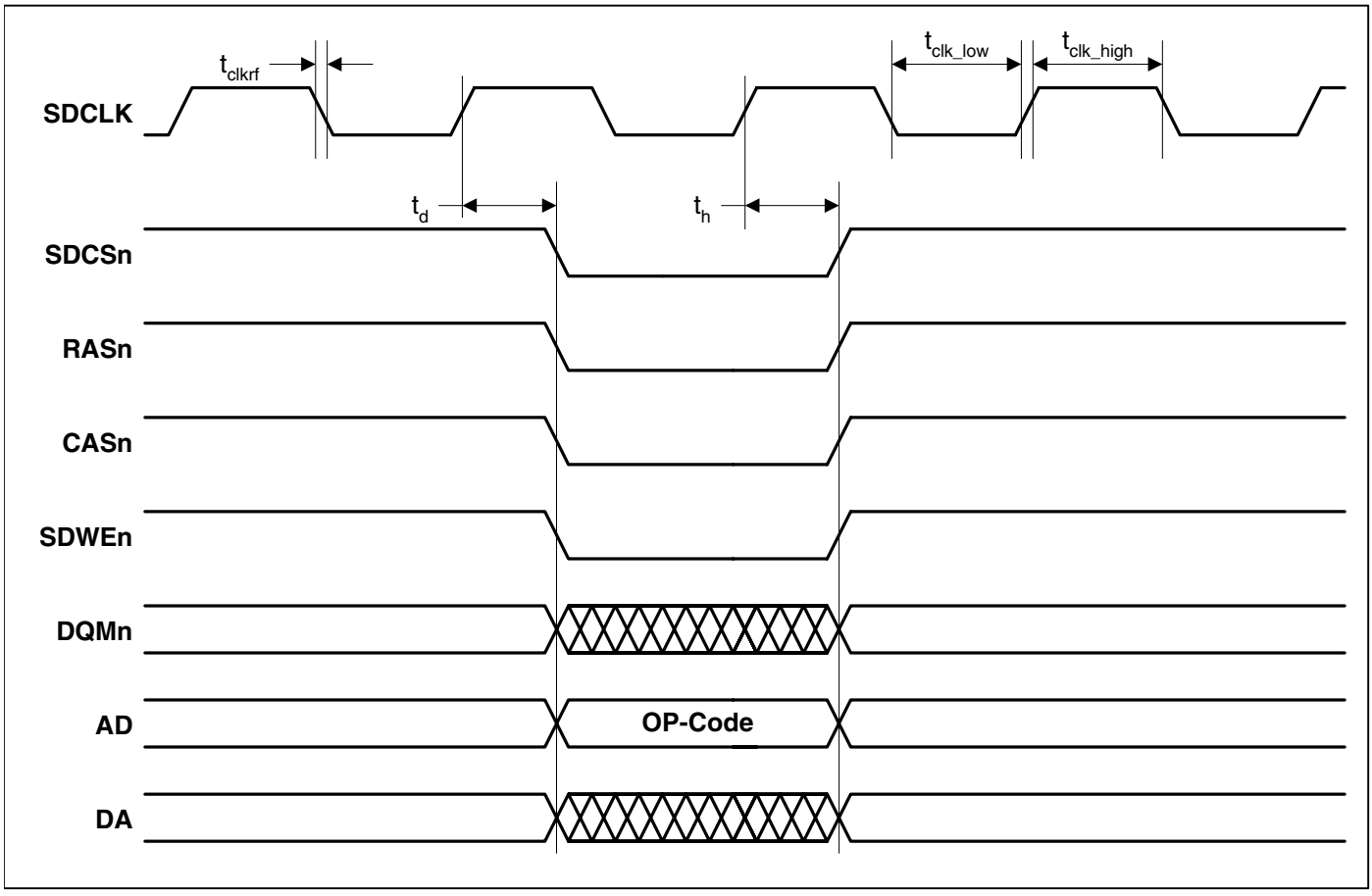


Figure 2. SDRAM Load Mode Register Cycle Timing Measurement

SDRAM Burst Read Cycle

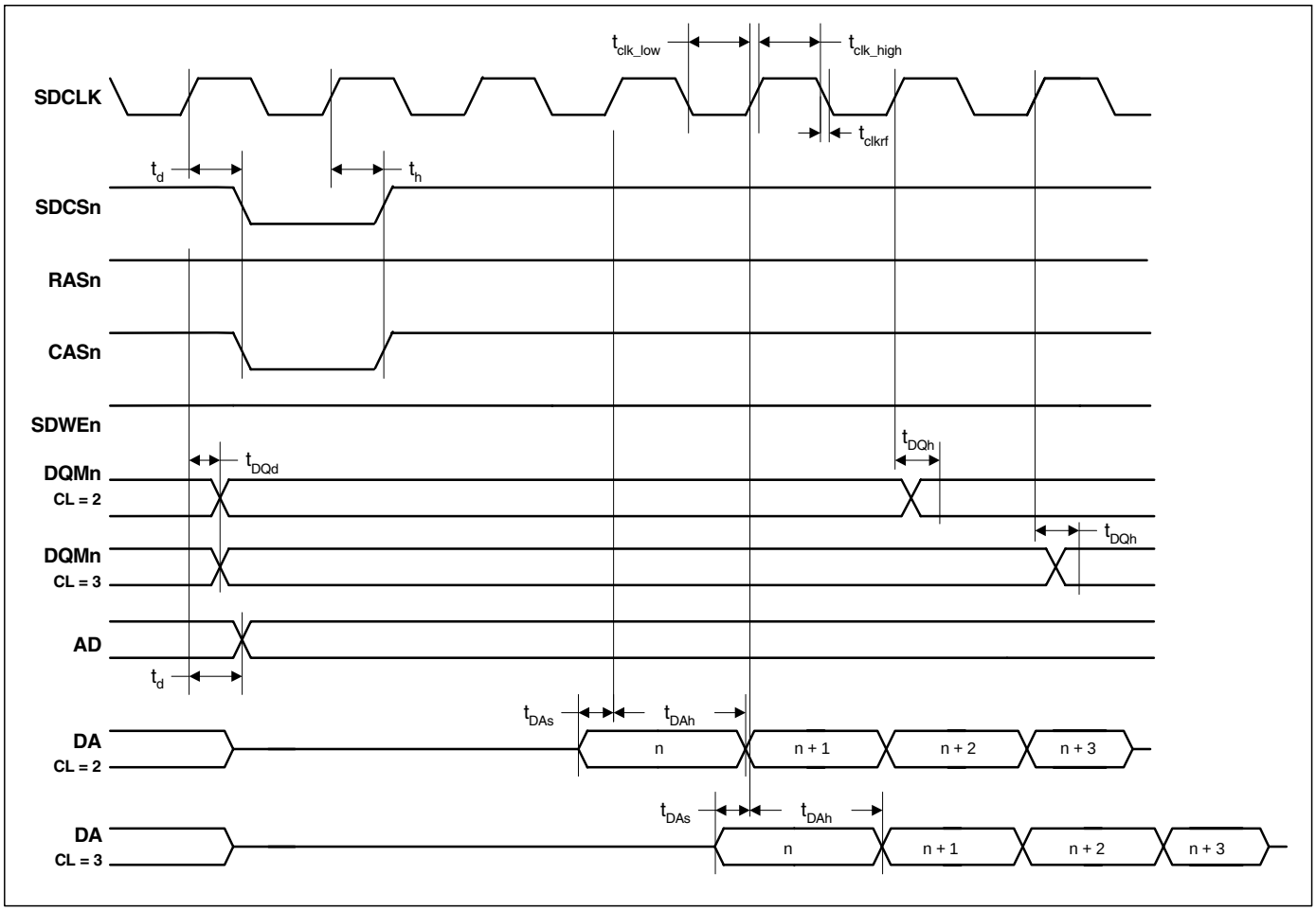


Figure 3. SDRAM Burst Read Cycle Timing Measurement

SDRAM Burst Write Cycle

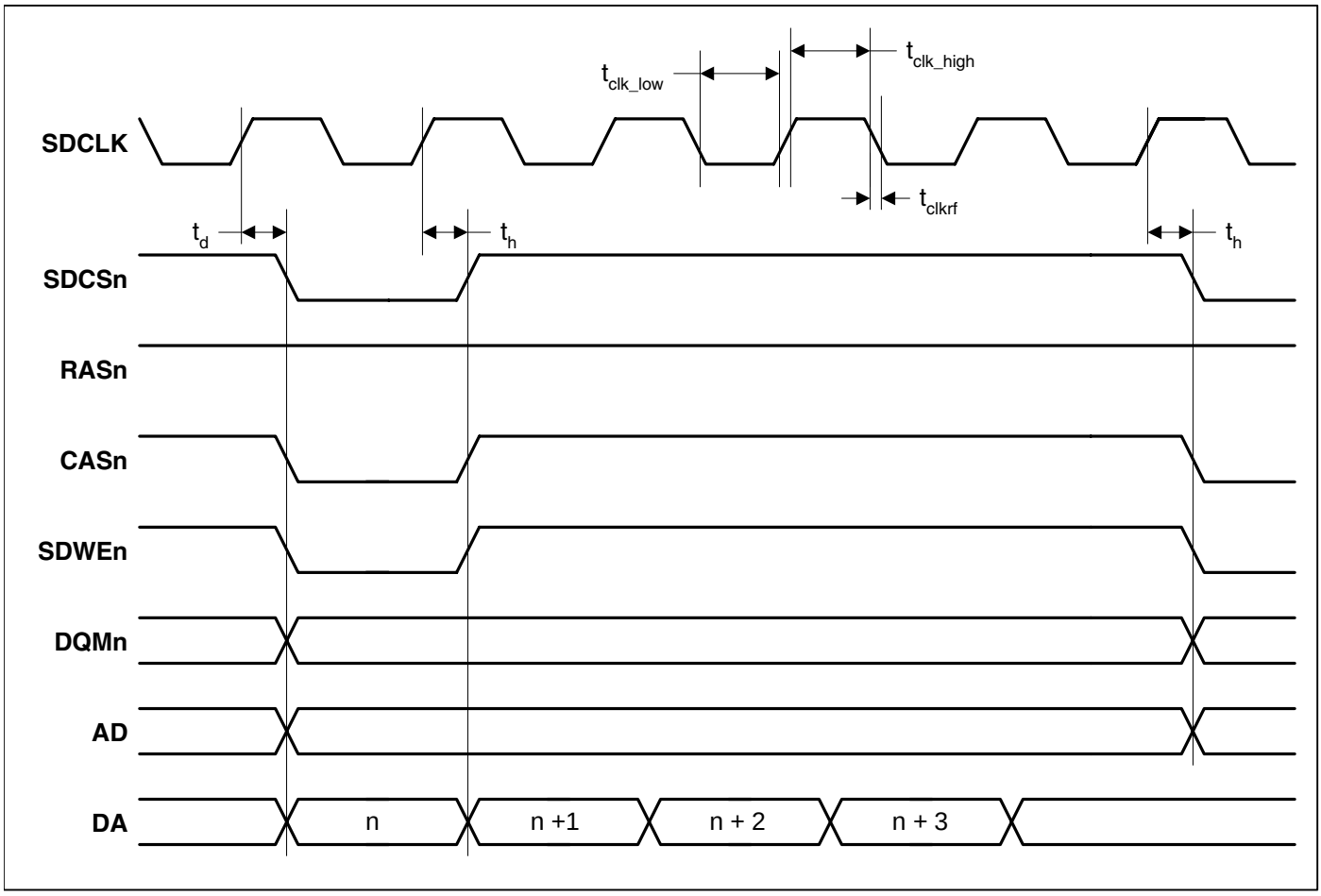
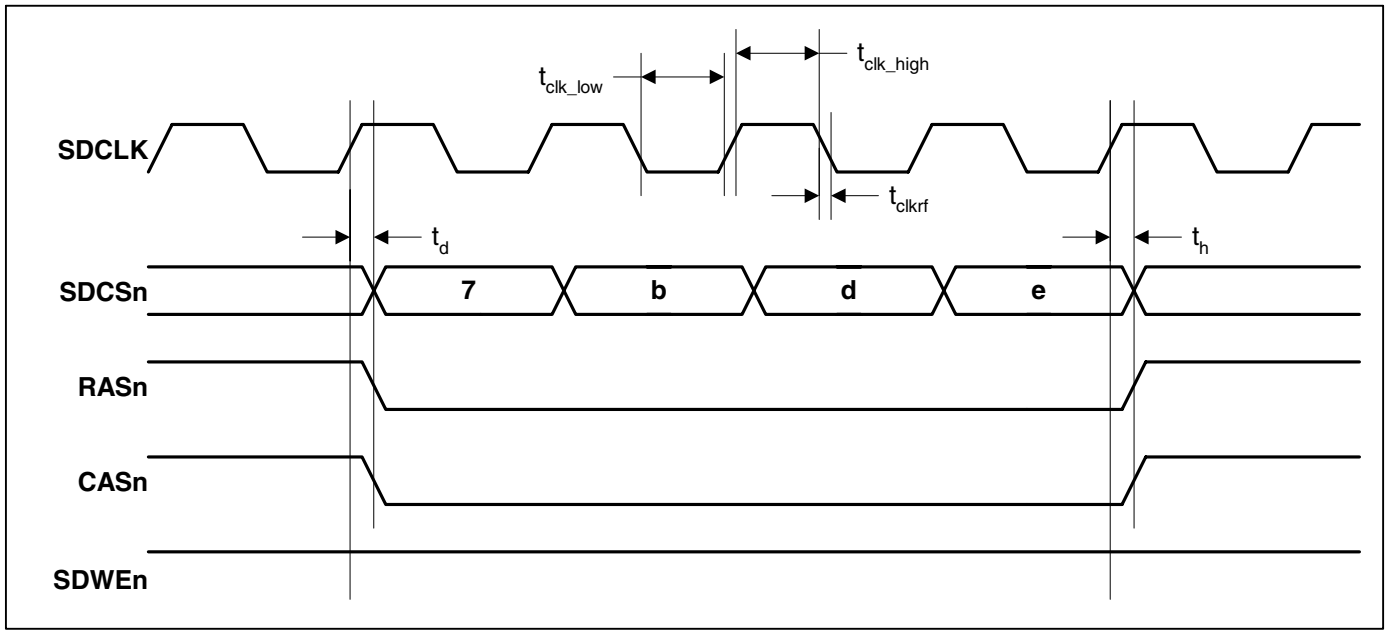


Figure 4. SDRAM Burst Write Cycle Timing Measurement

SDRAM Auto Refresh Cycle



Note: Chip select shown as bus to illustrate multiple devices being put into auto refresh in one access

Figure 5. SDRAM Auto Refresh Cycle Timing Measurement

Static Memory 32-bit Read on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to Address transition time	t_{AD1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{AD2}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{AD3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times (4 \times WST1 + 5)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

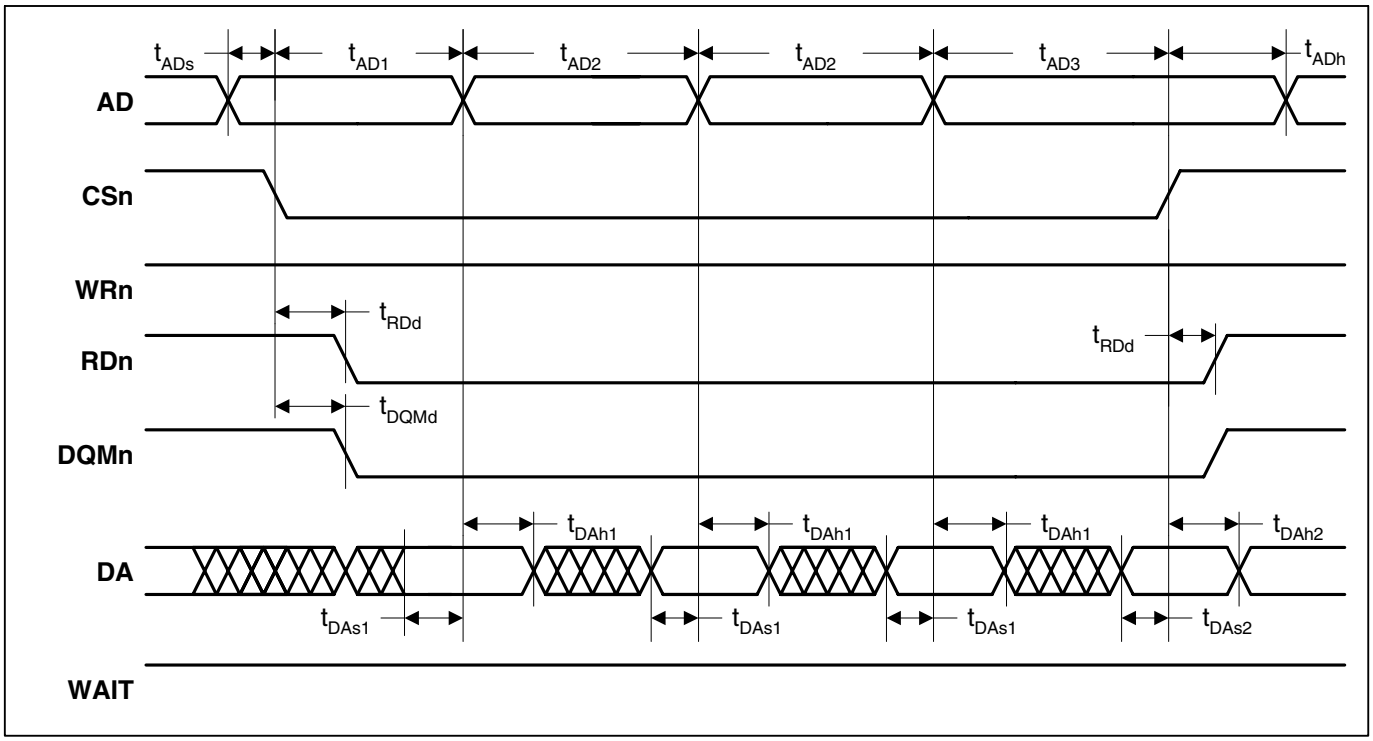


Figure 8. Static Memory Multiple Word Read 8-bit Cycle Timing Measurement

Static Memory 32-bit Write on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	$t_{HCLK} \times 2$	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

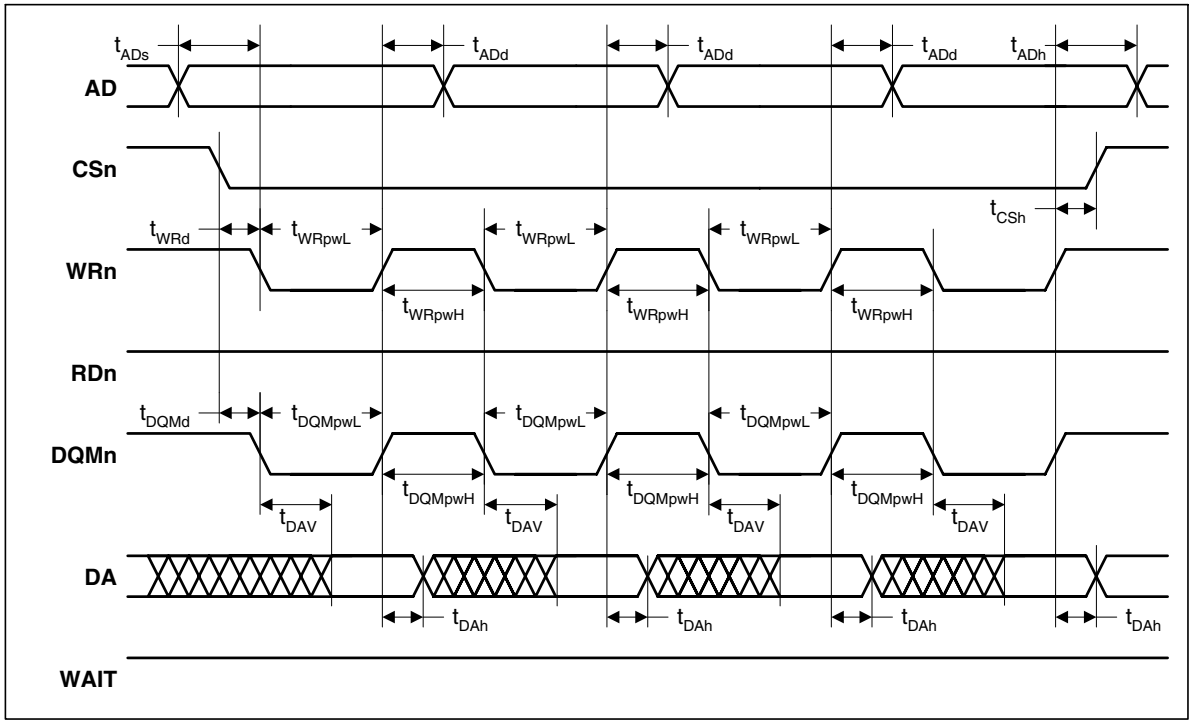


Figure 9. Static Memory Multiple Word Write 8-bit Cycle Timing Measurement

Static Memory 32-bit Read on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to AD transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd2}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times ((2 \times WST1) + 3)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

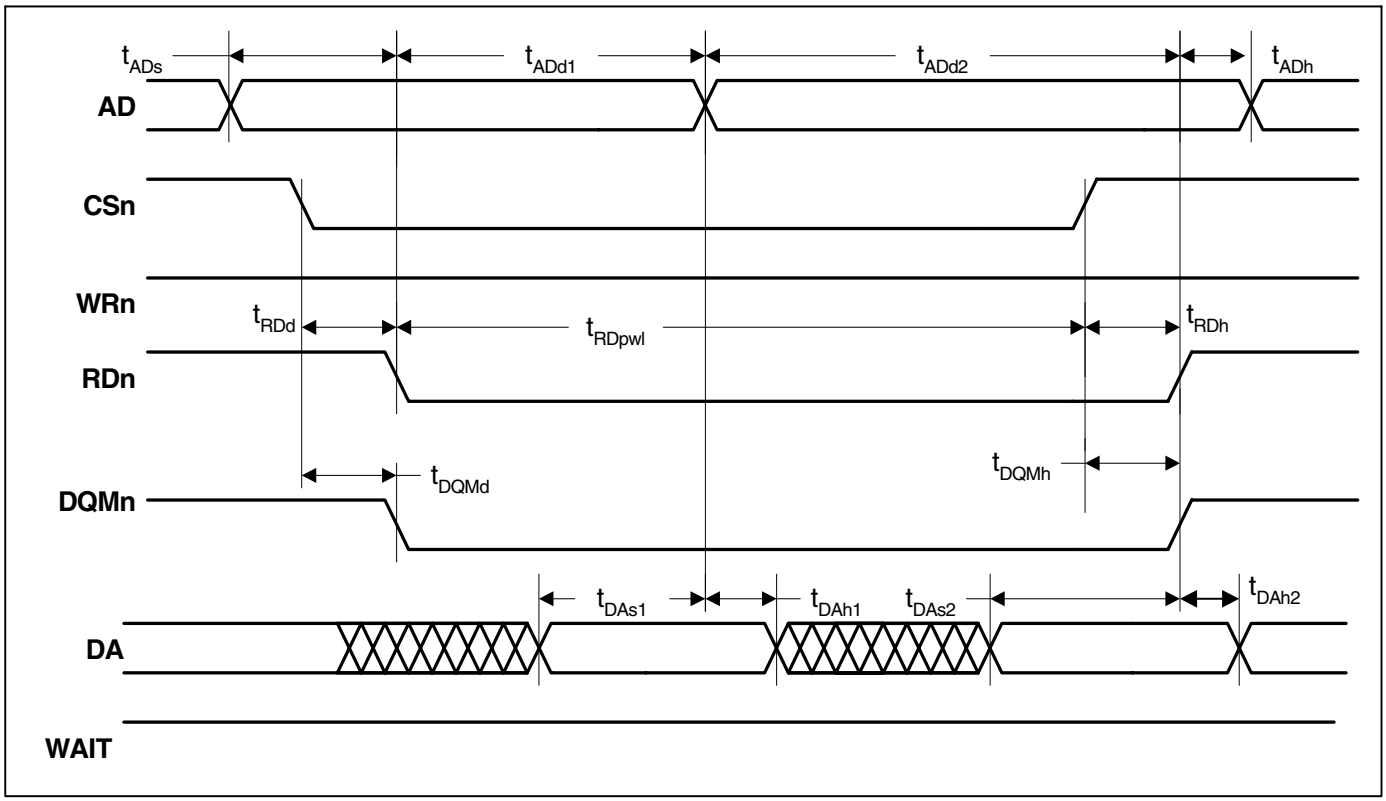


Figure 10. Static Memory Multiple Word Read 16-bit Cycle Timing Measurement

Static Memory 32-bit Write on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	-	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh1}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

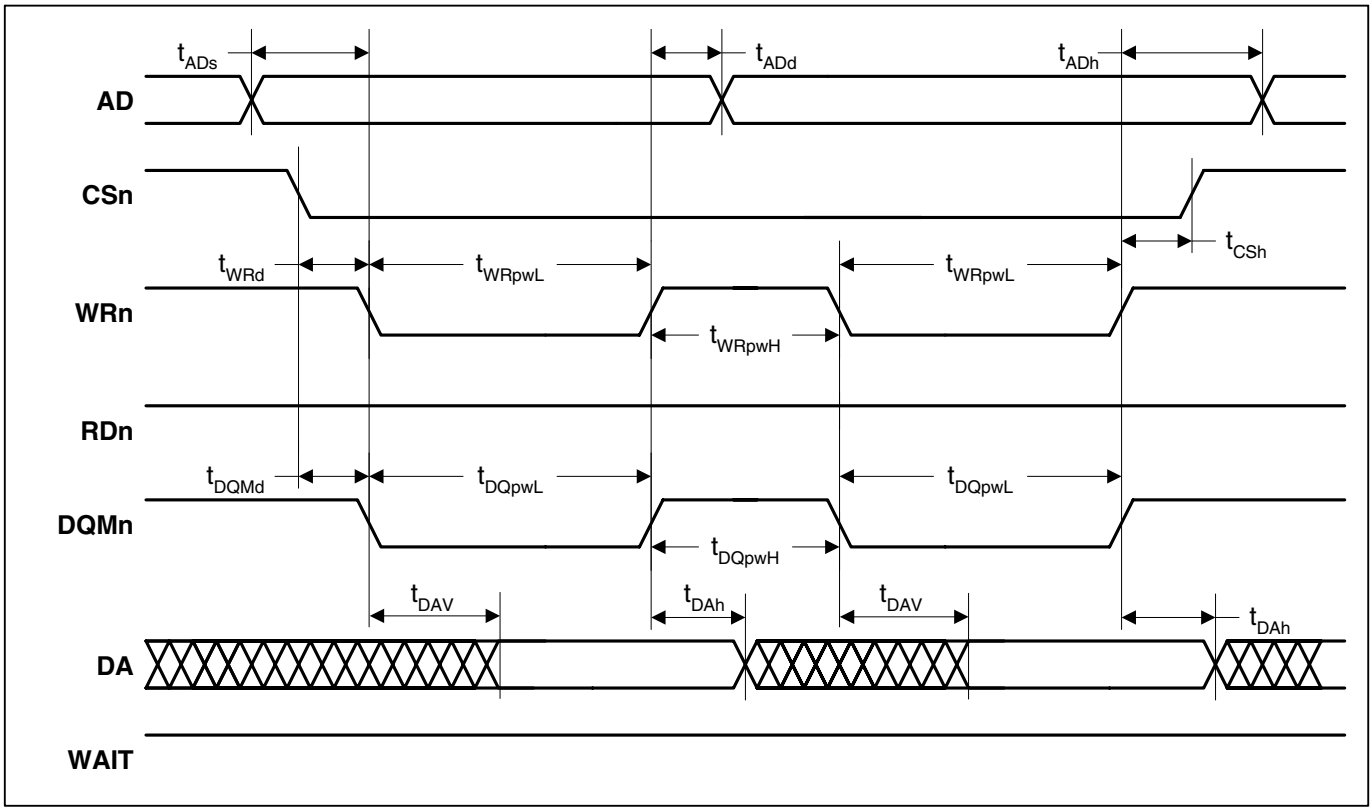


Figure 11. Static Memory Multiple Word Write 16-bit Cycle Timing Measurement

Static Memory Single Read Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times (WST1-2)$	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

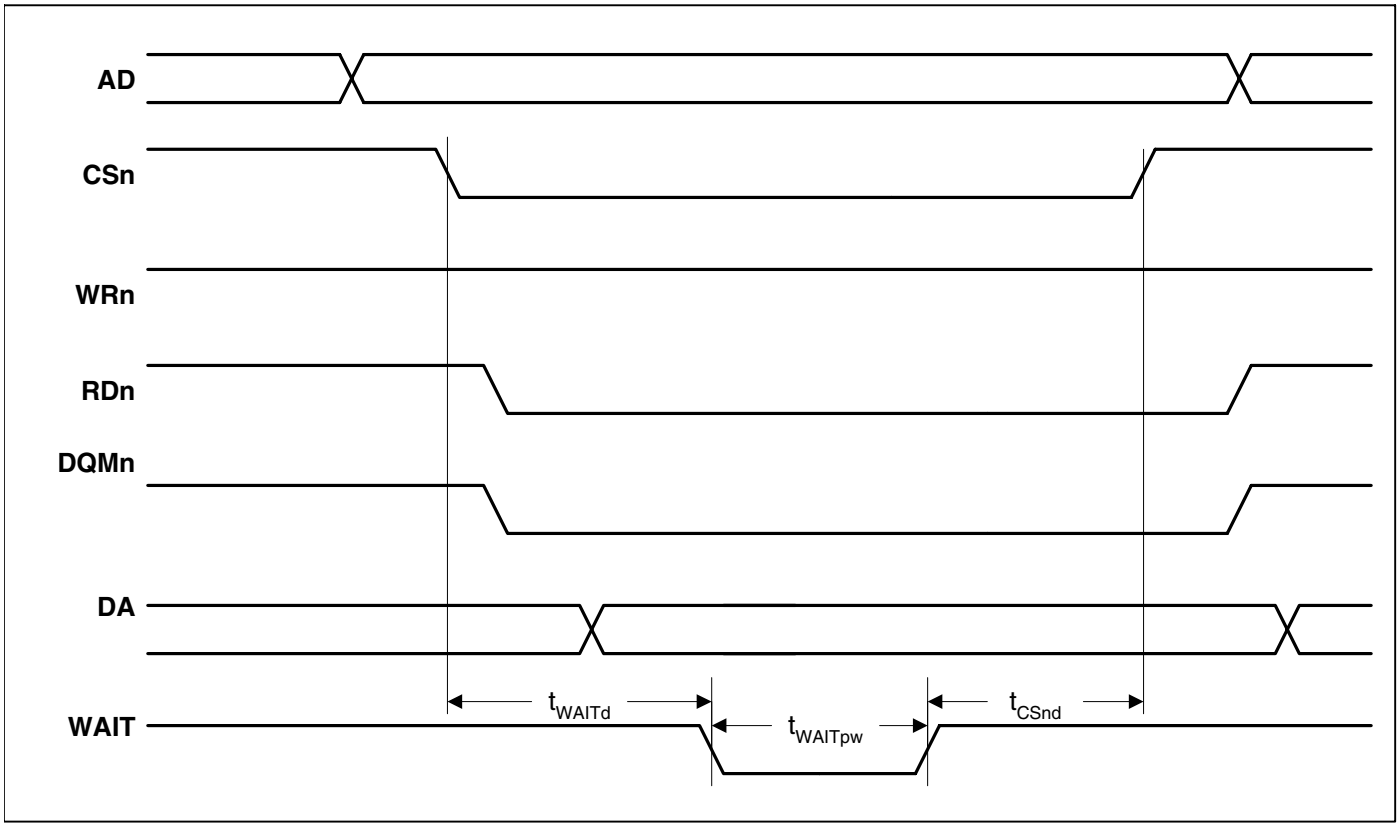


Figure 14. Static Memory Single Read Wait Cycle Timing Measurement

Static Memory Single Write Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
WAIT to WRn deassert delay time	t_{WRd}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 4$	ns
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times$ (WST1-2)	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

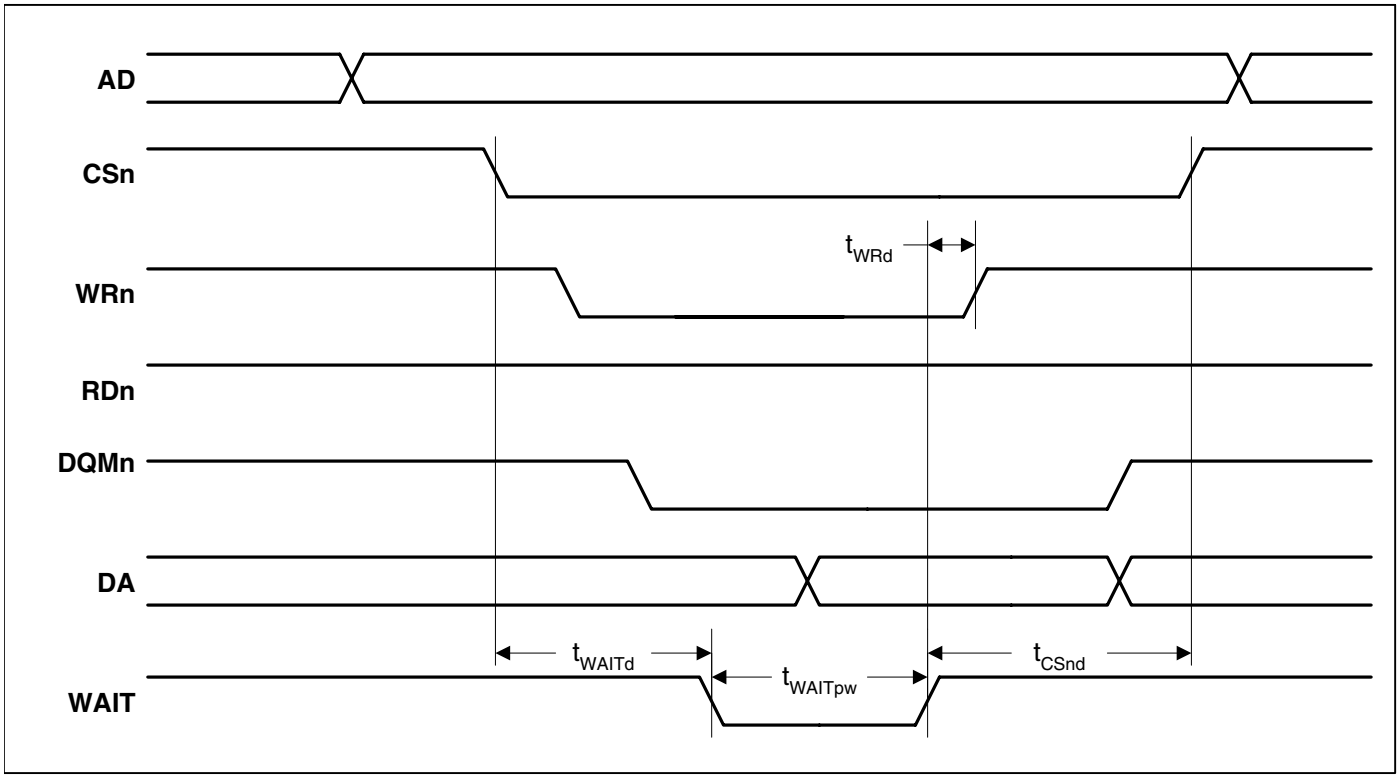


Figure 15. Static Memory Single Write Wait Cycle Timing Measurement

IDE Interface

Register Transfers

Parameter			Symbol	Mode 0 (in ns)	Mode 1 (in ns)	Mode 2 (in ns)	Mode 3 (in ns)	Mode 4 (in ns)
Cycle time	(min)	(Notes 1, 4, 5)	t_0	600	383	330	180	120
Address valid to DIORn / DIOWn setup	(min)	(Note 4)	t_1	70	50	30	30	25
DIORn / DIOWn pulse width 8-bit	(min)	(Note 1, 4)	t_2	290	290	290	80	70
DIORn / DIOWn recovery time	(min)	(Note 1, 4)	t_{2i}	-	-	-	70	25
DIOWn data setup	(min)	(Note 4)	t_3	60	45	30	30	20
DIOWn data hold	(min)		t_4	0	0	0	0	0
DIORn data setup	(min)		t_5	20	20	20	20	20
DIORn data hold	(min)		t_6	0	0	0	0	0
DIORn data high impedance state	(max)	(Note 2, 4)	t_{6z}	30	30	30	30	30
DIORn / DIOWn to address valid hold	(min)	(Note 4)	t_9	20	15	10	10	10
Read Data Valid to IORDY active (if IORDY initially low after t_A)	(min)	(Note 4)	t_{RD}	0	0	0	0	0
IORDY Setup time		(Note 3, 4)	t_A	35	35	35	35	35
IORDY Pulse Width	(max)	(Note 4)	t_B	1250	1250	1250	1250	1250
IORDY assertion to release	(max)		t_C	5	5	5	5	5
DIOWn assert to data valid	(max)		t_{DDV}	10	10	10	10	10

Note: 1. t_0 is the minimum total cycle time, t_2 is the minimum DIORn / DIOWn assertion time, and t_{2i} is the minimum DIORn / DIOWn negation time. A host implementation shall lengthen t_2 and/or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

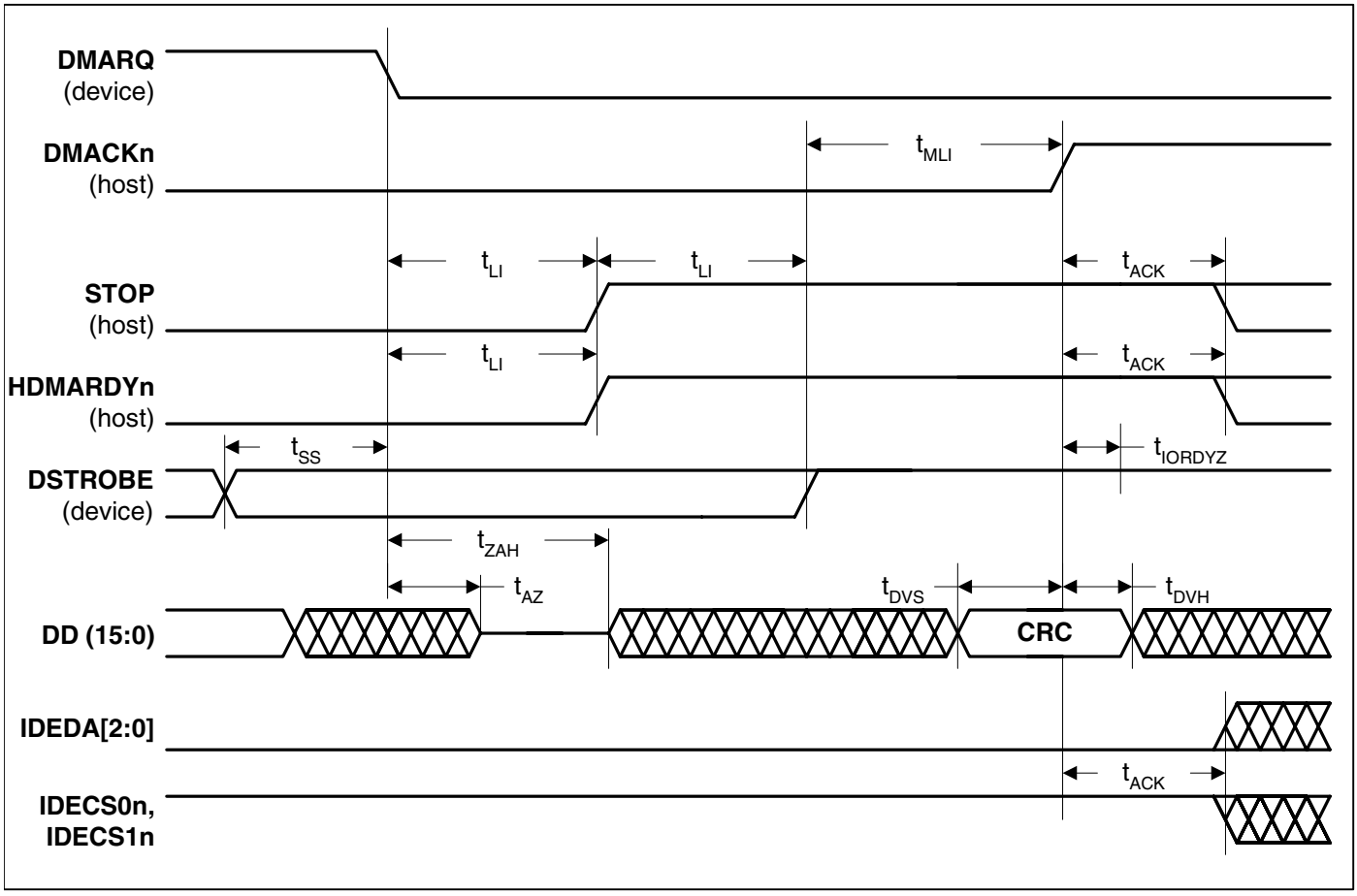
2. This parameter specifies the time from the negation edge of DIORn to the time that the data bus is released by the device.

3. The delay from the activation of DIORn or DIOWn until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the register transfer cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIORn or DIOWn, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIORn or DIOWn, then t_{RD} shall be met and t_5 is not applicable.

4. Timings based upon software control. See User's Guide.

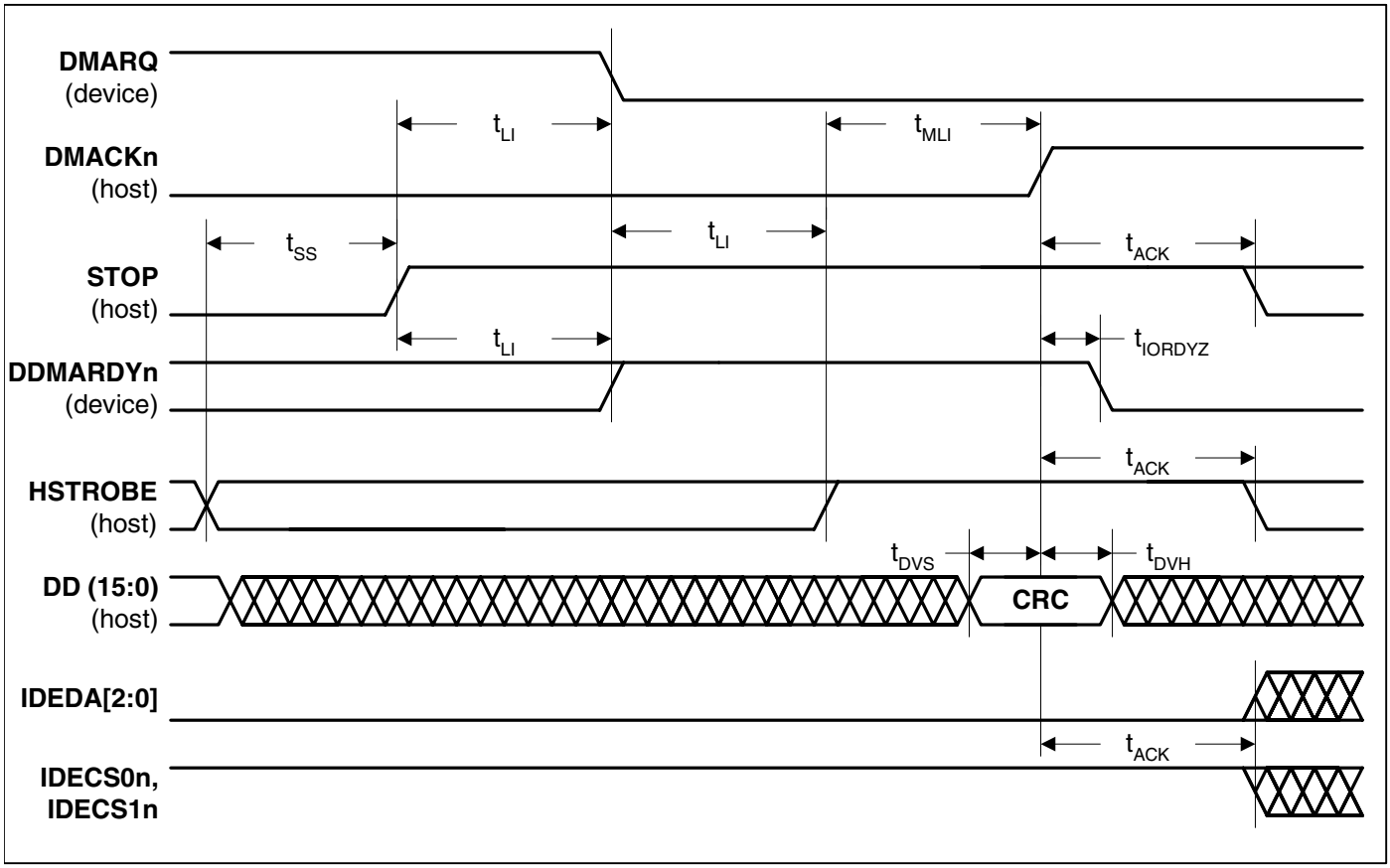
5. ATA / ATAPI standards prior to ATA / ATAPI-5 inadvertently specified an incorrect value for mode 2 time t_0 by utilizing the 16-bit PIO value.

6. All IDE timing is based upon HCLK = 100 MHz.



Note: The definitions for the DIOWn:STOP, DIORn:HDMARDYn:HSTROBE and IORDY:DDMARDYn:DSTROBE signal lines are no longer in effect after DMARQ and DMACKn are negated.

Figure 22. Device Terminating an Ultra DMA data-in Burst



Note: The definitions for the DIOWn:STOP, IORDY:DDMARDYn:DSTROBE and DIORn:HDMARDYn:HSTROBE signal lines are no longer in effect after DMARQ and DMACKn are negated.

Figure 27. Host Terminating an Ultra DMA data-out Burst

Audio Interface

The following table contains the values for the timings of each of the SPI modes.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{clk_per}	-	tspix_clk	-	ns
SCLK high time	t_{clk_high}	-	(tspix_clk) / 2	-	ns
SCLK low time	t_{clk_low}	-	(tspix_clk) / 2	-	ns
SCLK rise/fall time	t_{clkrf}	1	-	8	ns
Data from master valid delay time	t_{DMd}	-	-	3	ns
Data from master setup time	t_{DMs}	20	-	-	ns
Data from master hold time	t_{DMh}	40	-	-	ns
Data from slave setup time	t_{DSs}	20	-	-	ns
Data from slave hold time	t_{DSh}	40	-	-	ns

Note: The tspix_clk is programmable by the user.

LCD Interface

Parameter	Symbol	Min	Typ	Max	Unit
SPCLK rise/fall time	t_{clkr}	2	-	8	ns
SPCLK rising edge to control signal transition time	t_{CD}	-	-	3	ns
SPCLK rising edge to data transition time	t_{DD}	-	-	10	ns
Data valid time	t_{Dv}	t_{SPCLK}	-	-	ns

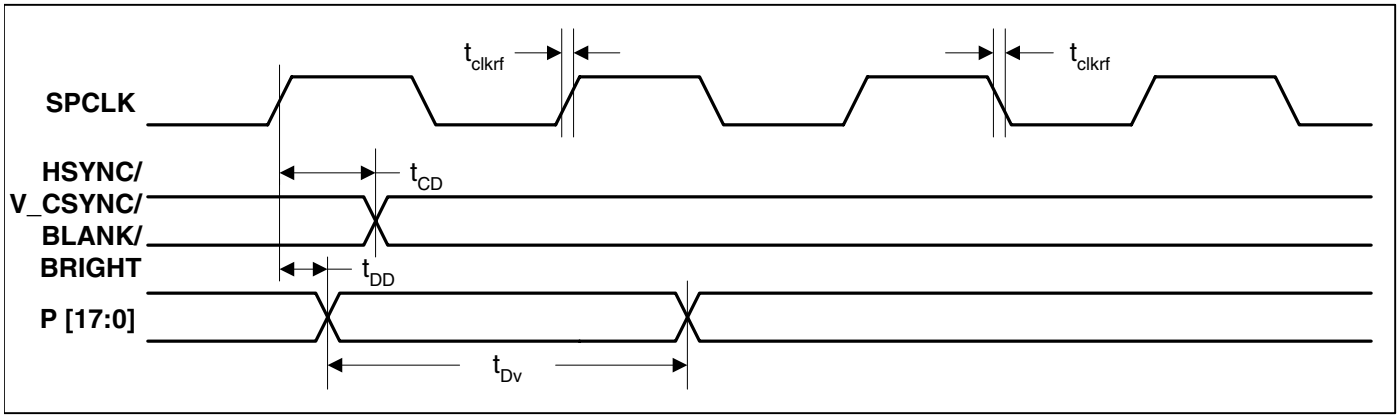


Figure 35. LCD Timing Measurement

352 Pin BGA Package Outline

352-Ball PBGA Diagram

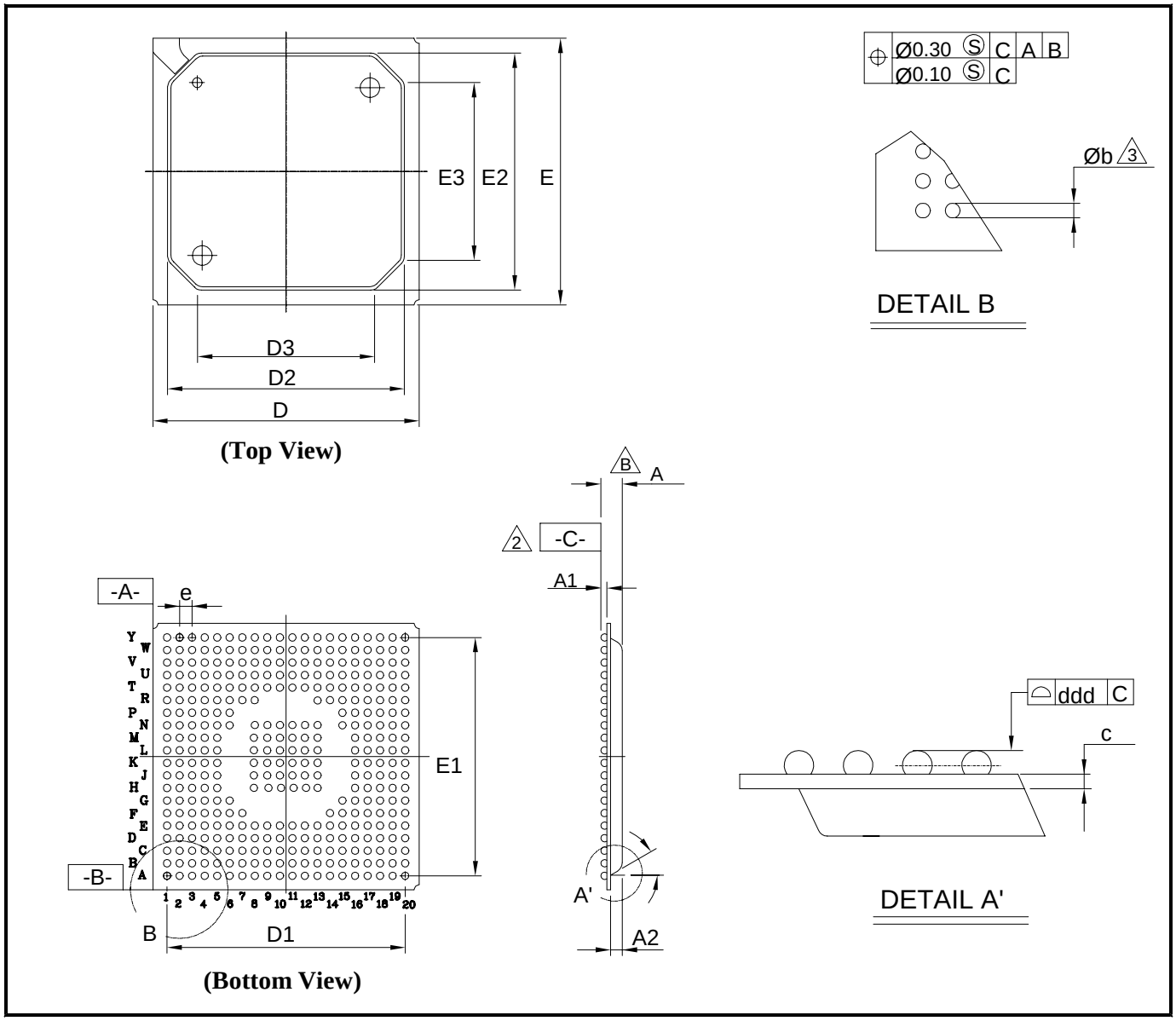


Figure 38. 352 Pin PBGA Pin Diagram

Figure 40. 352 PIN BGA PINOUT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
Y	HSYNC	DD[1]	DD[12]	P[2]	AD[15]	DA[6]	DA[4]	AD[10]	DA[1]	AD[8]	IDEDA[0]	DTRN	TDO	BOOT[0]	EEDAT	ASDO	SFRM1	RDLED	USBP[1]	ABITCLK	**Y**
W	P[12]	P[9]	DD[0]	P[5]	P[3]	DA[7]	DA[5]	AD[11]	AD[9]	IDECS1N	IDEDA[1]	TCK	TMS	EECLK	SCLK1	GRLED	INT[3]	SLA[1]	SLA[0]	RXD[2]	**W**
V	P[16]	P[11]	P[8]	DD[15]	DD[13]	P[1]	AD[14]	AD[12]	DA[2]	IDECS0N	IDEDA[2]	TDI	GND	ASYNC	SSPTX1	INT[2]	RTSN	USBP[0]	CTSN	TXD[0]	**V**
U	AD[0]	P[15]	P[10]	P[7]	P[6]	P[4]	P[0]	AD[13]	DA[3]	DA[0]	DSRN	BOOT[1]	NC	SSPRX1	INT[1]	PWMOUT	USBM[0]	RXD[1]	TXD[1]	ROW[1]	**U**
T	DA[8]	BLANK	P[13]	SPCLK	V_CSYNC	DD[14]	GND	CVDD	RVDD	GND	GND	RVDD	CVDD	GND	INT[0]	USBM[1]	RXD[0]	TXD[2]	ROW[2]	ROW[4]	**T**
R	AD[2]	AD[1]	P[17]	P[14]	RVDD	RVDD	GND	CVDD					CVDD	GND	RVDD	RVDD	ROW[0]	ROW[3]	PLL_GND	ROW[5]	**R**
P	AD[4]	DA[10]	DA[9]	BRIGHT	RVDD	RVDD									RVDD	RVDD	XTALI	PLL_VDD	ROW[6]	ROW[7]	**P**
N	DA[13]	DA[12]	DA[11]	AD[3]	CVDD	CVDD		GND	GND	GND	GND	GND	GND		GND	GND	XTALO	COL[0]	COL[1]	COL[2]	**N**
M	AD[7]	DA[14]	AD[6]	AD[5]	CVDD			GND	GND	GND	GND	GND	GND			GND	COL[4]	COL[3]	COL[6]	CSN[0]	**M**
L	DA[18]	DA[17]	DA[16]	DA[15]	GND			GND	GND	GND	GND	GND	GND			CVDD	COL[5]	COL[7]	RSTON	PRSTN	**L**
K	AD[22]	DA[20]	AD[21]	DA[19]	RVDD			GND	GND	GND	GND	GND	GND			CVDD	SYM	SYP	SXM	SXP	**K**
J	DA[21]	DQMN[0]	DQMN[1]	DQMN[2]	GND			GND	GND	GND	GND	GND	GND			CVDD	RTCXTALI	XM	YP	YM	**J**
H	DQMN[3]	CASN	RASN	SDCSN[2]	CVDD			GND	GND	GND	GND	GND	GND			RVDD	RTCXTALO	ADC_VDD	ADC_GND	XP	**H**
G	SDCSN[0]	SDCSN[1]	SDWEN	SDCLK	RVDD	RVDD									RVDD	RVDD	EGPIO[7]	EGPIO[9]	EGPIO[10]	EGPIO[11]	**G**
F	SDCSN[3]	DA[22]	DA[24]	AD[25]	RVDD	GND	CVDD							CVDD	GND	GND	EGPIO[2]	EGPIO[4]	EGPIO[6]	EGPIO[8]	**F**
E	AD[23]	DA[23]	DA[26]	CSN[6]	GND	GND	CVDD	CVDD	RVDD	GND	GND	RVDD	CVDD	CVDD	GND	ASDI	DIOWN	EGPIO[0]	EGPIO[3]	EGPIO[5]	**E**
D	AD[24]	DA[25]	DD[11]	SDCLKEN	AD[19]	DD[9]	DD[5]	AD[16]	MIIRXD[2]	MIITXD[3]	TXEN	NC	NC	NC	EGPIO[14]	NC	USBM[2]	ARSTN	DIORN	EGPIO[1]	**D**
C	CSN[1]	CSN[3]	AD[20]	DA[29]	DD[10]	DD[6]	DD[2]	MDC	MIIRXD[3]	TXCLK	MIITXD[0]	NC	NC	NC	NC	NC	NC	USBP[2]	IORDY	DMACKN	**C**
B	CSN[2]	DA[31]	DA[30]	DA[27]	DD[7]	DD[3]	WRN	MDIO	MIIRXD[1]	RXERR	MIITXD[1]	CRS	NC	NC	NC	NC	EGPIO[13]	NC	WAITN	TRSTN	**B**
A	CSN[7]	DA[28]	AD[18]	DD[8]	DD[4]	AD[17]	RDN	RXCLK	MIIRXD[0]	RXDVAL	MIITXD[2]	TXERR	CLD	NC	NC	NC	EGPIO[12]	EGPIO[15]	NC	NC	**A**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	

The following section focuses on the EP9312 pin signals from two viewpoints - the pin usage and pad characteristics, and the pin multiplexing usage. The first table (Table S) is a summary of all the EP9312 pin signals. The second table (Table T) illustrates the pin signal multiplexing and configuration options.

Table S is a summary of the EP9312 pin signals, which illustrates the pad type and pad pull type (if any). The symbols used in the table are defined as follows. (Note: A blank box means Not Applicable (NA) or, for Pull Type, No Pull (NP).)

Under the Pad Type column:

- A - Analog pad
- P - Power pad
- G - Ground pad
- I - Pin is an input only
- I/O - Pin is input/output
- 4mA - Pin is a 4 mA output driver
- 8mA - Pin is an 8 mA output driver
- 12mA - Pin is an 12 mA output driver

See the text description for additional information about bi-directional pins.

Under the Pull Type Column:

- PU - Resistor is a pull up to the RVDD supply
- PD - Resistor is a pull down to the RGND supply