# Renesas Electronics America Inc - R5F212K2SNFP#X6 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | LINbus, SIO, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 25 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 5.5V |
| Data Converters | A/D 9x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212k2snfp-x6 |

# 1. Overview

## 1.1 Features

The R8C/2K Group and R8C/2L Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.
Furthermore, the R8C/2L Group has on-chip data flash (1 KB × 2 blocks).
The difference between the R8C/2K Group and R8C/2L Group is only the presence or absence of data flash. Their peripheral functions are the same.

### 1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

**Table 1.3 Specifications for R8C/2L Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C/Tiny series core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to **Table 1.6 Product List for R8C/2L Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 |
| I/O Ports | Programmable I/O ports | • Input-only: 3 pins<br>• CMOS I/O ports: 25, selectable pull-up resistor<br>• High current drive ports: 8 |
| Clock | Clock generation circuits | 2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),<br>On-chip oscillator (high-speed, low-speed)<br>(high-speed on-chip oscillator has a frequency adjustment function)<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • External: 4 sources, Internal: 15 sources, Software: 4 sources<br>• Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits × 2 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |

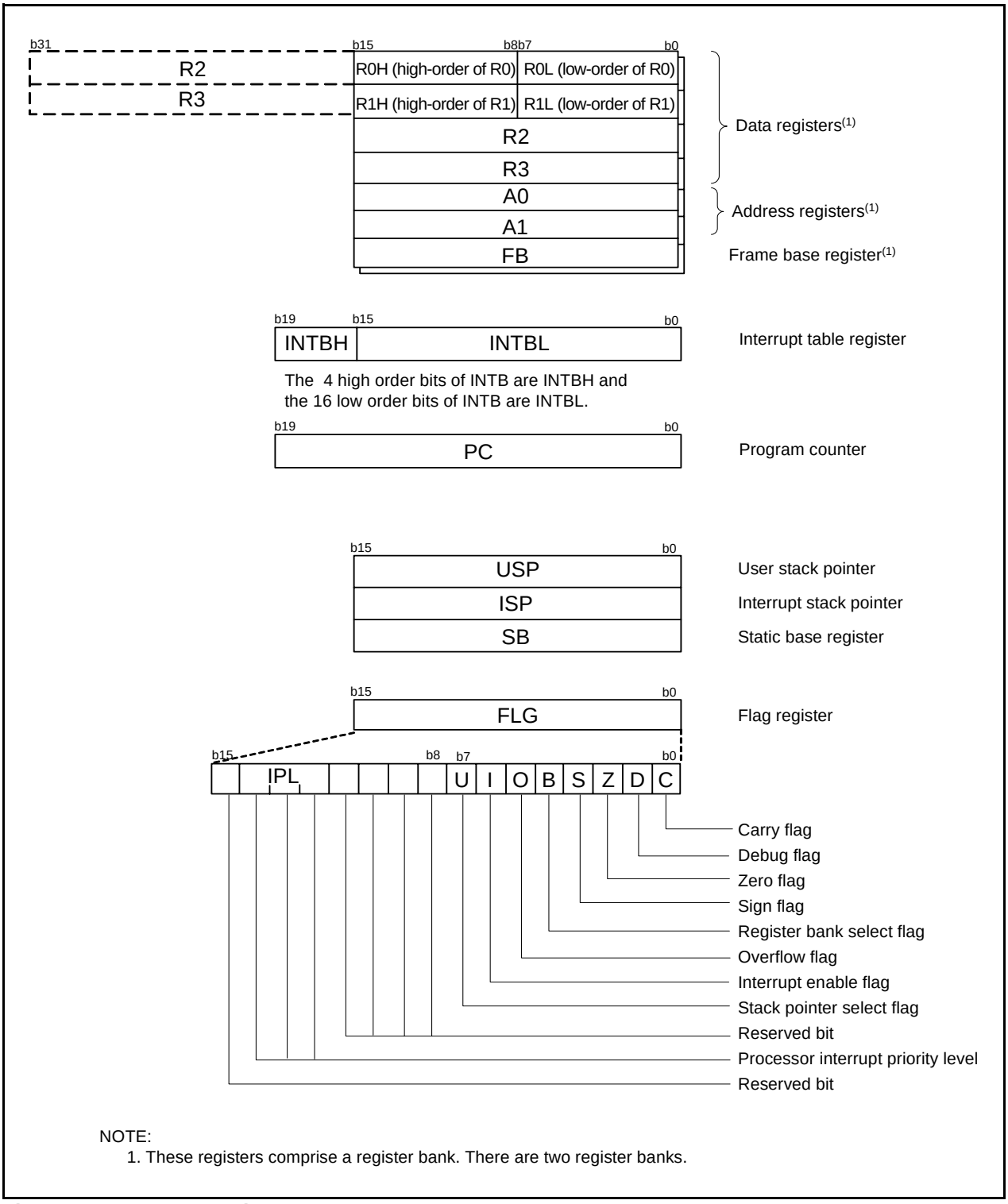
**Table 1.4 Specifications for R8C/2L Group (2)**

| Item | Function | Specification |
|---|---|---|
| Serial Interface | UART0, UART2 | Clock synchronous serial I/O/UART × 2 |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| A/D Converter | | 10-bit resolution × 9 channels, includes sample and hold function |
| Flash Memory | | • Programming and erasure voltage: VCC = 2.7 to 5.5 V<br>• Programming and erasure endurance: 10,000 times (data flash)<br>1,000 times (program ROM)<br>• Program security: ROM code protect, ID code check<br>• Debug functions: On-chip debug, on-board flash rewrite function |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V)<br>f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V)<br>f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V) (VCC = 2.7 to 5.5 V for A/D converter only) |
| Current consumption | | Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz)<br>Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz)<br>Typ. 23 μA (VCC = 3.0 V, wait mode, low-speed on-chip oscillator used)<br>Typ. 0.7 μA (VCC = 3.0 V, stop mode) |
| Operating Ambient Temperature | | -20 to 85°C (N version)<br>-40 to 85°C (D version)(1)<br>-20 to 105°C (Y version)(2) |
| Package | | 32-pin LQFP<br>• Package code: PLQP0032GB-A (previous code: 32P6U-A) |

NOTES:
1. Specify the D version if D version functions are to be used.
2. Please contact Renesas Technology sales offices for the Y version.

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.




NOTE:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 CPU Registers**

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

**Table 4.5 SFR Information (5)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0100h | Timer RA Control Register | TRACR | 00h |
| 0101h | Timer RA I/O Control Register | TRAIOC | 00h |
| 0102h | Timer RA Mode Register | TRAMR | 00h |
| 0103h | Timer RA Prescaler Register | TRAPRE | FFh |
| 0104h | Timer RA Register | TRA | FFh |
| 0105h | LIN Control Register 2 | LINCR2 | 00h |
| 0106h | LIN Control Register | LINCR | 00h |
| 0107h | LIN Status Register | LINST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | | | |
| 0111h | | | |
| 0112h | | | |
| 0113h | | | |
| 0114h | | | |
| 0115h | | | |
| 0116h | | | |
| 0117h | | | |
| 0118h | | | |
| 0119h | | | |
| 011Ah | | | |
| 011Bh | | | |
| 011Ch | | | |
| 011Dh | | | |
| 011Eh | | | |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011111b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | | | |
| 0134h | | | |
| 0135h | | | |
| 0136h | | | |
| 0137h | Timer RD Start Register | TRDSTR | 11111100b |
| 0138h | Timer RD Mode Register | TRDMR | 00001110b |
| 0139h | Timer RD PWM Mode Register | TRDPMR | 10001000b |
| 013Ah | Timer RD Function Control Register | TRDFCR | 10000000b |
| 013Bh | Timer RD Output Master Enable Register 1 | TRDOER1 | FFh |
| 013Ch | Timer RD Output Master Enable Register 2 | TRDOER2 | 01111111b |
| 013Dh | Timer RD Output Control Register | TRDOCR | 00h |
| 013Eh | Timer RD Digital Filter Function Select Register 0 | TRDDF0 | 00h |
| 013Fh | Timer RD Digital Filter Function Select Register 1 | TRDDF1 | 00h |

NOTE:
1. The blank regions are reserved. Do not access locations in these regions

# 5. Electrical Characteristics

The electrical characteristics of N version (Topr = –20°C to 85°C) and D version (Topr = –40°C to 85°C) are listed below.
Please contact Renesas Technology sales offices for the electrical characteristics in the Y version (Topr = –20°C to 105°C).

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | Condition | Rated Value | Unit |
|---|---|---|---|---|
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | –0.3 to 6.5 | V |
| $V_I$ | Input voltage | | –0.3 to $V_{CC}$ + 0.3 | V |
| $V_O$ | Output voltage | | –0.3 to $V_{CC}$ + 0.3 | V |
| $P_d$ | Power dissipation | $T_{opr}$ = 25°C | 500 | mW |
| $T_{opr}$ | Operating ambient temperature | | –20 to 85 (N version) / –40 to 85 (D version) | °C |
| $T_{stg}$ | Storage temperature | | –65 to 150 | °C |

**Table 5.2 Recommended Operating Conditions**

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage | | | 2.2 | – | 5.5 | V |
| $AV_{CC}$ | Supply voltage | | | 2.7 | – | 5.5 | |
| $V_{SS}/AV_{SS}$ | Supply voltage | | | – | 0 | – | V |
| $V_{IH}$ | Input “H” voltage | | | 0.8 $V_{CC}$ | – | $V_{CC}$ | V |
| $V_{IL}$ | Input “L” voltage | | | 0 | – | 0.2 $V_{CC}$ | V |
| $I_{OH(sum)}$ | Peak sum output “H” current | Sum of all pins $I_{OH(peak)}$ | | – | – | –160 | mA |
| $I_{OH(sum)}$ | Average sum output “H” current | Sum of all pins $I_{OH(avg)}$ | | – | – | –80 | mA |
| $I_{OH(peak)}$ | Peak output “H” current | Except P2_0 to P2_7 | | – | – | –10 | mA |
| | | P2_0 to P2_7 | | – | – | –40 | mA |
| $I_{OH(avg)}$ | Average output “H” current | Except P2_0 to P2_7 | | – | – | –5 | mA |
| | | P2_0 to P2_7 | | – | – | –20 | mA |
| $I_{OL(sum)}$ | Peak sum output “L” currents | Sum of all pins $I_{OL(peak)}$ | | – | – | 160 | mA |
| $I_{OL(sum)}$ | Average sum output “L” currents | Sum of all pins $I_{OL(avg)}$ | | – | – | 80 | mA |
| $I_{OL(peak)}$ | Peak output “L” currents | Except P2_0 to P2_7 | | – | – | 10 | mA |
| | | P2_0 to P2_7 | | – | – | 40 | mA |
| $I_{OL(avg)}$ | Average output “L” current | Except P2_0 to P2_7 | | – | – | 5 | mA |
| | | P2_0 to P2_7 | | – | – | 20 | mA |
| $f_{(XIN)}$ | XIN clock input oscillation frequency | | 3.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 20 | MHz |
| | | | 2.7 V ≤ $V_{CC}$ < 3.0 V | 0 | – | 10 | MHz |
| | | | 2.2 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 5 | MHz |
| – | System clock | OCD2 = 0<br>XIN clock selected | 3.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 20 | MHz |
| | | | 2.7 V ≤ $V_{CC}$ < 3.0 V | 0 | – | 10 | MHz |
| | | | 2.2 V ≤ $V_{CC}$ < 2.7 V | 0 | – | 5 | MHz |
| | | OCD2 = 1<br>On-chip oscillator clock selected | FRA01 = 0<br>Low-speed on-chip oscillator clock selected | – | 125 | – | kHz |
| | | | FRA01 = 1<br>High-speed on-chip oscillator clock selected<br>3.0 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 20 | MHz |
| | | | FRA01 = 1<br>High-speed on-chip oscillator clock selected<br>2.7 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 10 | MHz |
| | | | FRA01 = 1<br>High-speed on-chip oscillator clock selected<br>2.2 V ≤ $V_{CC}$ ≤ 5.5 V | – | – | 5 | MHz |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

**Table 5.3 A/D Converter Characteristics**

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref}$ = $AV_{CC}$ | – | – | 10 | Bits |
| – | Absolute accuracy | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±3 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±2 | LSB |
| | | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±5 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±2 | LSB |
| $R_{ladder}$ | Resistor ladder | | $V_{ref}$ = $AV_{CC}$ | 10 | – | 40 | kΩ |
| $t_{conv}$ | Conversion time | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 3.3 | – | – | µs |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 2.8 | – | – | µs |
| $V_{ref}$ | Reference voltage | | | 2.2 | – | $AV_{CC}$ | V |
| $V_{IA}$ | Analog input voltage(2) | | | 0 | – | $AV_{CC}$ | V |
| – | A/D operating clock frequency | Without sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 0.25 | – | 10 | MHz |
| | | With sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 1 | – | 10 | MHz |

NOTES:
1. $AV_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

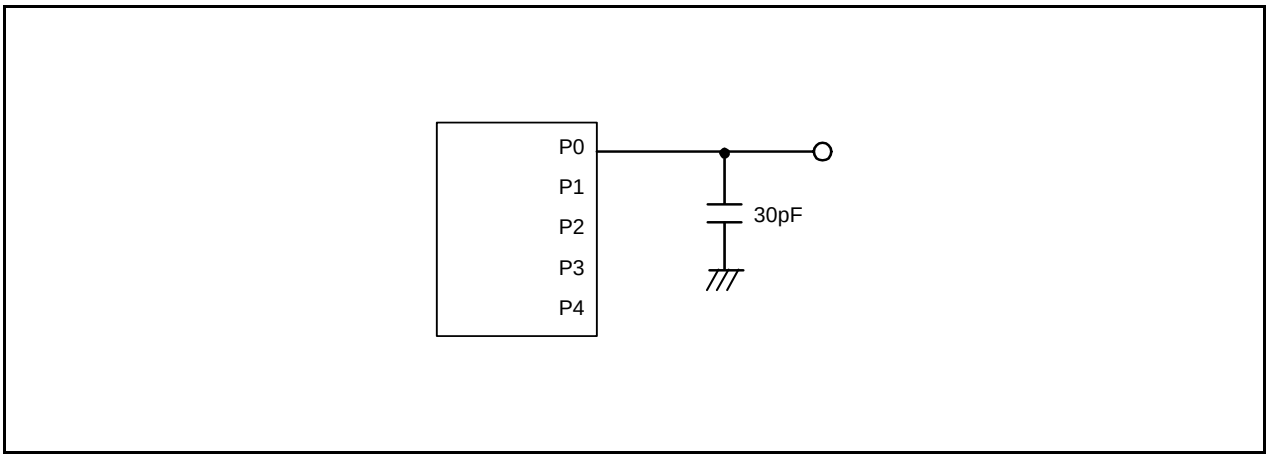



**Figure 5.1 Ports P0 to P4 Timing Measurement Circuit**

**Table 5.4 Flash Memory (Program ROM) Electrical Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance(2) | R8C/2K Group | 100(3) | – | – | times |
| | | R8C/2L Group | 1,000(3) | – | – | times |
| – | Byte program time | | – | 50 | 400 | µs |
| – | Block erase time | | – | 0.4 | 9 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | µs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | µs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time(7) | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance(2) | | 10,000(3) | – | – | times |
| – | Byte program time (program/erase endurance ≤ 1,000 times) | | – | 50 | 400 | µs |
| – | Byte program time (program/erase endurance > 1,000 times) | | – | 65 | – | µs |
| – | Block erase time (program/erase endurance ≤ 1,000 times) | | – | 0.2 | 9 | s |
| – | Block erase time (program/erase endurance > 1,000 times) | | – | 0.3 | – | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | µs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | µs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | –20(8) | – | 85 | °C |
| – | Data hold time(9) | Ambient temperature = 55 °C | 20 | – | – | year |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. –40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

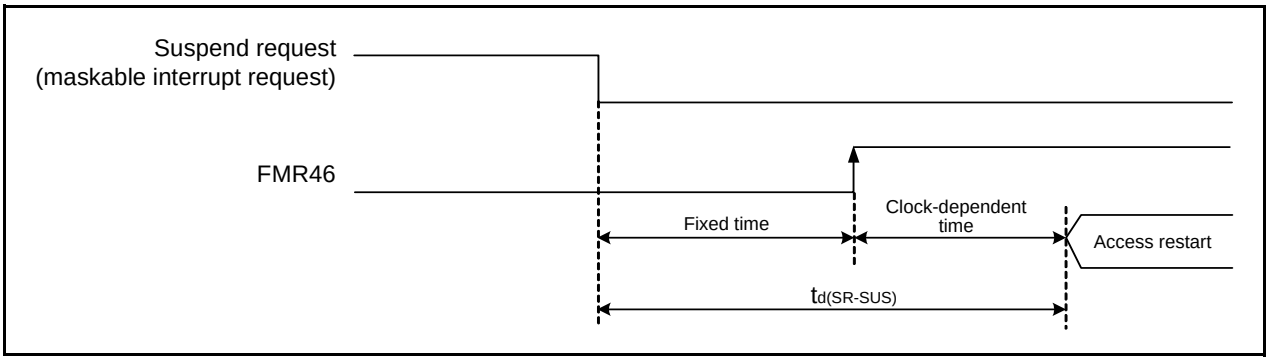



**Figure 5.2 Time delay until Suspend**

### Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det0}$ | Voltage detection level | | 2.2 | 2.3 | 2.4 | V |
| – | Voltage detection circuit self power consumption | VCA25 = 1, $V_{CC}$ = 5.0 V | – | 0.9 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(2) | | – | – | 300 | µs |
| Vccmin | MCU operating voltage minimum value | | 2.2 | – | – | V |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

### Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level(4) | | 2.70 | 2.85 | 3.00 | V |
| – | Voltage monitor 1 interrupt request generation time(2) | | – | 40 | – | µs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes $V_{det1}$.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

### Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level | | 3.3 | 3.6 | 3.9 | V |
| – | Voltage monitor 2 interrupt request generation time(2) | | – | 40 | – | µs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{det2}$.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

### Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature • supply voltage dependence | $V_{CC}$ = 2.7 V to 5.5 V<br>−20°C ≤ $T_{opr}$ ≤ 85°C(2) | 39.2 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V<br>−40°C ≤ $T_{opr}$ ≤ 85°C(2) | 39.0 | 40 | 41.0 | MHz |
| | | $V_{CC}$ = 2.2 V to 5.5 V<br>−20°C ≤ $T_{opr}$ ≤ 85°C(3) | 35.2 | 40 | 44.8 | MHz |
| | | $V_{CC}$ = 2.2 V to 5.5 V<br>−40°C ≤ $T_{opr}$ ≤ 85°C(3) | 34.0 | 40 | 46.0 | MHz |
| | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4) | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 36.864 | – | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V<br>−20°C ≤ $T_{opr}$ ≤ 85°C | −3% | – | 3% | % |
| – | Value in FRA1 register after reset | | 08h | – | F7h | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to -1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 550 | – | µA |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

### Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 15 | – | µA |

NOTE:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.

### Table 5.12 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on(2) | | 1 | – | 2000 | µs |
| $t_{d(R-S)}$ | STOP exit time(3) | | – | – | 150 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

**Table 5.15 Electrical Characteristics (3) [Vcc = 5 V]**
**(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power supply current ($V_{CC}$ = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are $V_{SS}$ | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 25 | 75 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 23 | 60 | µA |
| | | Stop mode | XIN clock off, $T_{opr}$ = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.8 | 3.0 | µA |
| | | | XIN clock off, $T_{opr}$ = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.2 | – | µA |

**Table 5.21 Electrical Characteristics (2) [Vcc = 3 V]**
**(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5 | 9 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 130 | 300 | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 25 | 70 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 23 | 55 | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | µA |

**Timing requirements**
**(Unless Otherwise Specified: $V_{CC}$ = 3 V, $V_{SS}$ = 0 V at $T_{opr}$ = 25°C) [$V_{CC}$ = 3 V]**

**Table 5.22 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 100 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 40 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 40 | – | ns |

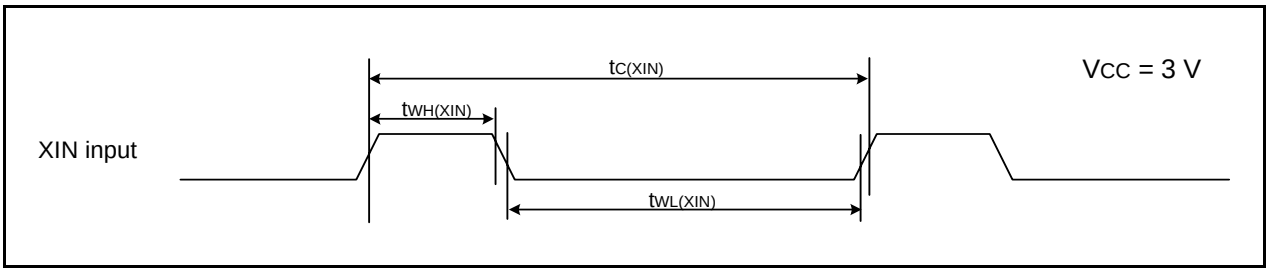



**Figure 5.8 XIN Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.23 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 300 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 120 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 120 | – | ns |

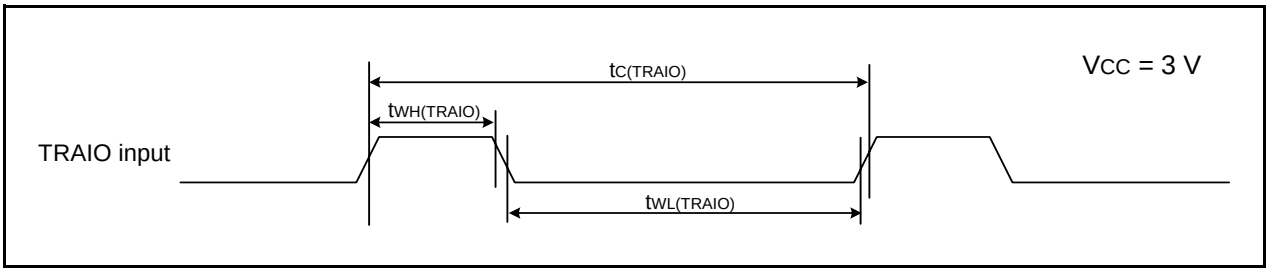



**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.24 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 150 | – | ns |
| $t_{W(CKL)}$ | CLKi Input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0, 2

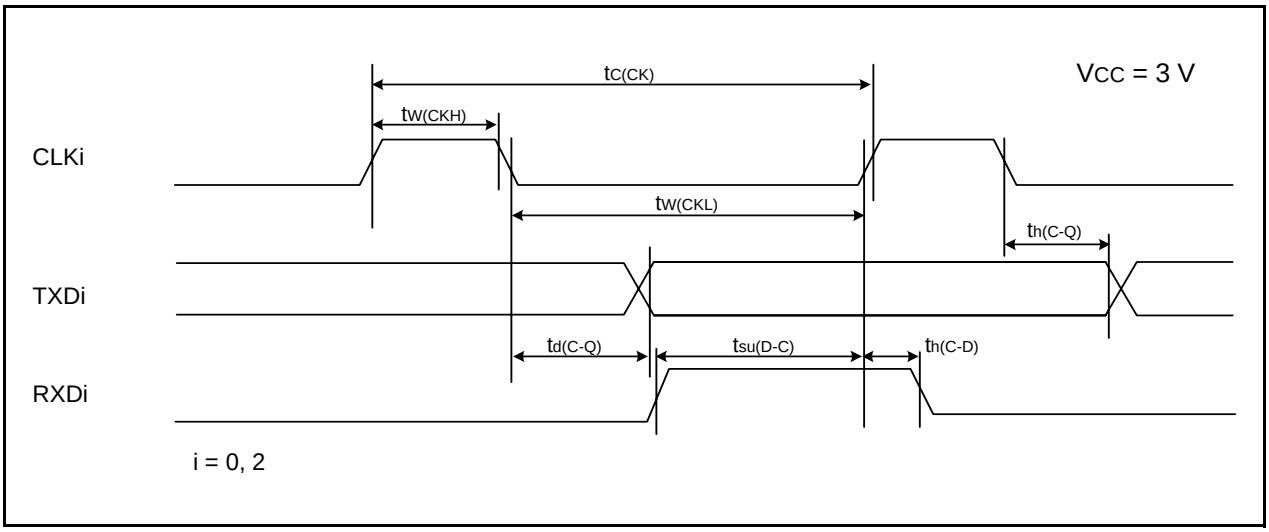



**Figure 5.10 Serial Interface Timing Diagram when VCC = 3 V**

**Table 5.25 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INTi}$ input “H” width | 380(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INTi}$ input “L” width | 380(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

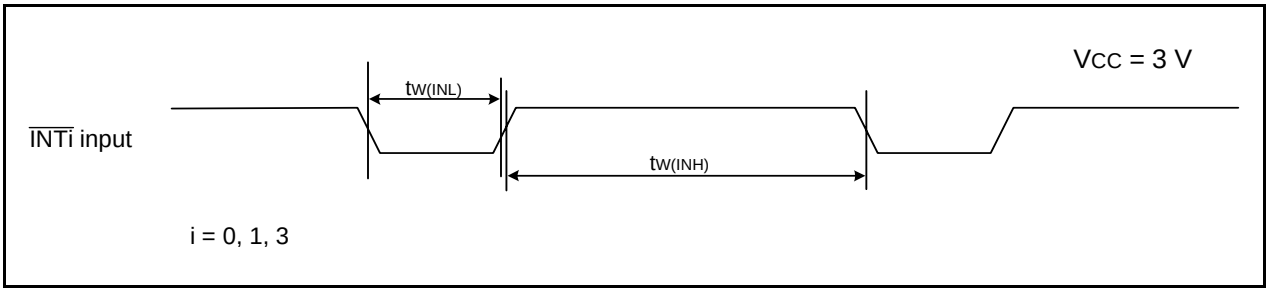



**Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V**

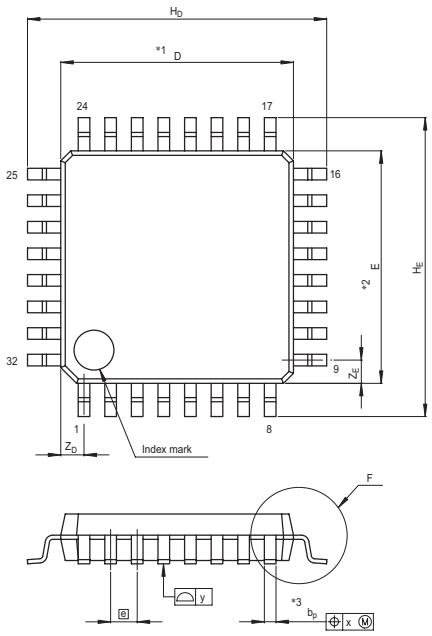
**Table 5.27 Electrical Characteristics (2) [Vcc = 2.2 V]**
**(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

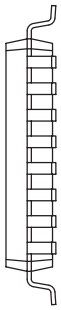
| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power supply current ($V_{CC}$ = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are $V_{SS}$ | High-speed clock mode | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.5 | – | mA |
| | | | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.5 | – | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 100 | 230 | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 22 | 60 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 20 | 55 | µA |
| | | Stop mode | XIN clock off, $T_{opr}$ = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | µA |
| | | | XIN clock off, $T_{opr}$ = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | µA |

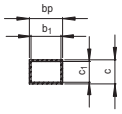
# Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

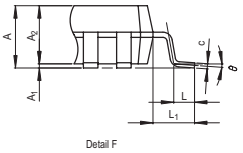
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP32-7x7-0.80 | PLQP0032GB-A | 32P6U-A | 0.2g |






Terminal cross section




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 8.8 | 9.0 | 9.2 |
| $H_E$ | 8.8 | 9.0 | 9.2 |
| A | — | — | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.32 | 0.37 | 0.42 |
| $b_1$ | — | 0.35 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.8 | — |
| x | — | — | 0.20 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.7 | — |
| $Z_E$ | — | 0.7 | — |
| L | 0.3 | 0.5 | 0.7 |
| $L_1$ | — | 1.0 | — |