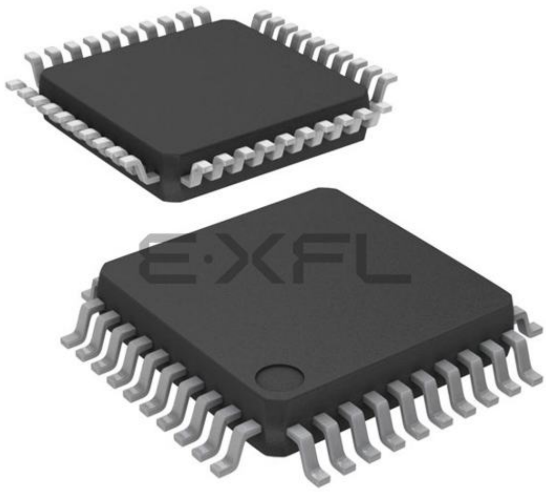

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212k4syfp-v2

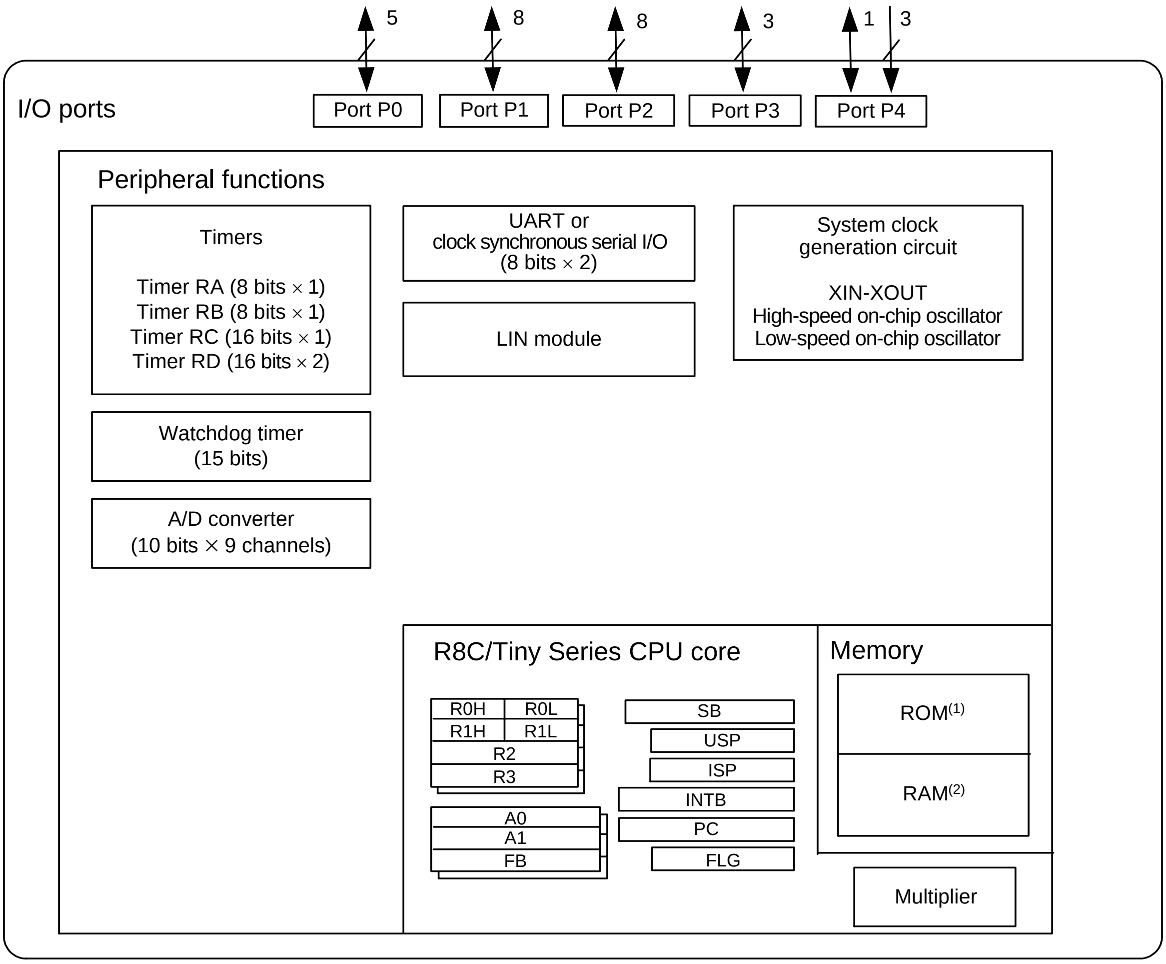
Table 1.2 Specifications for R8C/2K Group (2)

Item	Function	Specification
Serial Interface	UART0, UART2	Clock synchronous serial I/O/UART × 2
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 9 channels, includes sample and hold function
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V) (VCC = 2.7 to 5.5 V for A/D converter only)
Current consumption		Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 23 μA (VCC = 3.0 V, wait mode, low-speed on-chip oscillator used) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version)(1) -20 to 105°C (Y version)(2)
Package		32-pin LQFP • Package code: PLQP0032GB-A (previous code: 32P6U-A)

NOTES:
1. Specify the D version if D version functions are to be used.
2. Please contact Renesas Technology sales offices for the Y version.

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

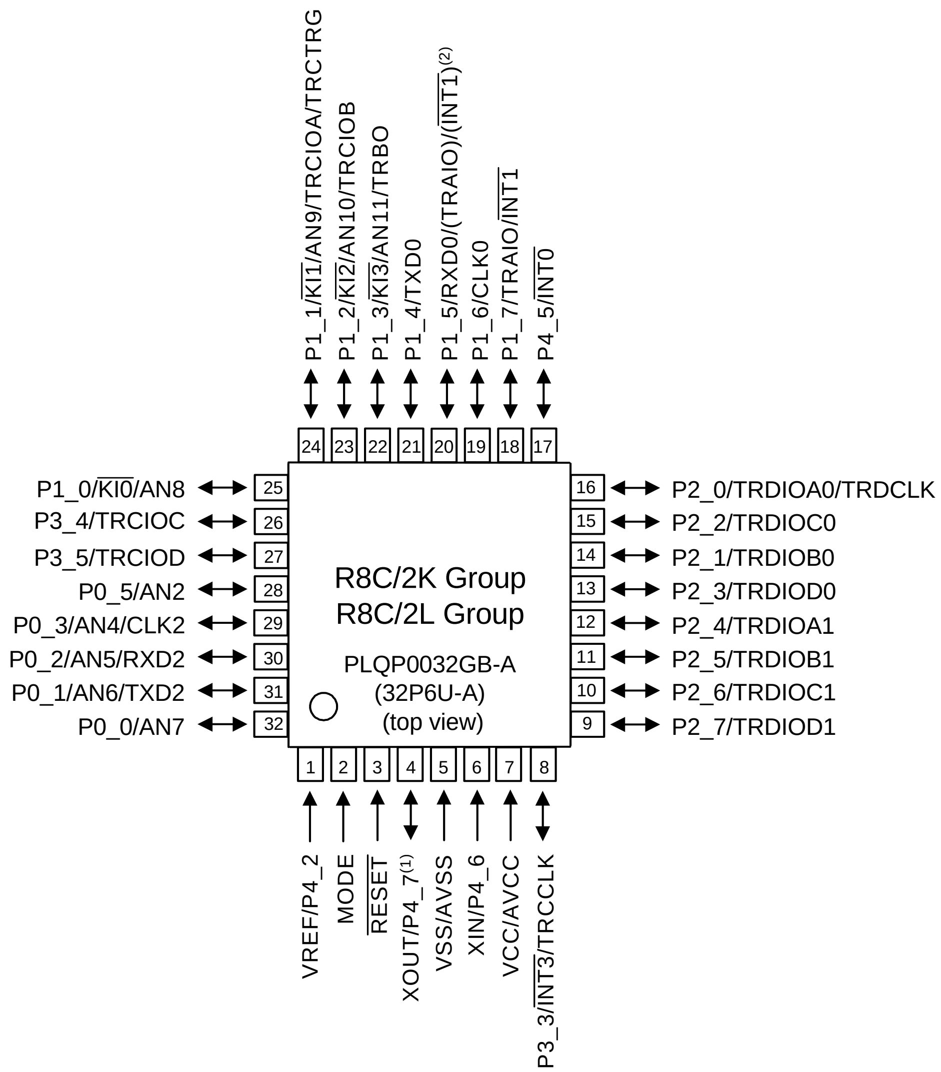


NOTES:
1. ROM size varies with MCU type.
2. RAM size varies with MCU type.

Figure 1.3 Block Diagram

1.4 Pin Assignment

Figure 1.4 shows the Pin Assignment (Top View). Table 1.7 outlines the Pin Name Information by Pin Number.



NOTES:
1. P4_7 are an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.4 Pin Assignment (Top View)

1.5 Pin Functions

Table 1.8 lists Pin Functions.

Table 1.8 Pin Functions

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins(1). To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RB, timer RC and timer RD input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD2	I	Serial data input pins
	TXD0, TXD2	O	Serial data output pins
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN2, AN4 to AN11	I	Analog input pins to A/D converter
I/O port	P0_0 to P0_3, P0_5, P1_0 to P1_7, P2_0 to P2_7, P3_3 to P3_5, P4_5,	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

NOTE:

1. Refer to the oscillator manufacturer for oscillation characteristics.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

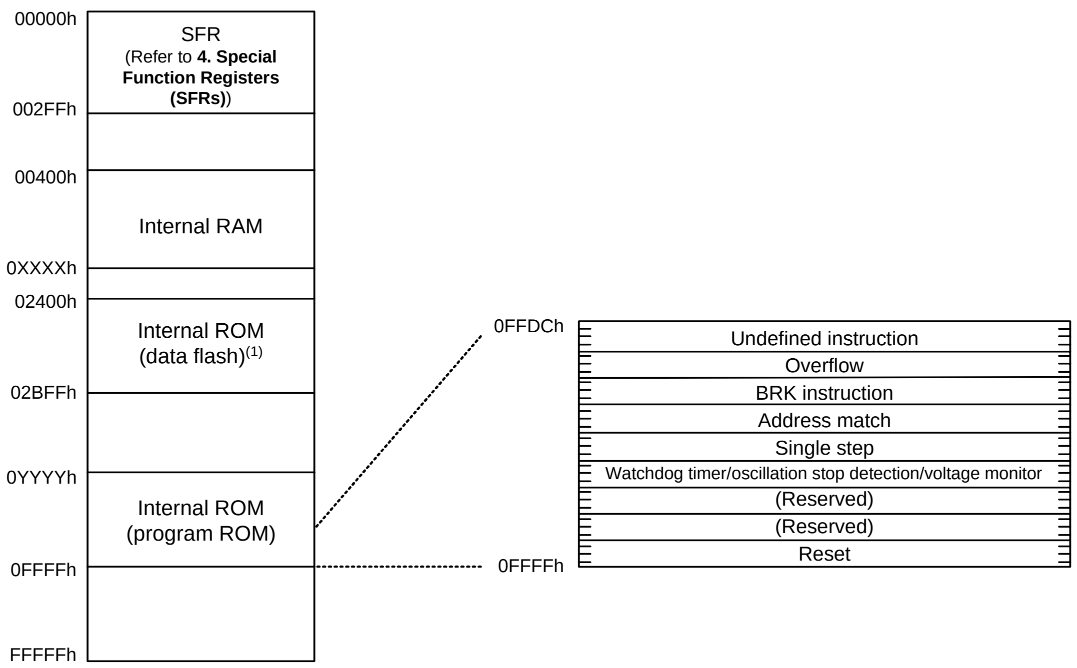
IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3.2 R8C/2L Group

Figure 3.2 is a Memory Map of R8C/2L Group. The R8C/2L Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1.5-Kbyte internal RAM is allocated addresses 00400h to 009FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F212L2SNFP, R5F212L2SDFP, R5F212L2SNXXXFP, R5F212L2SDXXXFP	8 Kbytes	0E000h	1 Kbyte	007FFh
R5F212L4SNFP, R5F212L4SDFP, R5F212L4SNXXXFP, R5F212L4SDXXXFP	16 Kbytes	0C000h	1.5 Kbytes	009FFh

Figure 3.2 Memory Map of R8C/2L Group

Table 4.7 SFR Information (7)[1]

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{CC}	Supply voltage			2.2	–	5.5	V
AV_{CC}	Supply voltage			2.7	–	5.5	
V_{SS}/AV_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	–160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$		–	–	–80	mA
$I_{OH(peak)}$	Peak output “H” current	Except P2_0 to P2_7		–	–	–10	mA
		P2_0 to P2_7		–	–	–40	mA
$I_{OH(avg)}$	Average output “H” current	Except P2_0 to P2_7		–	–	–5	mA
		P2_0 to P2_7		–	–	–20	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL(peak)}$		–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” currents	Sum of all pins $I_{OL(avg)}$		–	–	80	mA
$I_{OL(peak)}$	Peak output “L” currents	Except P2_0 to P2_7		–	–	10	mA
		P2_0 to P2_7		–	–	40	mA
$I_{OL(avg)}$	Average output “L” current	Except P2_0 to P2_7		–	–	5	mA
		P2_0 to P2_7		–	–	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V $\leq V_{CC} \leq$ 5.5 V	0	–	20	MHz
			2.7 V $\leq V_{CC} <$ 3.0 V	0	–	10	MHz
			2.2 V $\leq V_{CC} <$ 2.7 V	0	–	5	MHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V $\leq V_{CC} \leq$ 5.5 V	0	–	20	MHz
			2.7 V $\leq V_{CC} <$ 3.0 V	0	–	10	MHz
			2.2 V $\leq V_{CC} <$ 2.7 V	0	–	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V $\leq V_{CC} \leq$ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V $\leq V_{CC} \leq$ 5.5 V	–	–	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V $\leq V_{CC} \leq$ 5.5 V	–	–	5	MHz

NOTES:
1. V_{CC} = 2.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/2K Group	100(3)	–	–	times
		R8C/2L Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		–20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. –40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

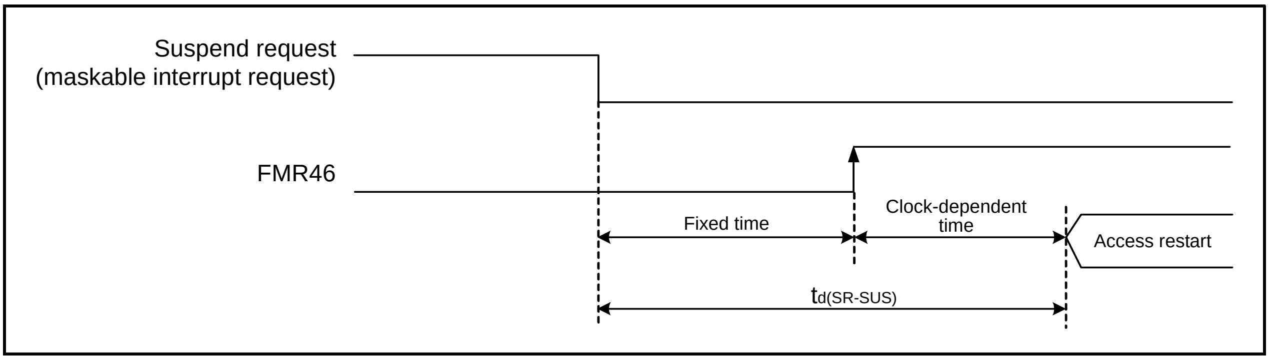


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level		2.2	2.3	2.4	V
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	0.9	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	300	µs
Vccmin	MCU operating voltage minimum value		2.2	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(4)		2.70	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

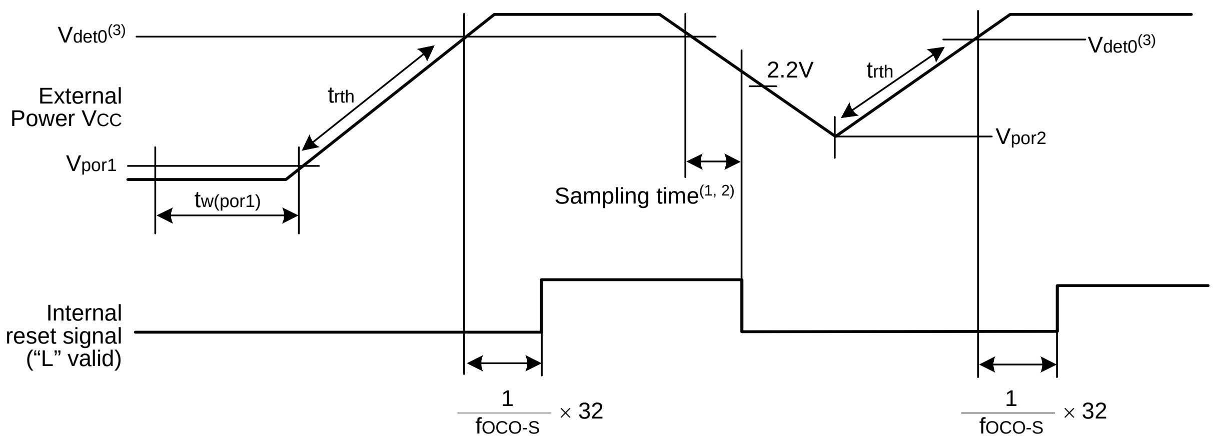
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V_{det0}	V
t_{rth}	External power V_{CC} rise gradient(2)		20	–	–	mV/msec

NOTES:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if $-20°C \leq T_{opr} \leq 85°C$, maintain $t_{w(por1)}$ for 3,000 s or more if $-40°C \leq T_{opr} < -20°C$.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 2.7 V to 5.5 V $-20°C \le T_{opr} \le 85°C$(2)	39.2	40	40.8	MHz
		V_{CC} = 2.7 V to 5.5 V $-40°C \le T_{opr} \le 85°C$(2)	39.0	40	41.0	MHz
		V_{CC} = 2.2 V to 5.5 V $-20°C \le T_{opr} \le 85°C$(3)	35.2	40	44.8	MHz
		V_{CC} = 2.2 V to 5.5 V $-40°C \le T_{opr} \le 85°C$(3)	34.0	40	46.0	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4)	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864	–	MHz
		V_{CC} = 2.7 V to 5.5 V $-20°C \le T_{opr} \le 85°C$	–3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	550	–	µA

NOTES:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.14 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA

Timing Requirements
(Unless Otherwise Specified: VCC = 5 V, VSS = 0 V at Topr = 25°C) [VCC = 5 V]

Table 5.16 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

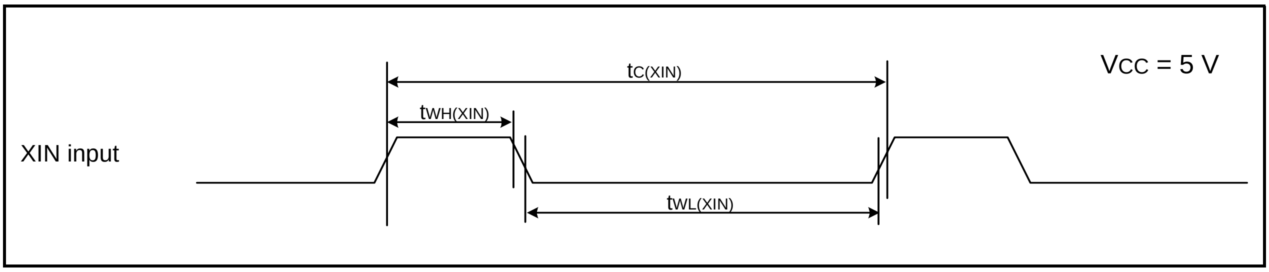


Figure 5.4 XIN Input Timing Diagram when VCC = 5 V

Table 5.17 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

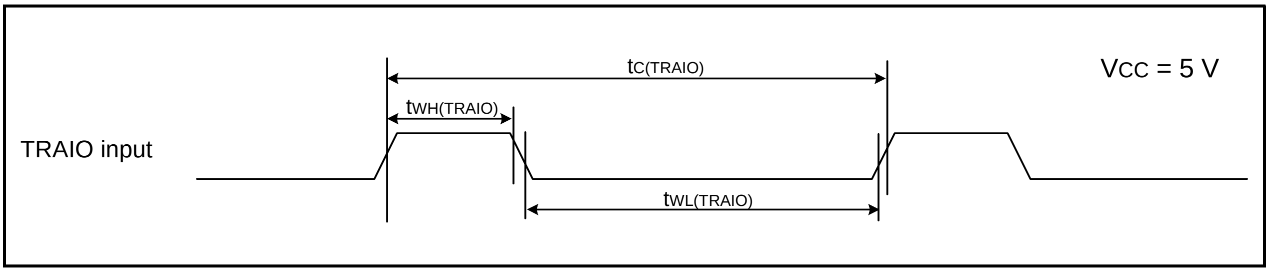


Figure 5.5 TRAIO Input Timing Diagram when VCC = 5 V

Table 5.21 Electrical Characteristics (2) [Vcc = 3 V]
(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	9	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	70	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	55	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

Timing requirements
(Unless Otherwise Specified: VCC = 3 V, VSS = 0 V at Topr = 25°C) [VCC = 3 V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input "H" width	40	–	ns
$t_{WL(XIN)}$	XIN input "L" width	40	–	ns

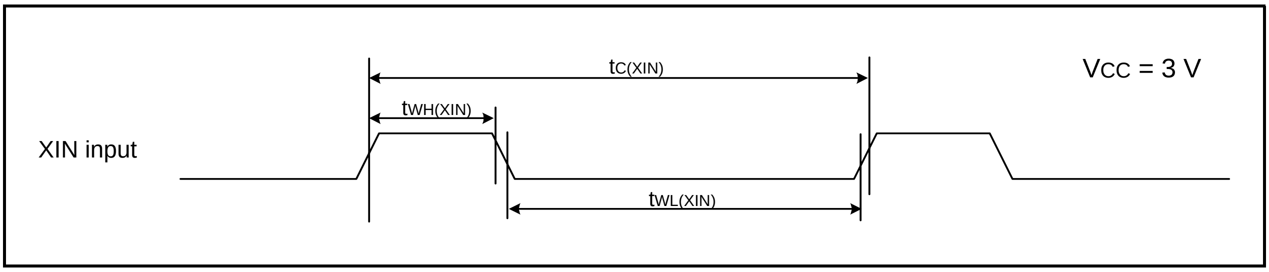


Figure 5.8 XIN Input Timing Diagram when VCC = 3 V

Table 5.23 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	120	–	ns

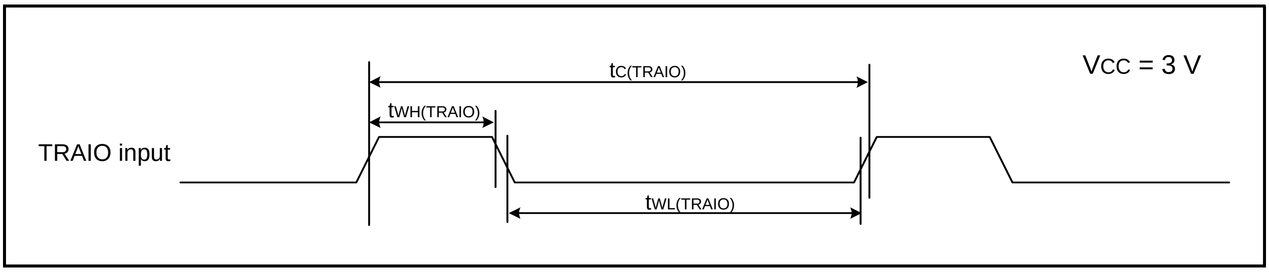


Figure 5.9 TRAIO Input Timing Diagram when VCC = 3 V

Table 5.26 Electrical Characteristics (1) [V_{CC} = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = –1 mA		V_{CC} – 0.5	–	V_{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = –2 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = –0.1 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = –50 μA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 2 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD2, CLK0, CLK2			0.05	0.3	–	V
		$\overline{RESET}$			0.05	0.15	–	V
I_{IH}	Input “H” current		VI = 2.2 V		–	–	4.0	μA
I_{IL}	Input “L” current		VI = 0 V		–	–	–4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V		100	200	600	kΩ
R_{fXIN}	Feedback resistance	XIN			–	5	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. V_{CC} = 2.2 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.27 Electrical Characteristics (2) [Vcc = 2.2 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

REVISION HISTORY	R8C/2K Group, R8C/2L Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Jul 20, 2007	–	First Edition issued
1.00	Nov 07, 2007	All pages	“Preliminary” deleted
		3, 5	Table 1.2, Table 1.4; Current consumption: “TBD” → “Typ. 10 mA” “Typ. 6 mA” “Typ. 2.0 μA” “Typ. 0.7 μA” revised
		6, 7	Table 1.5, Table 1.6 revised Figure 1.1, Figure 1.2; ROM number “XXX” added, NOTE1 added
		20	Table 4.4 “005Fh” “006Fh” “007Fh” “008Fh” added
		24	Table 5.2 NOTE2 revised
		32, 33	Table 5.14, Table 5.15 revised
		37, 41	Table 5.21, Table 5.27 revised
1.10	Dec 21, 2007	3, 5	Table 1.2, Table 1.4; revised, NOTE2 added
		6, 7	Figure 1.1, Figure 1.2; “Y: Operating ambient ....”, NOTE1 added
		15, 16	Figure 3.1, Figure 3.2; “Expanded area” deleted
		17	Table 4.1 “002Ch” added, “003Bh” “003Ch” “003Dh” deleted
		20	Table 4.4 “00D4h” “00D6h” revised
		22	Table 4.6 “0143h” revised
		24	5. “The electrical characteristics ....” added
		31	Table 5.10 Symbol “fOCO40M”: Parameter added, NOTE4 added