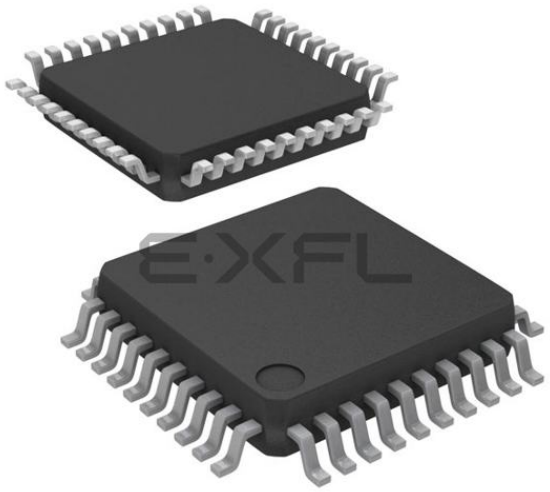

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | LINbus, SIO, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 25 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 5.5V |
| Data Converters | A/D 9x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212l2sdfp-v2 |

### 1.1.2 Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2K Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2L Group.

**Table 1.1 Specifications for R8C/2K Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C/Tiny series core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to **Table 1.5 Product List for R8C/2K Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 |
| I/O Ports | Programmable I/O ports | • Input-only: 3 pins<br>• CMOS I/O ports: 25, selectable pull-up resistor<br>• High current drive ports: 8 |
| Clock | Clock generation circuits | 2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),<br>On-chip oscillator (high-speed, low-speed)<br>(high-speed on-chip oscillator has a frequency adjustment function)<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • External: 4 sources, Internal: 15 sources, Software: 4 sources<br>• Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits × 2 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

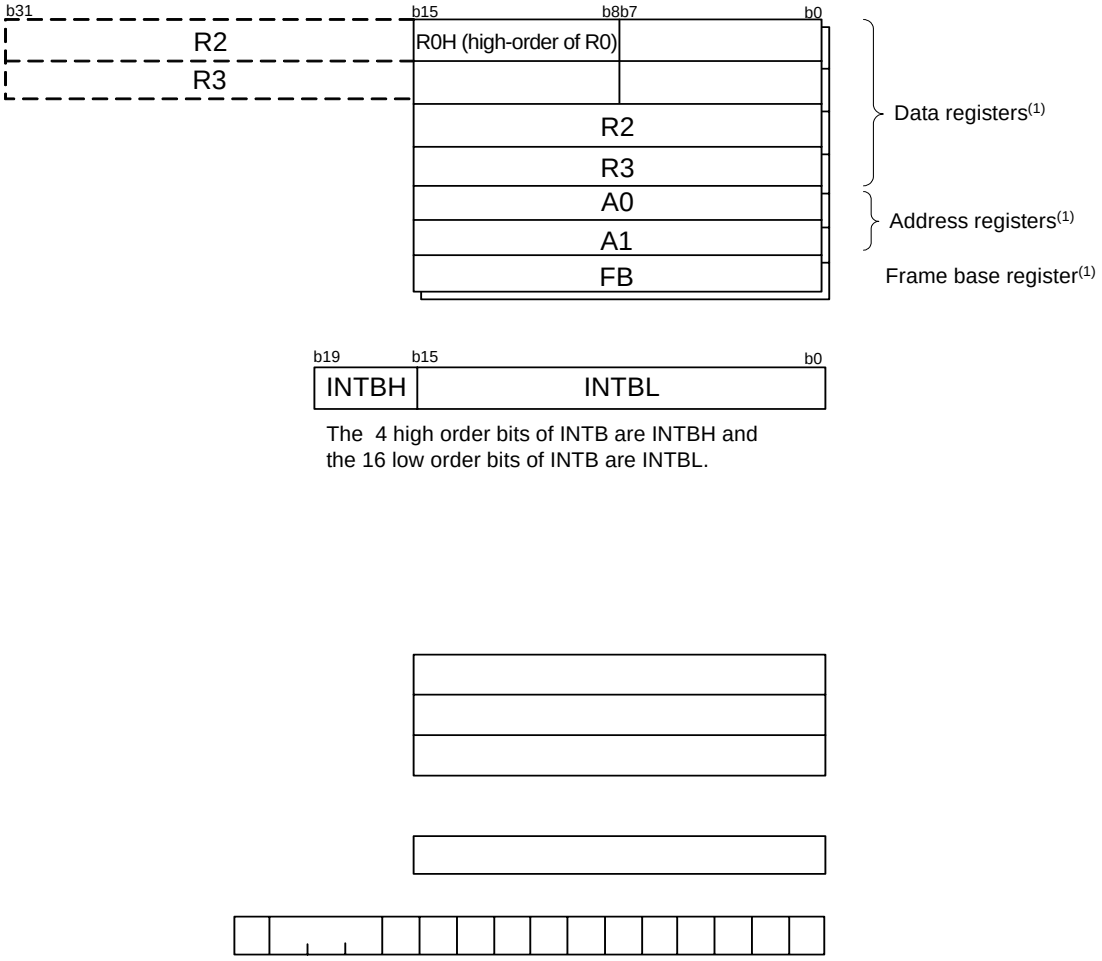



**Figure 2.1 CPU Registers**

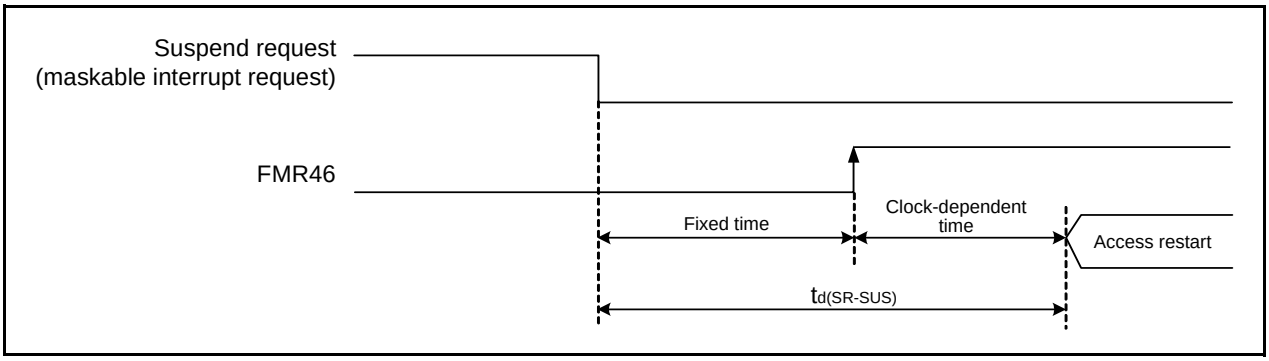



**Figure 5.2 Time delay until Suspend**

**Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det0}$ | Voltage detection level | | 2.2 | 2.3 | 2.4 | V |
| – | Voltage detection circuit self power consumption | VCA25 = 1, $V_{CC}$ = 5.0 V | – | 0.9 | – | μA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(2) | | – | – | 300 | μs |
| Vccmin | MCU operating voltage minimum value | | 2.2 | – | – | V |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

**Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level(4) | | 2.70 | 2.85 | 3.00 | V |
| – | Voltage monitor 1 interrupt request generation time(2) | | – | 40 | – | μs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | μA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | μs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes $V_{det1}$.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

**Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics**

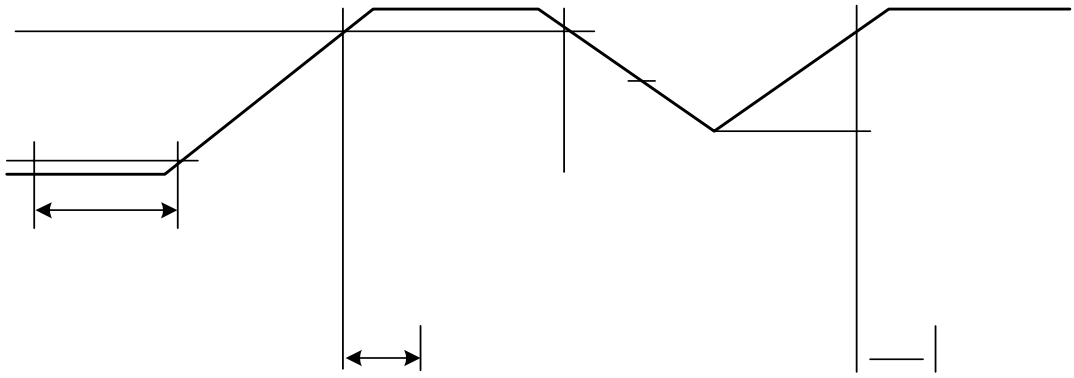
| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level | | 3.3 | 3.6 | 3.9 | V |
| – | Voltage monitor 2 interrupt request generation time(2) | | – | 40 | – | μs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | μA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | μs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{det2}$.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

**Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{por1}$ | Power-on reset valid voltage(4) | | – | – | 0.1 | V |
| $V_{por2}$ | Power-on reset or voltage monitor 0 reset valid voltage | | 0 | – | $V_{det0}$ | V |
| $t_{rth}$ | External power $V_{CC}$ rise gradient(2) | | 20 | – | – | mV/msec |

NOTES:
1. The measurement condition is $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This condition (external power $V_{CC}$ rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power $V_{CC}$ must be held below the effective voltage ($V_{por1}$) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if –20°C ≤ $T_{opr}$ ≤ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if –40°C ≤ $T_{opr}$ < –20°C.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. $V_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.

**Figure 5.3 Reset Circuit Electrical Characteristics**

### Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature • supply voltage dependence | $V_{CC}$ = 2.7 V to 5.5 V<br>–20°C ≤ $T_{opr}$ ≤ 85°C(2) | 39.2 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V<br>–40°C ≤ $T_{opr}$ ≤ 85°C(2) | 39.0 | 40 | 41.0 | MHz |
| | | $V_{CC}$ = 2.2 V to 5.5 V<br>–20°C ≤ $T_{opr}$ ≤ 85°C(3) | 35.2 | 40 | 44.8 | MHz |
| | | $V_{CC}$ = 2.2 V to 5.5 V<br>–40°C ≤ $T_{opr}$ ≤ 85°C(3) | 34.0 | 40 | 46.0 | MHz |
| | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4) | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 36.864 | – | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V<br>–20°C ≤ $T_{opr}$ ≤ 85°C | –3% | – | 3% | % |
| – | Value in FRA1 register after reset | | 08h | – | F7h | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to -1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 10 | 100 | μs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 550 | – | μA |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

### Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | μs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 15 | – | μA |

NOTE:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

### Table 5.12 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on(2) | | 1 | – | 2000 | μs |
| $t_{d(R-S)}$ | STOP exit time(3) | | – | – | 150 | μs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

**Table 5.13 Electrical Characteristics (1) [$V_{CC}$ = 5 V]**

| Symbol | Parameter | | Condition | Standard Min. | Standard Typ. | Standard Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output “H” voltage | Except P2_0 to P2_7, XOUT | $I_{OH}$ = –5 mA | $V_{CC}$ – 2.0 | – | $V_{CC}$ | V |
| | | | $I_{OH}$ = –200 μA | $V_{CC}$ – 0.5 | | | |

NOTE:
1. $V_{CC}$ = 4.2 to 5.5 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Timing Requirements**
**(Unless Otherwise Specified: $V_{CC}$ = 5 V, $V_{SS}$ = 0 V at $T_{opr}$ = 25°C) [$V_{CC}$ = 5 V]**

**Table 5.16 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 50 | – | ns |
| $t_{WH(XIN)}$ | XIN input "H" width | 25 | – | ns |
| $t_{WL(XIN)}$ | XIN input "L" width | 25 | – | ns |

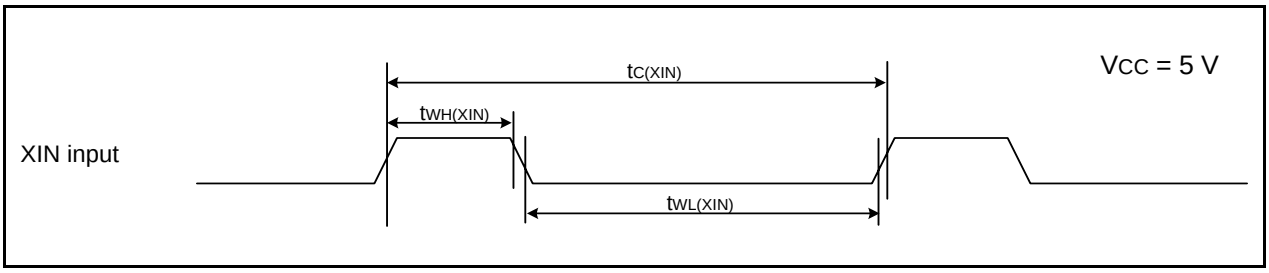



**Figure 5.4 XIN Input Timing Diagram when $V_{CC}$ = 5 V**

**Table 5.17 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input "H" width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input "L" width | 40 | – | ns |

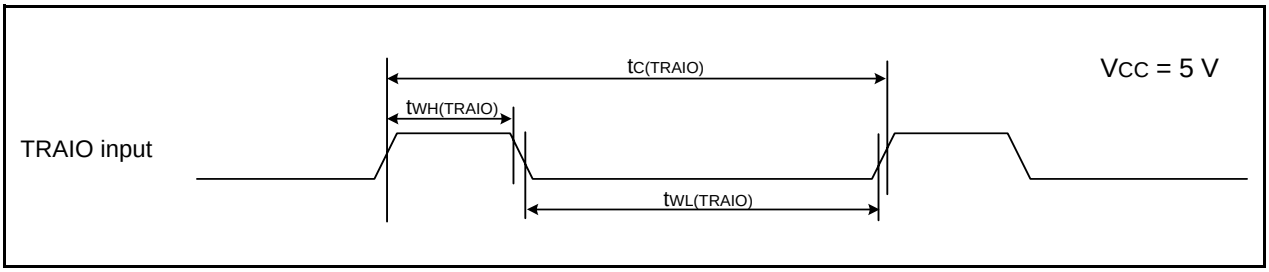



**Figure 5.5 TRAIO Input Timing Diagram when $V_{CC}$ = 5 V**

**Table 5.21 Electrical Characteristics (2) [Vcc = 3 V]**
**(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5 | 9 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 130 | 300 | μA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 25 | 70 | μA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 23 | 55 | μA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | μA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | μA |

**Table 5.26 Electrical Characteristics (1) [$V_{CC}$ = 2.2 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P2_0 to P2_7, XOUT | $I_{OH}$ = –1 mA | | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OH}$ = –2 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = –0.1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = –50 μA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Except P2_0 to P2_7, XOUT | $I_{OL}$ = 1 mA | | – | – | 0.5 | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OL}$ = 2 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 50 μA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD2, CLK0, CLK2 | | | 0.05 | 0.3 | – | V |
| | | $\overline{RESET}$ | | | 0.05 | 0.15 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 2.2 V | | – | – | 4.0 | μA |
| $I_{IL}$ | Input “L” current | | VI = 0 V | | – | – | –4.0 | μA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V | | 100 | 200 | 600 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 5 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:
1. $V_{CC}$ = 2.2 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

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