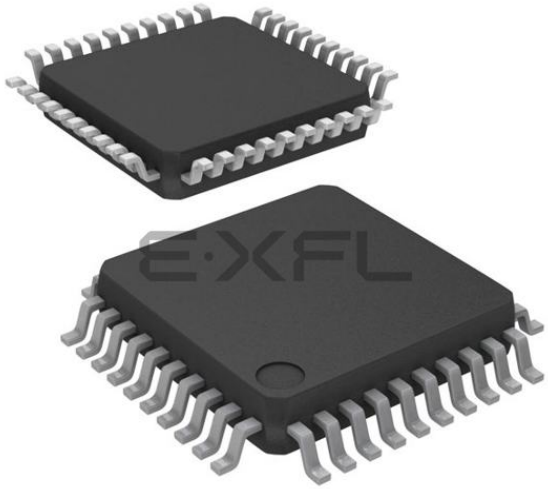
Renesas Electronics America Inc - R5F212L2SNFP#X6 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212l2snfp-x6

1.1.2 Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2K Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2L Group.

Table 1.1 Specifications for R8C/2K Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.5 Product List for R8C/2K Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3
I/O Ports	Programmable I/O ports	• Input-only: 3 pins • CMOS I/O ports: 25, selectable pull-up resistor • High current drive ports: 8
Clock	Clock generation circuits	2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function) • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• External: 4 sources, Internal: 15 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits × 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)

1.2 Product List

Table 1.5 lists the Product List for R8C/2K Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2K Group, Table 1.6 lists the Product List for R8C/2L Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2L Group.

Table 1.5 Product List for R8C/2K Group **Current of Dec. 2007**

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212K2SNFP	8 Kbytes	1 Kbyte	PLQP0032GB-A	N version
R5F212K4SNFP	16 Kbytes	1.5 Kbytes	PLQP0032GB-A	
R5F212K2SDFP	8 Kbytes	1 Kbyte	PLQP0032GB-A	D version
R5F212K4SDFP	16 Kbytes	1.5 Kbytes	PLQP0032GB-A	
R5F212K2SNXXXFP (D)	8 Kbytes	1 Kbyte	PLQP0032GB-A	N version Factory programming product(1)
R5F212K4SNXXXFP (D)	16 Kbytes	1.5 Kbytes	PLQP0032GB-A	
R5F212K2SDXXXFP (D)	8 Kbytes	1 Kbyte	PLQP0032GB-A	D version Factory programming product(1)
R5F212K4SDXXXFP (D)	16 Kbytes	1.5 Kbytes	PLQP0032GB-A	

(D): Under development
NOTE:
1. The user ROM is programmed before shipment.

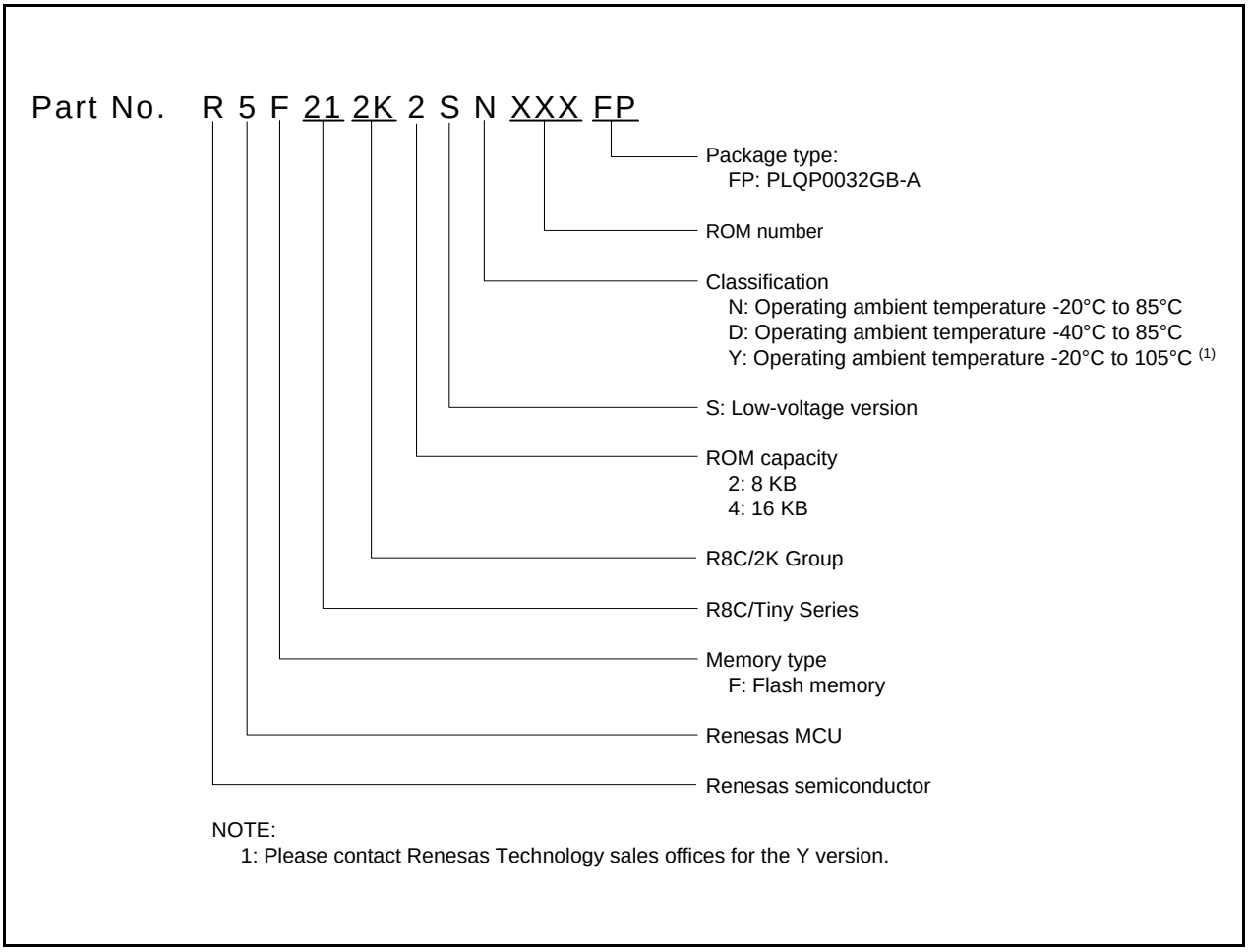


Figure 1.1 Part Number, Memory Size, and Package of R8C/2K Group

Table 1.6 Product List for R8C/2L Group **Current of Dec. 2007**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F212L2SNFP	8 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	N version
R5F212L4SNFP	16 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A	
R5F212L2SDFP	8 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	D version
R5F212L4SDFP	16 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A	
R5F212L2SNXXXFP (D)	8 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	N version Factory programming product(1)
R5F212L4SNXXXFP (D)	16 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A	
R5F212L2SDXXXFP (D)	8 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0032GB-A	D version Factory programming product(1)
R5F212L4SDXXXFP (D)	16 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A	

(D): Under development
NOTE:
1. The user ROM is programmed before shipment.

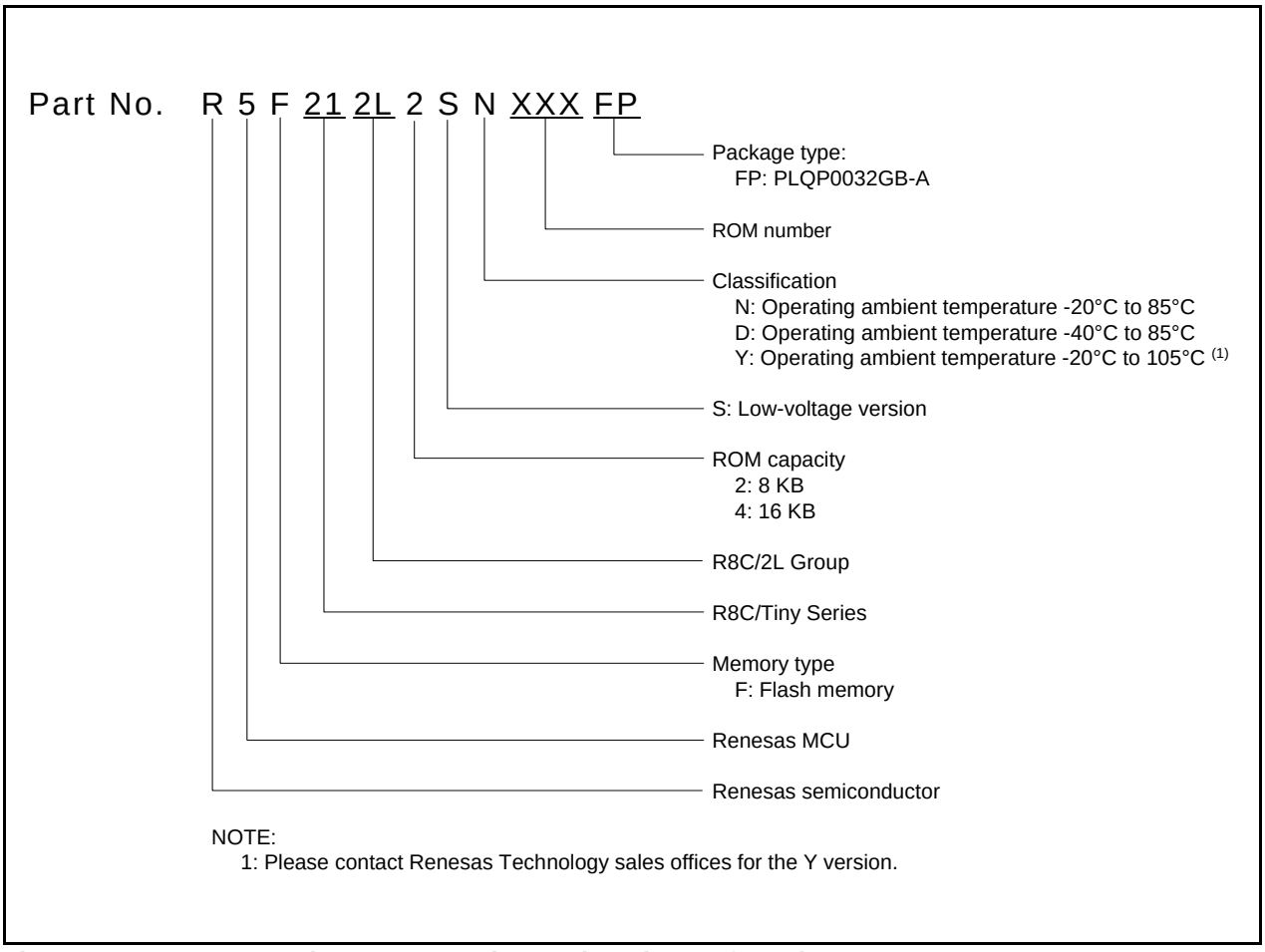


Figure 1.2 Part Number, Memory Size, and Package of R8C/2L Group

Table 1.7 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
			Interrupt	Timer	Serial Interface	A/D Converter
1	VREF	P4_2				
2	MODE					
3	$\overline{\text{RESET}}$					
4	XOUT	P4_7				
5	VSS/AVSS					
6	XIN	P4_6				
7	VCC/AVCC					
8		P3_3	$\overline{\text{INT3}}$	TRCCLK		
9		P2_7		TRDIOD1		
10		P2_6		TRDIOC1		
11		P2_5		TRDIOB1		
12		P2_4		TRDIOA1		
13		P2_3		TRDIOD0		
14		P2_1		TRDIOB0		
15		P2_2		TRDIOC0		
16		P2_0		TRDIOA0/TRDCLK		
17		P4_5	$\overline{\text{INT0}}$			
18		P1_7	$\overline{\text{INT1}}$	TRAIO		
19		P1_6			CLK0	
20		P1_5	($\overline{\text{INT1}}$)(1)	(TRAIO)(1)	RXD0	
21		P1_4			TXD0	
22		P1_3	$\overline{\text{KI3}}$	TRBO		AN11
23		P1_2	$\overline{\text{KI2}}$	TRCIOB		AN10
24		P1_1	$\overline{\text{KI1}}$	TRCIOA/TRCTRG		AN9
25		P1_0	$\overline{\text{KI0}}$			AN8
26		P3_4		TRCIOC		
27		P3_5		TRCIOD		
28		P0_5				AN2
29		P0_3			CLK2	AN4
30		P0_2			RXD2	AN5
31		P0_1			TXD2	AN6
32		P0_0				AN7

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

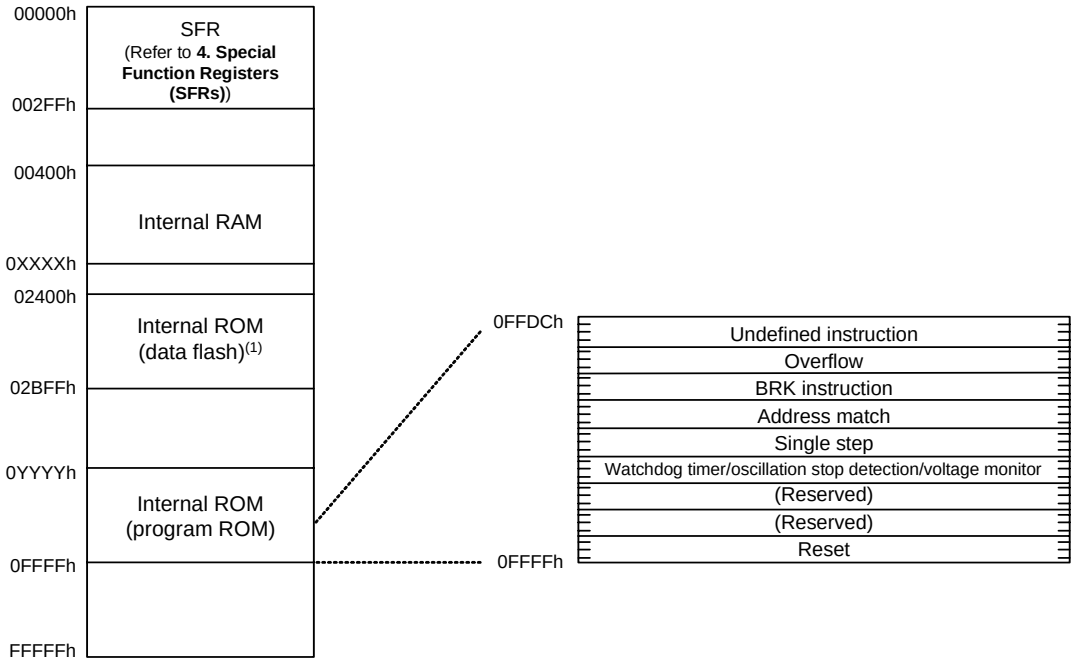
IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3.2 R8C/2L Group

Figure 3.2 is a Memory Map of R8C/2L Group. The R8C/2L Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1.5-Kbyte internal RAM is allocated addresses 00400h to 009FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F212L2SNFP, R5F212L2SDFP, R5F212L2SNXXXFP, R5F212L2SDXXXFP	8 Kbytes	0E000h	1 Kbyte	007FFh
R5F212L4SNFP, R5F212L4SDFP, R5F212L4SNXXXFP, R5F212L4SDXXXFP	16 Kbytes	0C000h	1.5 Kbytes	009FFh

Figure 3.2 Memory Map of R8C/2L Group

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah			
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.3 SFR Information (3)(1)

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.2	–	5.5	V
AV_{CC}	Supply voltage			2.7	–	5.5	
V_{SS}/AV_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	–160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$		–	–	–80	mA
$I_{OH(peak)}$	Peak output “H” current	Except P2_0 to P2_7		–	–	–10	mA
		P2_0 to P2_7		–	–	–40	mA
$I_{OH(avg)}$	Average output “H” current	Except P2_0 to P2_7		–	–	–5	mA
		P2_0 to P2_7		–	–	–20	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL(peak)}$		–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” currents	Sum of all pins $I_{OL(avg)}$		–	–	80	mA
$I_{OL(peak)}$	Peak output “L” currents	Except P2_0 to P2_7		–	–	10	mA
		P2_0 to P2_7		–	–	40	mA
$I_{OL(avg)}$	Average output “L” current	Except P2_0 to P2_7		–	–	5	mA
		P2_0 to P2_7		–	–	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V_{CC} ≤ 5.5 V	–	–	5	MHz

NOTES:
1. V_{CC} = 2.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/2K Group	100(3)	–	–	times
		R8C/2L Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		–20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. –40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

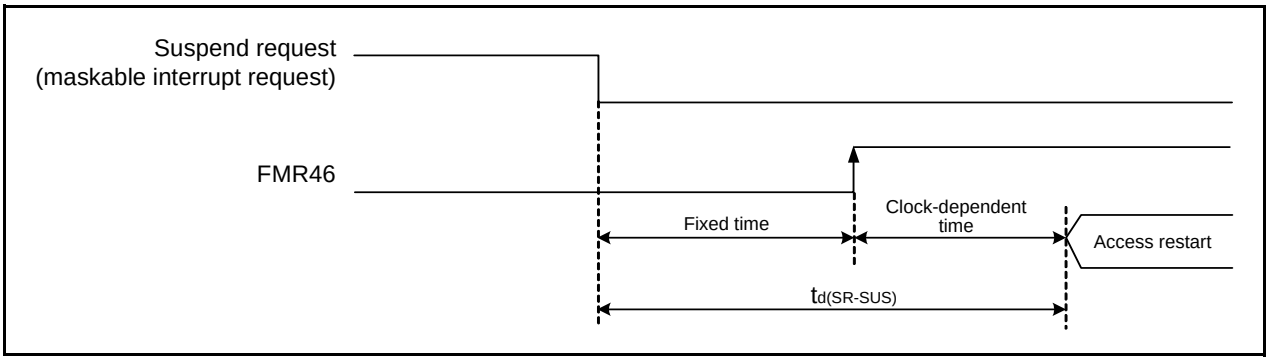


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level		2.2	2.3	2.4	V
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	0.9	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	300	µs
Vccmin	MCU operating voltage minimum value		2.2	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(4)		2.70	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 2.7 V to 5.5 V −20°C ≤ T_{opr} ≤ 85°C(2)	39.2	40	40.8	MHz
		V_{CC} = 2.7 V to 5.5 V −40°C ≤ T_{opr} ≤ 85°C(2)	39.0	40	41.0	MHz
		V_{CC} = 2.2 V to 5.5 V −20°C ≤ T_{opr} ≤ 85°C(3)	35.2	40	44.8	MHz
		V_{CC} = 2.2 V to 5.5 V −40°C ≤ T_{opr} ≤ 85°C(3)	34.0	40	46.0	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4)	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864	–	MHz
		V_{CC} = 2.7 V to 5.5 V −20°C ≤ T_{opr} ≤ 85°C	−3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	550	–	µA

NOTES:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.14 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA

Table 5.15 Electrical Characteristics (3) [Vcc = 5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V_{SS}	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
		Stop mode	XIN clock off, T_{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	µA
			XIN clock off, T_{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	µA

Timing Requirements
(Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 5 V]

Table 5.16 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

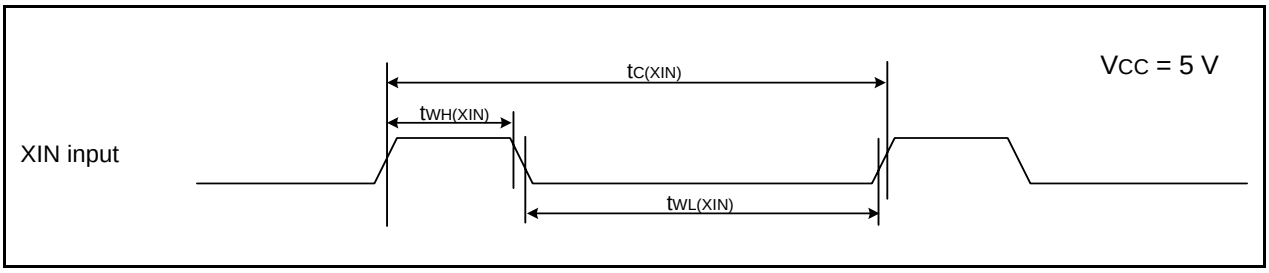


Figure 5.4 XIN Input Timing Diagram when V_{CC} = 5 V

Table 5.17 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

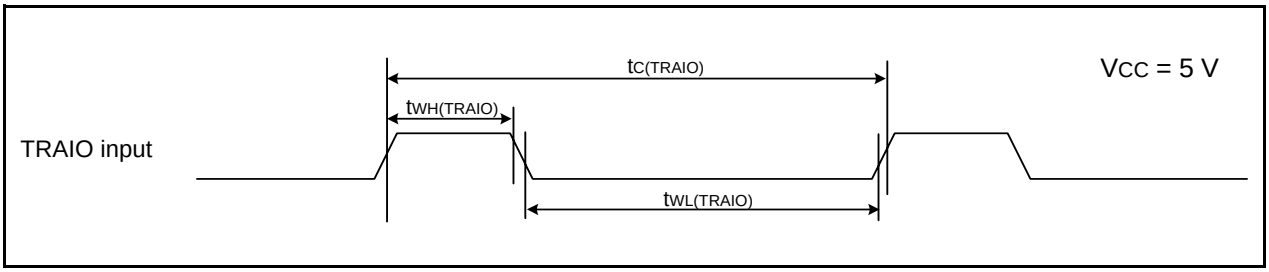


Figure 5.5 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 5.27 Electrical Characteristics (2) [Vcc = 2.2 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V_{SS}	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
		Stop mode	XIN clock off, T_{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, T_{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

Timing requirements
(Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 2.2 V]

Table 5.28 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns

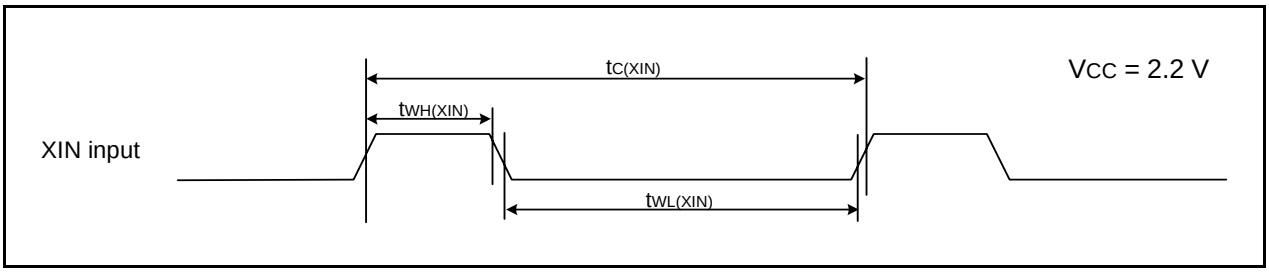


Figure 5.12 XIN Input Timing Diagram when V_{CC} = 2.2 V

Table 5.29 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

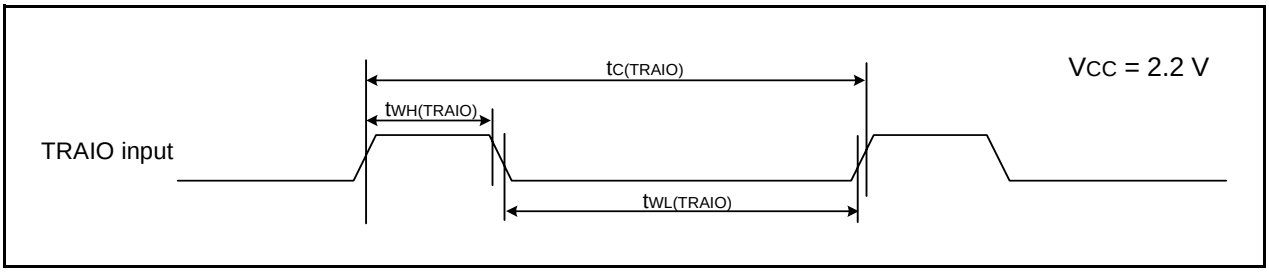


Figure 5.13 TRAIO Input Timing Diagram when V_{CC} = 2.2 V

REVISION HISTORY	R8C/2K Group, R8C/2L Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Jul 20, 2007	–	First Edition issued
1.00	Nov 07, 2007	All pages	“Preliminary” deleted
		3, 5	Table 1.2, Table 1.4; Current consumption: “TBD” → “Typ. 10 mA” “Typ. 6 mA” “Typ. 2.0 μA” “Typ. 0.7 μA” revised
		6, 7	Table 1.5, Table 1.6 revised Figure 1.1, Figure 1.2; ROM number “XXX” added, NOTE1 added
		20	Table 4.4 “005Fh” “006Fh” “007Fh” “008Fh” added
		24	Table 5.2 NOTE2 revised
		32, 33	Table 5.14, Table 5.15 revised
		37, 41	Table 5.21, Table 5.27 revised
1.10	Dec 21, 2007	3, 5	Table 1.2, Table 1.4; revised, NOTE2 added
		6, 7	Figure 1.1, Figure 1.2; “Y: Operating ambient ....”, NOTE1 added
		15, 16	Figure 3.1, Figure 3.2; “Expanded area” deleted
		17	Table 4.1 “002Ch” added, “003Bh” “003Ch” “003Dh” deleted
		20	Table 4.4 “00D4h” “00D6h” revised
		22	Table 4.6 “0143h” revised
		24	5. “The electrical characteristics ....” added
		31	Table 5.10 Symbol “fOCO40M”: Parameter added, NOTE4 added