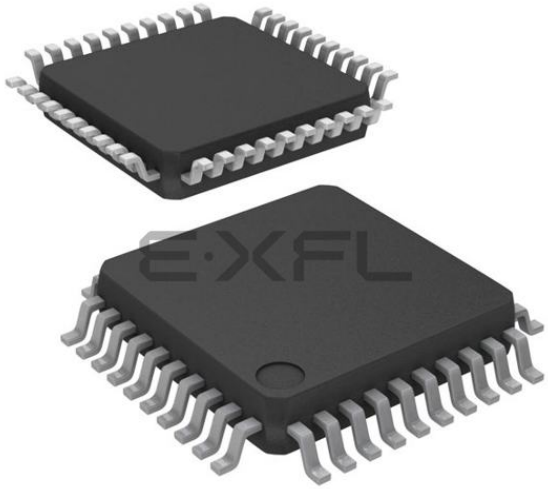
# Renesas Electronics America Inc - R5F212L4SNFP#X6 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | LINbus, SIO, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 25 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 5.5V |
| Data Converters | A/D 9x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212l4snfp-x6 |

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# 1. Overview

## 1.1 Features

The R8C/2K Group and R8C/2L Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.
Furthermore, the R8C/2L Group has on-chip data flash (1 KB × 2 blocks).
The difference between the R8C/2K Group and R8C/2L Group is only the presence or absence of data flash. Their peripheral functions are the same.

### 1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

### 1.1.2 Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2K Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2L Group.

**Table 1.1 Specifications for R8C/2K Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C/Tiny series core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to **Table 1.5 Product List for R8C/2K Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 |
| I/O Ports | Programmable I/O ports | • Input-only: 3 pins<br>• CMOS I/O ports: 25, selectable pull-up resistor<br>• High current drive ports: 8 |
| Clock | Clock generation circuits | 2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),<br>On-chip oscillator (high-speed, low-speed)<br>(high-speed on-chip oscillator has a frequency adjustment function)<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • External: 4 sources, Internal: 15 sources, Software: 4 sources<br>• Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits × 2 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |

**Table 1.3 Specifications for R8C/2L Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C/Tiny series core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to **Table 1.6 Product List for R8C/2L Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 |
| I/O Ports | Programmable I/O ports | • Input-only: 3 pins<br>• CMOS I/O ports: 25, selectable pull-up resistor<br>• High current drive ports: 8 |
| Clock | Clock generation circuits | 2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),<br>On-chip oscillator (high-speed, low-speed)<br>(high-speed on-chip oscillator has a frequency adjustment function)<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • External: 4 sources, Internal: 15 sources, Software: 4 sources<br>• Priority levels: 7 levels |
| Watchdog Timer | | 15 bits × 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits × 2 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |

**Table 1.4 Specifications for R8C/2L Group (2)**

| Item | Function | Specification |
|---|---|---|
| Serial Interface | UART0, UART2 | Clock synchronous serial I/O/UART × 2 |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| A/D Converter | | 10-bit resolution × 9 channels, includes sample and hold function |
| Flash Memory | | • Programming and erasure voltage: VCC = 2.7 to 5.5 V<br>• Programming and erasure endurance: 10,000 times (data flash)<br>1,000 times (program ROM)<br>• Program security: ROM code protect, ID code check<br>• Debug functions: On-chip debug, on-board flash rewrite function |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V)<br>f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V)<br>f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V) (VCC = 2.7 to 5.5 V for A/D converter only) |
| Current consumption | | Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz)<br>Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz)<br>Typ. 23 μA (VCC = 3.0 V, wait mode, low-speed on-chip oscillator used)<br>Typ. 0.7 μA (VCC = 3.0 V, stop mode) |
| Operating Ambient Temperature | | -20 to 85°C (N version)<br>-40 to 85°C (D version)(1)<br>-20 to 105°C (Y version)(2) |
| Package | | 32-pin LQFP<br>• Package code: PLQP0032GB-A (previous code: 32P6U-A) |

NOTES:
1. Specify the D version if D version functions are to be used.
2. Please contact Renesas Technology sales offices for the Y version.

## 1.5 Pin Functions

Table 1.8 lists Pin Functions.

**Table 1.8 Pin Functions**

| Item | Pin Name | I/O Type | Description |
|---|---|---|---|
| Power supply input | VCC, VSS | – | Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | – | Power supply for the A/D converter.<br>Connect a capacitor between AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Input “L” on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| XIN clock input | XIN | I | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins(1). To use an external clock, input it to the XIN pin and leave the XOUT pin open. |
| XIN clock output | XOUT | O | |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$ | I | $\overline{\text{INT}}$ interrupt input pins.<br>$\overline{\text{INT0}}$ is timer RB, timer RC and timer RD input pins. |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins |
| Timer RA | TRAIO | I/O | Timer RA I/O pin |
| Timer RB | TRBO | O | Timer RB output pin |
| Timer RC | TRCCLK | I | External clock input pin |
| | TRCTRG | I | External trigger input pin |
| | TRCIOA, TRCIOB, TRCIOC, TRCIOD | I/O | Timer RC I/O pins |
| Timer RD | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | I/O | Timer RD I/O pins |
| | TRDCLK | I | External clock input pin |
| Serial interface | CLK0, CLK2 | I/O | Transfer clock I/O pins |
| | RXD0, RXD2 | I | Serial data input pins |
| | TXD0, TXD2 | O | Serial data output pins |
| Reference voltage input | VREF | I | Reference voltage input pin to A/D converter |
| A/D converter | AN2, AN4 to AN11 | I | Analog input pins to A/D converter |
| I/O port | P0_0 to P0_3, P0_5, P1_0 to P1_7, P2_0 to P2_7, P3_3 to P3_5, P4_5, | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.<br>Any port set to input can be set to use a pull-up resistor or not by a program.<br>P2_0 to P2_7 also function as LED drive ports. |
| Input port | P4_2, P4_6, P4_7 | I | Input-only ports |

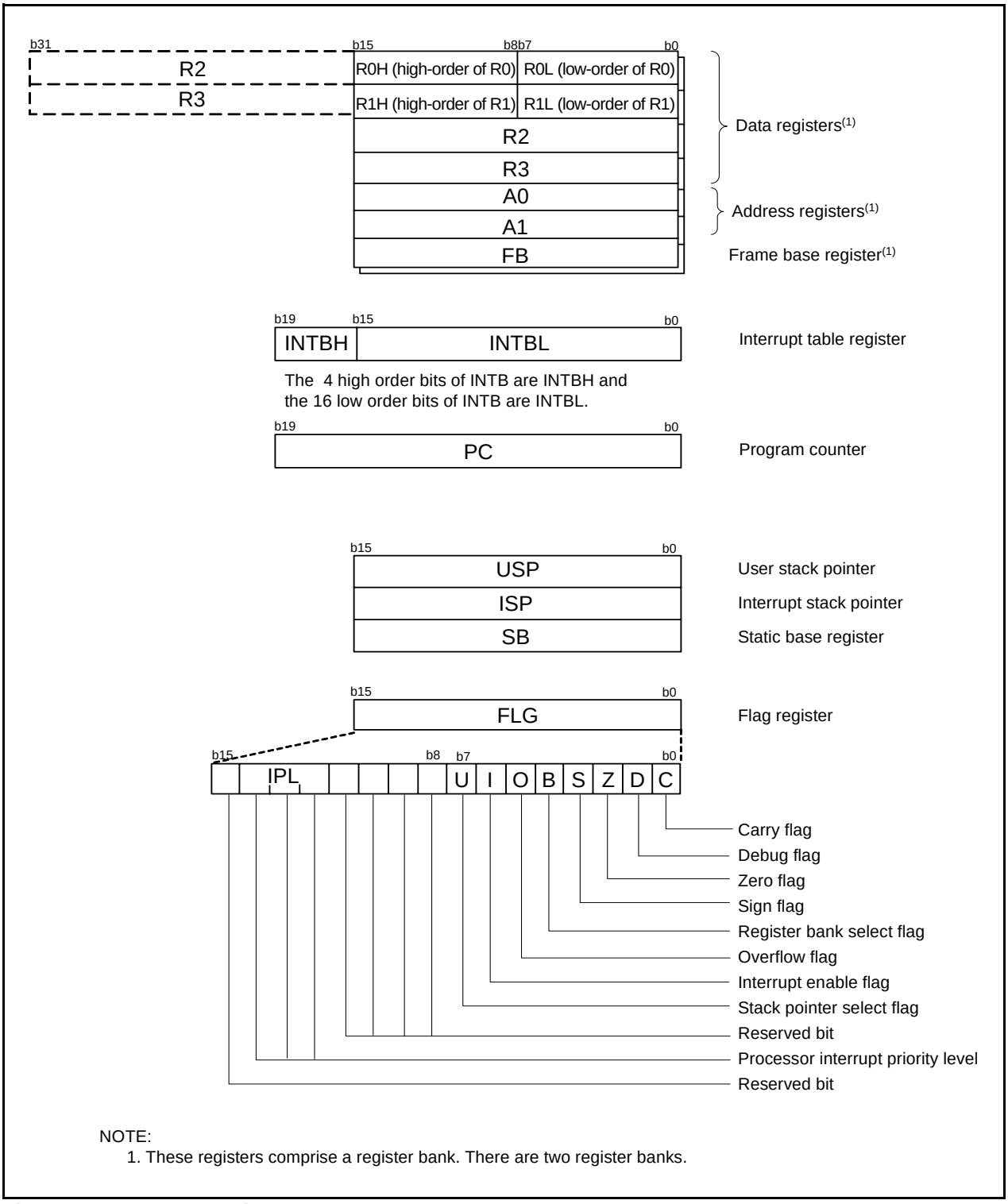
I: Input O: Output I/O: Input and output

NOTE:

1. Refer to the oscillator manufacturer for oscillation characteristics.

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.




NOTE:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 CPU Registers**

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

# 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

**Table 4.1 SFR Information (1)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 01101000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | | | |
| 0009h | | | |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | | | |
| 000Ch | Oscillation Stop Detection Register | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00X11111b |
| 0010h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0011h | | | 00h |
| 0012h | | | 00h |
| 0013h | Address Match Interrupt Enable Register | AIER | 00h |
| 0014h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0015h | | | 00h |
| 0016h | | | 00h |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h<br>10000000b[6] |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h | | | |
| 0021h | | | |
| 0022h | | | |
| 0023h | High-Speed On-Chip Oscillator Control Register 0 | FRA0 | 00h |
| 0024h | High-Speed On-Chip Oscillator Control Register 1 | FRA1 | When shipping |
| 0025h | High-Speed On-Chip Oscillator Control Register 2 | FRA2 | 00h |
| 0026h | | | |
| 0027h | | | |
| 0028h | | | |
| 0029h | | | |
| 002Ah | | | |
| 002Bh | High-Speed On-Chip Oscillator Control Register 6 | FRA6 | When Shipping |
| 002Ch | High-Speed On-Chip Oscillator Control Register 7 | FRA7 | When Shipping |
| 0030h | | | |
| 0031h | Voltage Detection Register 1[2] | VCA1 | 00001000b |
| 0032h | Voltage Detection Register 2[2] | VCA2 | 00h[3]<br>00100000b[4] |
| 0033h | | | |
| 0034h | | | |
| 0035h | | | |
| 0036h | Voltage Monitor 1 Circuit Control Register[5] | VW1C | 00001000b |
| 0037h | Voltage Monitor 2 Circuit Control Register[5] | VW2C | 00h |
| 0038h | Voltage Monitor 0 Circuit Control Register[2] | VW0C | 0000X000b[3]<br>0100X001b[4] |
| 0039h | | | |
| 003Ah | | | |
| 003Eh | | | |
| 003Fh | | | |

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

**Table 4.4 SFR Information (4)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 00C0h | A/D Register | AD | XXh |
| 00C1h | | | XXh |
| 00C2h | | | |
| 00C3h | | | |
| 00C4h | | | |
| 00C5h | | | |
| 00C6h | | | |
| 00C7h | | | |
| 00C8h | | | |
| 00C9h | | | |
| 00CAh | | | |
| 00CBh | | | |
| 00CCh | | | |
| 00CDh | | | |
| 00CEh | | | |
| 00CFh | | | |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Control Register 2 | ADCON2 | 00h |
| 00D5h | | | |
| 00D6h | A/D Control Register 0 | ADCON0 | 00h |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | XXh |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | Port P2 Register | P2 | XXh |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | Port P2 Direction Register | PD2 | 00h |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | | | |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | | | |
| 00ECh | | | |
| 00EDh | | | |
| 00EEh | | | |
| 00EFh | | | |
| 00F0h | | | |
| 00F1h | | | |
| 00F2h | | | |
| 00F3h | | | |
| 00F4h | Port P2 Drive Capacity Control Register | P2DRR | 00h |
| 00F5h | Pin Select Register 1 | PINSR1 | XXh |
| 00F6h | Pin Select Register 2 | PINSR2 | XXh |
| 00F7h | Pin Select Register 3 | PINSR3 | XXh |
| 00F8h | Port Mode Register | PMR | 00h |
| 00F9h | External Input Enable Register | INTEN | 00h |
| 00FAh | INT Input Filter Select Register | INTF | 00h |
| 00FBh | Key Input Enable Register | KIEN | 00h |
| 00FCh | Pull-Up Control Register 0 | PUR0 | 00h |
| 00FDh | Pull-Up Control Register 1 | PUR1 | XX000000b |
| 00FEh | | | |
| 00FFh | | | |

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

**Table 4.5 SFR Information (5)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0100h | Timer RA Control Register | TRACR | 00h |
| 0101h | Timer RA I/O Control Register | TRAIOC | 00h |
| 0102h | Timer RA Mode Register | TRAMR | 00h |
| 0103h | Timer RA Prescaler Register | TRAPRE | FFh |
| 0104h | Timer RA Register | TRA | FFh |
| 0105h | LIN Control Register 2 | LINCR2 | 00h |
| 0106h | LIN Control Register | LINCR | 00h |
| 0107h | LIN Status Register | LINST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | | | |
| 0111h | | | |
| 0112h | | | |
| 0113h | | | |
| 0114h | | | |
| 0115h | | | |
| 0116h | | | |
| 0117h | | | |
| 0118h | | | |
| 0119h | | | |
| 011Ah | | | |
| 011Bh | | | |
| 011Ch | | | |
| 011Dh | | | |
| 011Eh | | | |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011111b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | | | |
| 0134h | | | |
| 0135h | | | |
| 0136h | | | |
| 0137h | Timer RD Start Register | TRDSTR | 11111100b |
| 0138h | Timer RD Mode Register | TRDMR | 00001110b |
| 0139h | Timer RD PWM Mode Register | TRDPMR | 10001000b |
| 013Ah | Timer RD Function Control Register | TRDFCR | 10000000b |
| 013Bh | Timer RD Output Master Enable Register 1 | TRDOER1 | FFh |
| 013Ch | Timer RD Output Master Enable Register 2 | TRDOER2 | 01111111b |
| 013Dh | Timer RD Output Control Register | TRDOCR | 00h |
| 013Eh | Timer RD Digital Filter Function Select Register 0 | TRDDF0 | 00h |
| 013Fh | Timer RD Digital Filter Function Select Register 1 | TRDDF1 | 00h |

NOTE:
1. The blank regions are reserved. Do not access locations in these regions

# 5. Electrical Characteristics

The electrical characteristics of N version (Topr = –20°C to 85°C) and D version (Topr = –40°C to 85°C) are listed below.
Please contact Renesas Technology sales offices for the electrical characteristics in the Y version (Topr = –20°C to 105°C).

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | Condition | Rated Value | Unit |
|---|---|---|---|---|
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | –0.3 to 6.5 | V |
| $V_I$ | Input voltage | | –0.3 to $V_{CC}$ + 0.3 | V |
| $V_O$ | Output voltage | | –0.3 to $V_{CC}$ + 0.3 | V |
| $P_d$ | Power dissipation | $T_{opr}$ = 25°C | 500 | mW |
| $T_{opr}$ | Operating ambient temperature | | –20 to 85 (N version) / –40 to 85 (D version) | °C |
| $T_{stg}$ | Storage temperature | | –65 to 150 | °C |

**Table 5.3 A/D Converter Characteristics**

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref}$ = $AV_{CC}$ | – | – | 10 | Bits |
| – | Absolute accuracy | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±3 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | – | – | ±2 | LSB |
| | | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±5 | LSB |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 3.3 V | – | – | ±2 | LSB |
| $R_{ladder}$ | Resistor ladder | | $V_{ref}$ = $AV_{CC}$ | 10 | – | 40 | kΩ |
| $t_{conv}$ | Conversion time | 10-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 3.3 | – | – | µs |
| | | 8-bit mode | $\phi_{AD}$ = 10 MHz, $V_{ref}$ = $AV_{CC}$ = 5.0 V | 2.8 | – | – | µs |
| $V_{ref}$ | Reference voltage | | | 2.2 | – | $AV_{CC}$ | V |
| $V_{IA}$ | Analog input voltage(2) | | | 0 | – | $AV_{CC}$ | V |
| – | A/D operating clock frequency | Without sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 0.25 | – | 10 | MHz |
| | | With sample and hold | $V_{ref}$ = $AV_{CC}$ = 2.7 to 5.5 V | 1 | – | 10 | MHz |

NOTES:
1. $AV_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

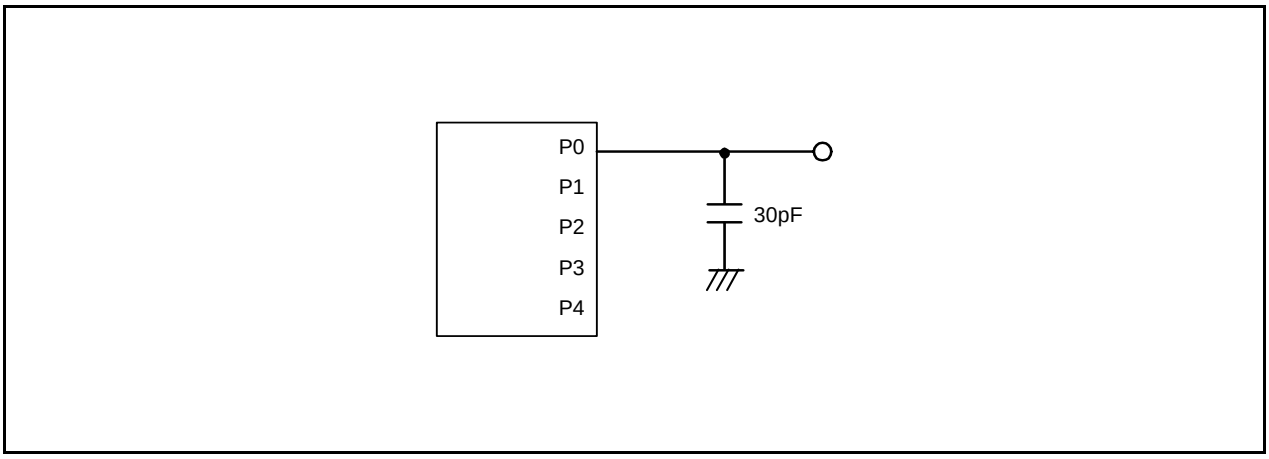
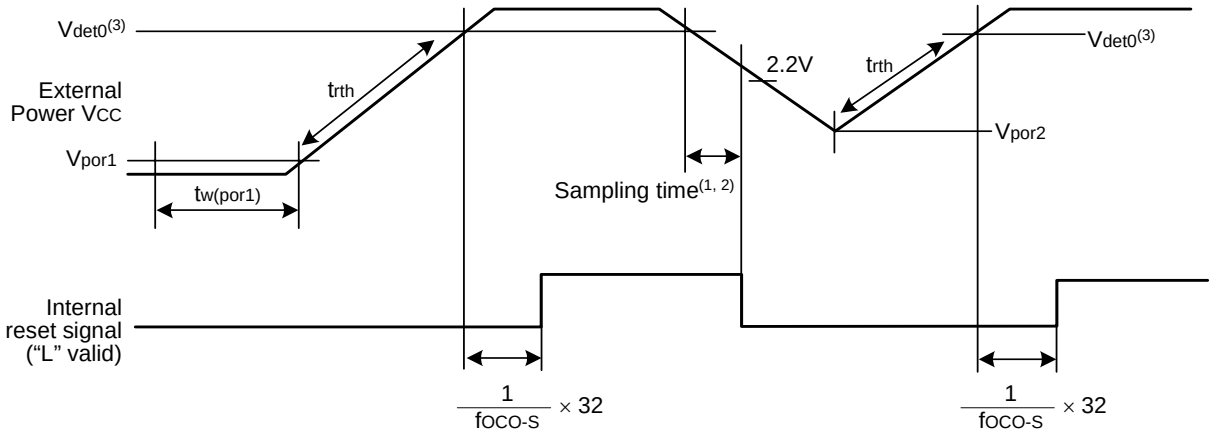



**Figure 5.1 Ports P0 to P4 Timing Measurement Circuit**

**Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{por1}$ | Power-on reset valid voltage(4) | | – | – | 0.1 | V |
| $V_{por2}$ | Power-on reset or voltage monitor 0 reset valid voltage | | 0 | – | $V_{det0}$ | V |
| $t_{rth}$ | External power $V_{CC}$ rise gradient(2) | | 20 | – | – | mV/msec |

NOTES:
1. The measurement condition is $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This condition (external power $V_{CC}$ rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power $V_{CC}$ must be held below the effective voltage ($V_{por1}$) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if –20°C ≤ $T_{opr}$ ≤ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if –40°C ≤ $T_{opr}$ < –20°C.




NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. $V_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.

**Figure 5.3 Reset Circuit Electrical Characteristics**

### Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature • supply voltage dependence | $V_{CC}$ = 2.7 V to 5.5 V<br>−20°C ≤ $T_{opr}$ ≤ 85°C(2) | 39.2 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V<br>−40°C ≤ $T_{opr}$ ≤ 85°C(2) | 39.0 | 40 | 41.0 | MHz |
| | | $V_{CC}$ = 2.2 V to 5.5 V<br>−20°C ≤ $T_{opr}$ ≤ 85°C(3) | 35.2 | 40 | 44.8 | MHz |
| | | $V_{CC}$ = 2.2 V to 5.5 V<br>−40°C ≤ $T_{opr}$ ≤ 85°C(3) | 34.0 | 40 | 46.0 | MHz |
| | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4) | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 36.864 | – | MHz |
| | | $V_{CC}$ = 2.7 V to 5.5 V<br>−20°C ≤ $T_{opr}$ ≤ 85°C | −3% | – | 3% | % |
| – | Value in FRA1 register after reset | | 08h | – | F7h | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to -1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 550 | – | µA |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

### Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 15 | – | µA |

NOTE:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.

### Table 5.12 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on(2) | | 1 | – | 2000 | µs |
| $t_{d(R-S)}$ | STOP exit time(3) | | – | – | 150 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

**Table 5.20 Electrical Characteristics (1) [Vcc = 3 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P2_0 to P2_7, XOUT | $I_{OH}$ = –1 mA | | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OH}$ = –5 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = –0.1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = –50 μA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Except P2_0 to P2_7, XOUT | $I_{OL}$ = 1 mA | | – | – | 0.5 | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | $I_{OL}$ = 5 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 50 μA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD2, CLK0, CLK2 | | | 0.1 | 0.3 | – | V |
| | | $\overline{RESET}$ | | | 0.1 | 0.4 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 3 V, $V_{CC}$ = 3 V | | – | – | 4.0 | μA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, $V_{CC}$ = 3 V | | – | – | –4.0 | μA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, $V_{CC}$ = 3 V | | 66 | 160 | 500 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 3.0 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:
1. $V_{CC}$ =2.7 to 3.3 V at $T_{opr}$ = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

**Table 5.21 Electrical Characteristics (2) [Vcc = 3 V]**
**(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5 | 9 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 130 | 300 | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 25 | 70 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 23 | 55 | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | µA |

**Timing requirements**
**(Unless Otherwise Specified: $V_{CC}$ = 3 V, $V_{SS}$ = 0 V at $T_{opr}$ = 25°C) [$V_{CC}$ = 3 V]**

**Table 5.22 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 100 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 40 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 40 | – | ns |

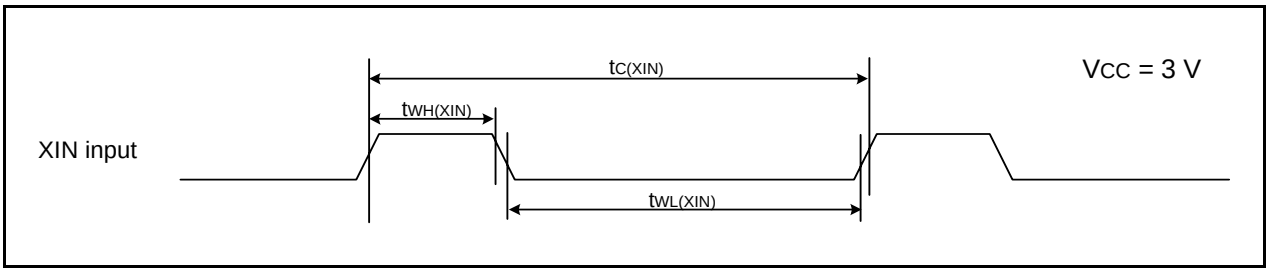



**Figure 5.8 XIN Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.23 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 300 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 120 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 120 | – | ns |

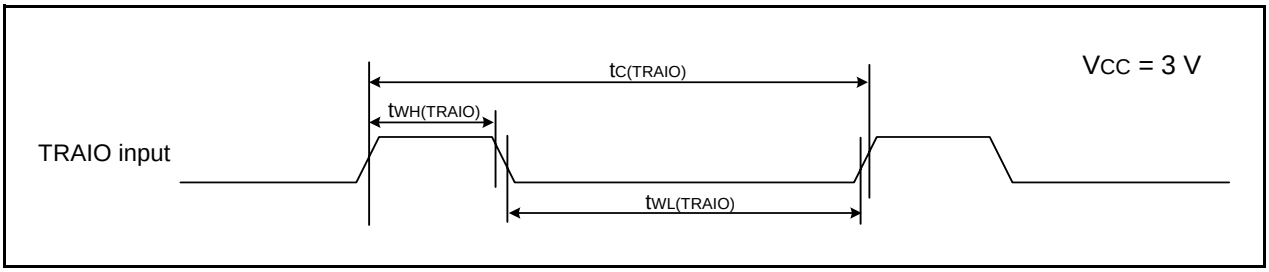



**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC}$ = 3 V**

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan



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**Renesas Technology America, Inc.**
450 Holger Way, San Jose, CA 95134-1368, U.S.A
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**Renesas Technology Europe Limited**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

**Renesas Technology Hong Kong Ltd.**
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

**Renesas Technology Taiwan Co., Ltd.**
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

**Renesas Technology Singapore Pte. Ltd.**
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510



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