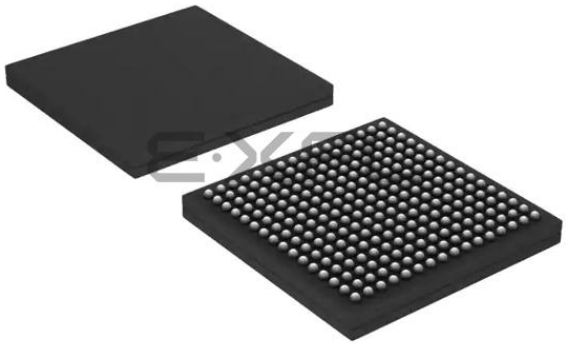

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Coldfire V2 |
| Core Size | 32-Bit Single-Core |
| Speed | 166MHz |
| Connectivity | EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB |
| Peripherals | DMA, WDT |
| Number of I/O | 69 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.4V ~ 1.6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-MAPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5274cvm166 |

In addition, the MCF5275 family features an enhanced multiply accumulate unit (EMAC), large on-chip memory (64 Kbytes SRAM, 16 Kbytes configurable cache), and a 16-bit DDR SDRAM memory controller.

These devices are ideal for cost-sensitive applications requiring significant control processing for file management, connectivity, data buffering, and user interface, as well as signal processing in a variety of key markets such as security, imaging, networking, gaming, and medical. This leading package of integration and high performance allows fast time to market through easy code reuse and extensive third party tool support.

To locate any published errata or updates for this document, refer to the ColdFire products website at http://www.freescale.com/coldfire.

# 1 MCF5275 Family Configurations

**Table 1. MCF5275 Family Configurations**

| Module | MCF5274L | MCF5275L | MCF5274 | MCF5275 |
|---|---|---|---|---|
| ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit) | • | • | • | • |
| System Clock | up to 166 MHz | | | |
| Performance (Dhrystone 2.1 MIPS) | up to 159 | | | |
| Instruction/Data Cache | 16 Kbytes (configurable) | | | |
| Static RAM (SRAM) | 64 Kbytes | | | |
| Interrupt Controllers (INTC) | 2 | 2 | 2 | 2 |
| Edge Port Module (EPORT) | • | • | • | • |
| External Interface Module (EIM) | • | • | • | • |
| 4-channel Direct-Memory Access (DMA) | • | • | • | • |
| DDR SDRAM Controller | • | • | • | • |
| Fast Ethernet Controller (FEC) | 1 | 1 | 2 | 2 |
| Watchdog Timer Module (WDT) | • | • | • | • |
| 4-channel Programmable Interval Timer Module (PIT) | • | • | • | • |
| 32-bit DMA Timers | 4 | 4 | 4 | 4 |
| USB | • | • | • | • |
| QSPI | • | • | • | • |
| UART(s) | 3 | 3 | 3 | 3 |
| $I^2C$ | • | • | • | • |
| PWM | 4 | 4 | 4 | 4 |
| General Purpose I/O Module (GPIO) | • | • | • | • |
| CIM = Chip Configuration Module + Reset Controller Module | • | • | • | • |
| Debug BDM | • | • | • | • |
| JTAG - IEEE 1149.1 Test Access Port | • | • | • | • |
| Hardware Encryption | — | • | — | • |
| Package | 196 MAPBGA | | 256 MAPBGA | |

# 2 Block Diagram

The superset device in the MCF5275 family comes in a 256 Mold Array Plastic Ball Grid Array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5275, the superset device.

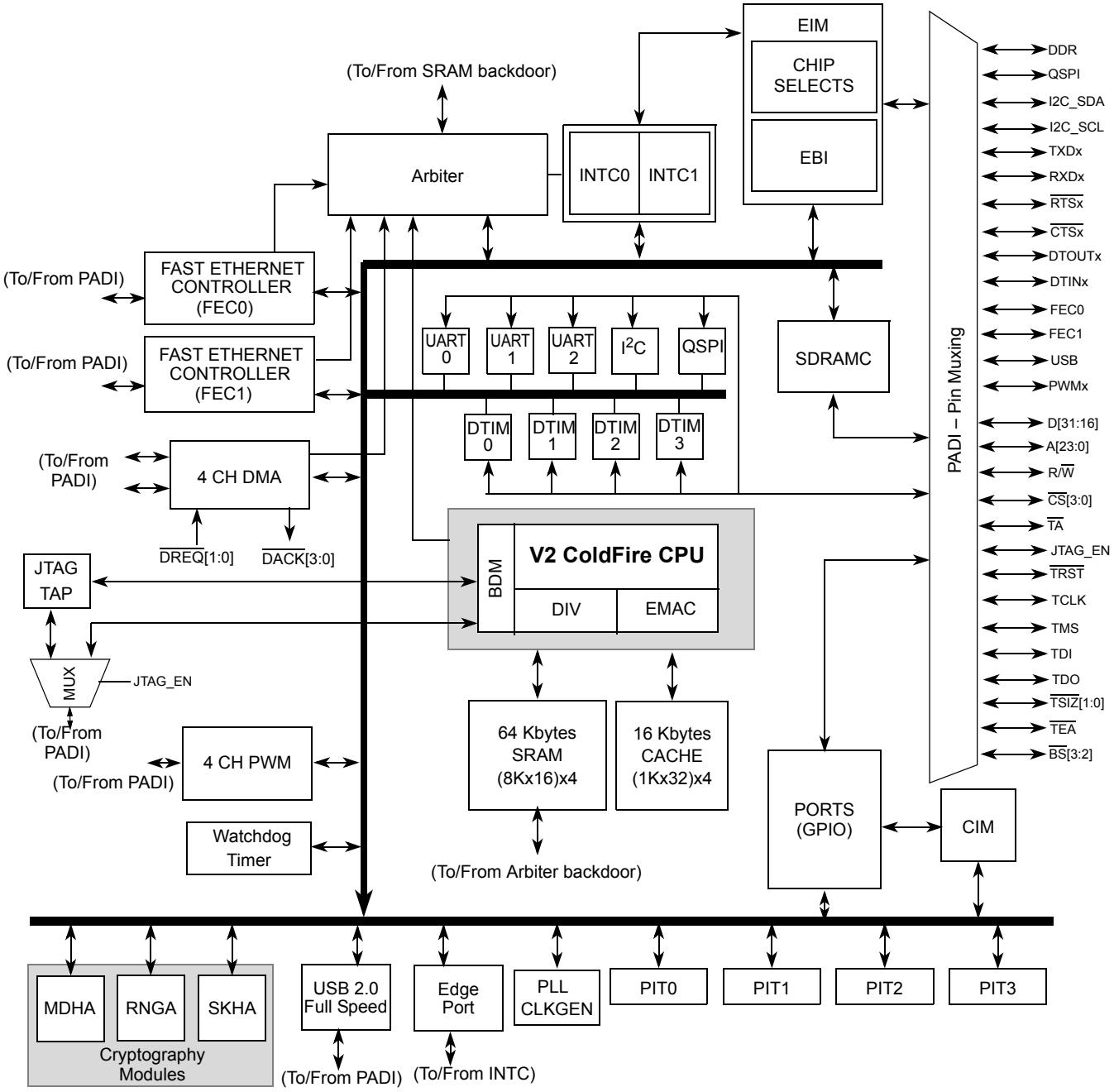



**Figure 1. MCF5275 Block Diagram**

# 3 Features

For a detailed feature list see the *MCF5275 Reference Manual* (MCF5275RM).

# 4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF5275 signals, consult the *MCF5275 Reference Manual* (MCF5275RM).

Table 2 lists the signals for the MCF5275 in functional group order. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts," for package diagrams.

**NOTE**

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

**NOTE**

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

**Table 2. MCF5274 and MCF5275 Signal Information and Muxing**

| Signal Name | GPIO | Alternate1 | Alternate2 | Dir.[1] | MCF5274 MCF5275 256 MAPBGA | MCF5274L MCF5275L 196 MAPBGA |
|---|---|---|---|---|---|---|
| **Reset** | | | | | | |
| $\overline{\text{RESET}}$ | — | — | — | I | N15 | K12 |
| $\overline{\text{RSTOUT}}$ | — | — | — | O | N14 | L12 |
| **Clock** | | | | | | |
| EXTAL | — | — | — | I | L16 | M14 |
| XTAL | — | — | — | O | M16 | N14 |
| CLKOUT | — | — | — | O | T12 | P9 |
| **Mode Selection** | | | | | | |
| CLKMOD[1:0] | — | — | — | I | N13, P13 | M11, N11 |
| $\overline{\text{RCON}}$ | — | — | — | I | P8 | M6 |
| **External Memory Interface and Ports** | | | | | | |
| A[23:21] | PADDR[7:5] | $\overline{\text{CS}}$[6:4] | — | O | A11, B11, C11 | A8, B8, C8 |
| A[20:0] | — | — | — | O | A12, B12, C12, A13, B13, C13, A14, B14, C14, B15, C15, B16, C16, D14, D15, E14:16, F14:16 | B9, D9, C9, C10, B10, A11, C11, B11, A12, D11, C12, B13, C13, D12, E11, D13, E12, F11, D14, E13, F13 |

**Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate1 | Alternate2 | Dir.[1] | MCF5274 MCF5275 256 MAPBGA | MCF5274L MCF5275L 196 MAPBGA |
|---|---|---|---|---|---|---|
| D[31:16] | — | — | — | O | M1, N1, N2, N3, P1, P2, R1, R2, P3, R3, T3, N4, P4, R4, T4, N5 | J3, L1, K2, K3, M1, L2, L3, L4, K4, J4, M2, N1, N2, M3, M4, N3 |
| $\overline{BS}$[3:2] | $\overline{PBS}$[3:2] | $\overline{CAS}$[3:2] | — | O | M3, R5 | K1, L5 |
| $\overline{OE}$ | PBUSCTL[7] | — | — | O | K1 | H4 |
| $\overline{TA}$ | PBUSCTL[6] | — | — | I | L13 | K14 |
| $\overline{TEA}$ | PBUSCTL[5] | $\overline{DREQ1}$ | — | I | T8 | — |
| R/$\overline{W}$ | PBUSCTL[4] | — | — | O | P7 | L6 |
| TSIZ1 | PBUSCTL[3] | DACK1 | — | O | D16 | B14 |
| TSIZ0 | PBUSCTL[2] | DACK0 | — | O | G16 | E14 |
| $\overline{TS}$ | PBUSCTL[1] | DACK2 | — | O | L4 | H2 |
| $\overline{TIP}$ | PBUSCTL[0] | $\overline{DREQ0}$ | — | O | P6 | — |
| **Chip Selects** | | | | | | |
| $\overline{CS}$[7:1] | PCS[7:1] | — | — | O | D10:13, E13, F13, N7 | D8, A9, A10, D10, B12, C14, P4 |
| $\overline{CS0}$ | — | — | — | O | R6 | N5 |
| **DDR SDRAM Controller** | | | | | | |
| DDR_CLKOUT | — | — | — | O | T7 | P6 |
| $\overline{DDR\_CLKOUT}$ | — | — | — | O | T6 | P5 |
| $\overline{SD\_CS}$[1:0] | PSDRAM[7:6] | $\overline{CS}$[3:2] | — | O | M2, T5 | H3, M5 |
| $\overline{SD\_SRAS}$ | PSDRAM[5] | — | — | O | L2 | H1 |
| $\overline{SD\_SCAS}$ | PSDRAM[4] | — | — | O | L1 | G3 |
| $\overline{SD\_WE}$ | PSDRAM[3] | — | — | O | K2 | G4 |
| SD_A10 | — | — | — | O | N6 | N4 |
| $\overline{SD\_DQS}$[3:2] | PSDRAM[2:1] | — | — | I/O | M4, P5 | J2, P3 |
| SD_CKE | PSDRAM[0] | — | — | O | L3 | J1 |
| SD_VREF | — | — | — | I | A15, T2 | A13, P2 |
| **External Interrupts Port** | | | | | | |
| $\overline{IRQ}$[7:5] | PIRQ[7:5] | — | — | I | G13, H16, H15 | F14, G13, G14 |
| $\overline{IRQ}$[4] | PIRQ[4] | $\overline{DREQ2}$ | — | I | H14 | H11 |
| $\overline{IRQ}$[3:2] | PIRQ[3:2] | $\overline{DREQ}$[3:2] | — | I | J14, J13 | H14, H12 |

**Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate1 | Alternate2 | Dir.[1] | MCF5274 MCF5275 256 MAPBGA | MCF5274L MCF5275L 196 MAPBGA |
|---|---|---|---|---|---|---|
| VSSPLL | — | — | — | I | K16 | L13 |
| VSS | — | — | — | I | A1, A10, A16, E5, E12, F6, F11, G7:10, H7:10, J1, J7:10, K7:10, L6, L11, M5, N16, R7, T1, T16 | F7, F8, G6:9, H6:9, J7, J8 |
| OVDD | — | — | — | I | E6:8, F5, F7, F8, G5, G6, H5, H6, J11, J12, K11, K12, L9, L10, L12, M9:11 | E5:7, F5, F6, H10, J9, J10, K8:10 |
| VDD | — | — | — | I | D8, H13, K4, N8 | D6, G5, G12, L7 |
| SD_VDD | — | — | — | I | E9:11, F9, F10, F12, G11, G12, H11, H12, J5, J6, K5, K6, L5, L7, L8, M6, M7, M8 | E8:10, F9, F10, G10, H5, J5, J6, K5:7 |

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

# 5 Design Recommendations

## 5.1 Layout

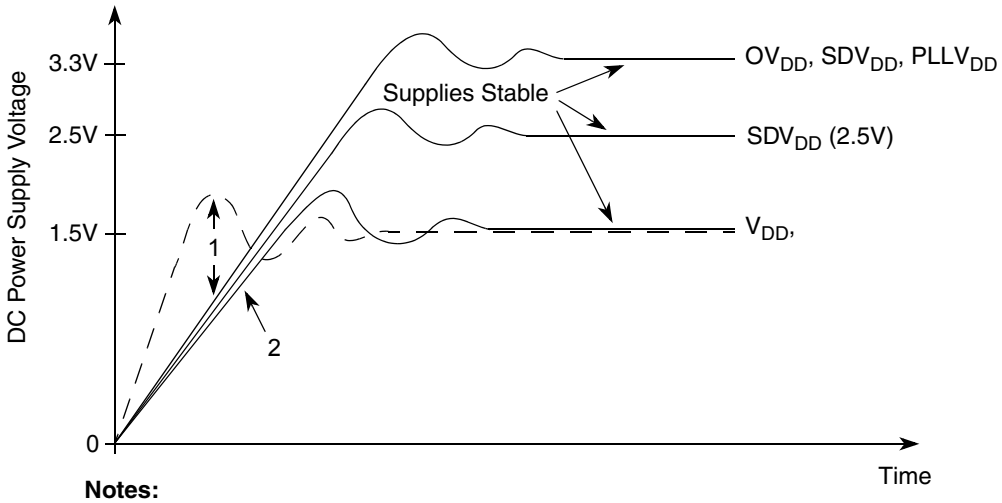
- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5275.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

## 5.2 Power Supply

- 33uF, 0.1 µF, and 0.01 µF across each power supply

### 5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O $V_{DD}$ ($OV_{DD}$), SDRAM $V_{DD}$ ($SDV_{DD}$), PLL $V_{DD}$ ($PLLV_{DD}$), and Core $V_{DD}$ ($V_{DD}$).




**Notes:**
1. VDD should not exceed OVDD, SDVDD or PLLVDD by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/SDVDD/PLLVDD up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, SDVDD, VDD, or PLLVDD) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

**Figure 2. Supply Voltage Sequencing and Separation Cautions**

The relationship between $SDV_{DD}$ and $OV_{DD}$ is non-critical during power-up and power-down sequences. $SDV_{DD}$ (2.5V or 3.3V) and $OV_{DD}$ are specified relative to $V_{DD}$.

#### 5.2.1.1 Power Up Sequence

If $OV_{DD}$/$SDV_{DD}$ are powered up with $V_{DD}$ at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the $OV_{DD}$/$SDV_{DD}$ to be in a high impedance state. There is no limit on how long after $OV_{DD}$/$SDV_{DD}$ powers up before $V_{DD}$ must powered up. $V_{DD}$ should not lead the $OV_{DD}$, $SDV_{DD}$, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or high current will be in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 µs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 µs or slower rise time for all supplies.
2. $V_{DD}$/$PLLV_{DD}$ and $OV_{DD}$/$SDV_{DD}$ should track up to 0.9 V, then separate for the completion of ramps with $OV_{DD}$/SD $V_{DD}$ going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

#### 5.2.1.2 Power Down Sequence

If $V_{DD}$ is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after $V_{DD}$ powers down before $OV_{DD}$, $SDV_{DD}$, or $PLLV_{DD}$ must power down. $V_{DD}$ should not lag $OV_{DD}$, $SDV_{DD}$, or $PLLV_{DD}$ going low by more than 0.4 V during power down or undesired high current will be in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop $V_{DD}$ to 0 V.
2. Drop $OV_{DD}$/$SDV_{DD}$/$PLLV_{DD}$ supplies.

## 5.3 Decoupling

- Place the decoupling capacitors as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 µF and 0.01 µF at each supply input

## 5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See electricals.

## 5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

## 5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

# 6 Mechanicals/Pinouts

## 6.1 256 MAPBGA Pinout

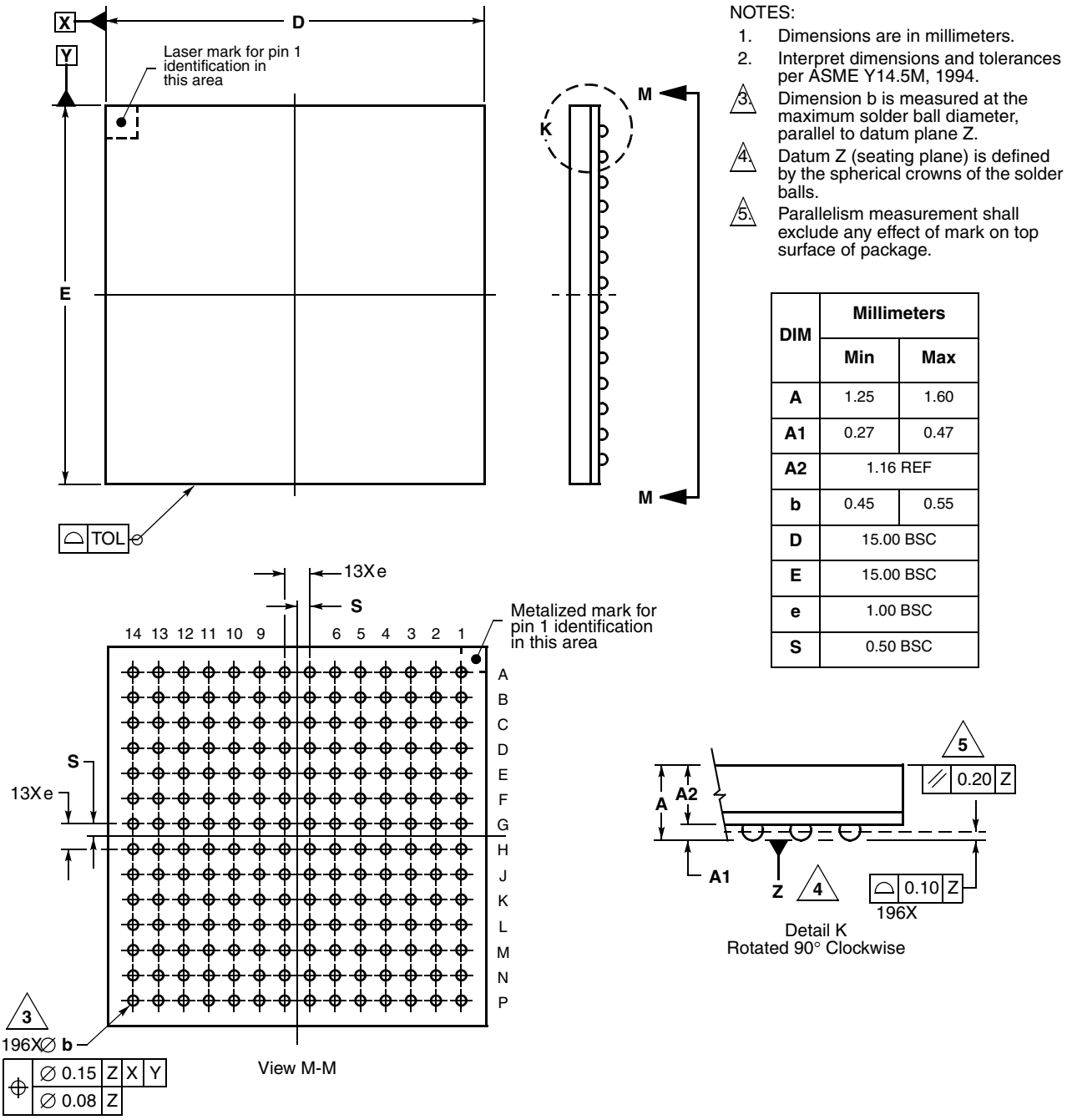
Figure 3 is a consolidated MCF5274/75 pinout for the 256 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | FEC1_ RXD1 | FEC1_ RXDV | FEC1_ CRS | FEC1_ COL | FEC0_ COL | FEC0_ MDIO | U0RXD | U1RXD | VSS | A23 | A20 | A17 | A14 | SD_ VREF | VSS | A |
| B | FEC1_ RXD3 | FEC1_ RXD2 | FEC1_ RXD0 | FEC1_ RXCLK | FEC0_ RXDV | FEC0_ RXCLK | FEC0_ MDC | U0TXD | U1TXD | I2C_ SDA | A22 | A19 | A16 | A13 | A11 | A9 | B |
| C | FEC1_ TXCLK | FEC1_ RXER | FEC0_ TXCLK | FEC0_ RXER | FEC0_ RXD2 | FEC0_ RXD0 | FEC0_ CRS | $\overline{\text{U0CTS}}$ | $\overline{\text{U1CTS}}$ | I2C_ SCL | A21 | A18 | A15 | A12 | A10 | A8 | C |
| D | FEC1_ TXER | FEC1_ TXEN | FEC0_ TXER | FEC0_ TXEN | FEC0_ RXD3 | FEC0_ RXD1 | $\overline{\text{U0RTS}}$ | VDD | $\overline{\text{U1RTS}}$ | $\overline{\text{CS7}}$ | $\overline{\text{CS6}}$ | $\overline{\text{CS5}}$ | $\overline{\text{CS4}}$ | A7 | A6 | TSIZ1 | D |
| E | FEC1_ TXD3 | FEC1_ TXD2 | FEC0_ TXD3 | NC | VSS | OVDD | OVDD | OVDD | SD_VDD | SD_VDD | SD_VDD | VSS | $\overline{\text{CS3}}$ | A5 | A4 | A3 | E |
| F | FEC1_ TXD0 | FEC1_ TXD1 | FEC0_ TXD2 | FEC0_ TXD1 | OVDD | VSS | OVDD | OVDD | SD_VDD | SD_VDD | VSS | SD_VDD | $\overline{\text{CS2}}$ | A2 | A1 | A0 | F |
| G | FEC1_ MDIO | FEC1_ MDC | DT0OUT | FEC0_ TXD0 | OVDD | OVDD | VSS | VSS | VSS | VSS | SD_VDD | SD_VDD | $\overline{\text{IRQ7}}$ | USB_ SPEED | USB_ CLK | TSIZ0 | G |
| H | DT1IN | DT1OUT | DT0IN | NC | OVDD | OVDD | VSS | VSS | VSS | VSS | SD_VDD | SD_VDD | VDD | $\overline{\text{IRQ4}}$ | $\overline{\text{IRQ5}}$ | $\overline{\text{IRQ6}}$ | H |
| J | VSS | DT2IN | DT2OUT | DT3IN | SD_VDD | SD_VDD | VSS | VSS | VSS | VSS | OVDD | OVDD | $\overline{\text{IRQ2}}$ | $\overline{\text{IRQ3}}$ | USB_RP | USB_RN | J |
| K | $\overline{\text{OE}}$ | $\overline{\text{SD_WE}}$ | DT3OUT | VDD | SD_VDD | SD_VDD | VSS | VSS | VSS | VSS | OVDD | OVDD | $\overline{\text{IRQ1}}$ | USB_TN | USB_TP | VSSPLL | K |
| L | $\overline{\text{SD_ SCAS}}$ | $\overline{\text{SD_ SRAS}}$ | SD_CKE | $\overline{\text{TS}}$ | SD_VDD | VSS | SD_VDD | SD_VDD | OVDD | OVDD | VSS | OVDD | $\overline{\text{TA}}$ | USB_ TXEN | USB_ RXD | EXTAL | L |
| M | D31 | $\overline{\text{SD_CS1}}$ | $\overline{\text{BS3}}$ | SD_DQS3 | VSS | SD_VDD | SD_VDD | SD_VDD | OVDD | OVDD | OVDD | NC | USB_ SUSP | PLL_ TEST | VDDPLL | XTAL | M |
| N | D30 | D29 | D28 | D20 | D16 | SD_A10 | $\overline{\text{CS1}}$ | VDD | TEST | DDATA2 | DDATA0 | QSPI_ CS2 | CLK MOD1 | $\overline{\text{RSTOUT}}$ | $\overline{\text{RESET}}$ | VSS | N |
| P | D27 | D26 | D23 | D19 | SD_DQS2 | $\overline{\text{TIP}}$ | R/$\overline{\text{W}}$ | $\overline{\text{RCON}}$ | $\overline{\text{U2CTS}}$ | DDATA3 | DDATA1 | QSPI_ CS0 | CLK MOD0 | $\overline{\text{TRST}}$/ DSCLK | TDO/ DSO | TCLK/ PSTCLK | P |
| R | D25 | D24 | D22 | D18 | $\overline{\text{BS2}}$ | $\overline{\text{CS0}}$ | VSS | $\overline{\text{U2RTS}}$ | U2TXD | PST2 | PST0 | QSPI_ DOUT | QSPI_ CS3 | JTAG_ EN | TMS/ $\overline{\text{BKPT}}$ | TDI/DSI | R |
| T | VSS | SD_ VREF | D21 | D17 | $\overline{\text{SD_CS0}}$ | $\overline{\text{DDR_CLK OUT}}$ | DDR_CLK OUT | $\overline{\text{TEA}}$ | U2RXD | PST3 | PST1 | CLKOUT | QSPI_ DIN | QSPI_ CS1 | QSPI_ CLK | VSS | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

**Figure 3. MCF5274 and MCF5275 Pinout (256 MAPBGA)**

## 6.4 Package Dimensions - 196 MAPBGA

Figure 6 shows MCF5275 196 MAPBGA package dimensions.




| DIM | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 1.25 | 1.60 |
| A1 | 0.27 | 0.47 |
| A2 | 1.16 REF | |
| b | 0.45 | 0.55 |
| D | 15.00 BSC | |
| E | 15.00 BSC | |
| e | 1.00 BSC | |
| S | 0.50 BSC | |

**Figure 6. 196 MAPBGA Package Dimensions**

$P_{INT}$ = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

## 8.3 ESD Protection

**Table 9. ESD Protection Characteristics[1, 2]**

| Characteristics | Symbol | Value | Units |
|---|---|---|---|
| ESD Target for Human Body Model | HBM | 2000 | V |
| ESD Target for Machine Model | MM | 200 | V |
| HBM Circuit Description | $R_{series}$ | 1500 | Ω |
| | C | 100 | pF |
| MM Circuit Description | $R_{series}$ | 0 | Ω |
| | C | 200 | pF |
| Number of pulses per pin (HBM)<br>positive pulses<br>negative pulses | <br>—<br>— | <br>1<br>1 | — |
| Number of pulses per pin (MM)<br>positive pulses<br>negative pulses | <br>—<br>— | <br>3<br>3 | — |
| Interval of Pulses | — | 1 | sec |

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

## 8.4 DC Electrical Specifications

**Table 10. DC Electrical Specifications[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | 1.4 | 1.6 | V |
| I/O Pad Supply Voltage | $OV_{DD}$ | 3.0 | 3.6 | V |
| PLL Supply Voltage | $V_{DDPLL}$ | 3.0 | 3.6 | V |
| SSTL I/O Pad Supply Voltage | $SDV_{DD}$ | 2.3 | 2.7 | V |
| SSTL I/O Pad Supply Voltage | $SDV_{DD}$ | 3.0 | 3.6 | V |
| SSTL Memory pads reference voltage (SD $V_{DD}$ = 2.5V) | $V_{REF}$ | 0.5 SD $V_{DD}$ | —[2] | V |
| SSTL Memory pads reference voltage (SD $V_{DD}$ = 3.3V) | $V_{REF}$ | 0.45 SD $V_{DD}$ | —[2] | V |
| Input High Voltage 3.3V I/O Pads | $V_{IH}$ | 0.7 x $OV_{DD}$ | $OV_{DD}$ + 0.3 | V |
| Input Low Voltage 3.3V I/O Pads | $V_{IL}$ | $V_{SS}$ – 0.3 | 0.35 x $OV_{DD}$ | V |
| Output High Voltage 3.3V I/O Pads<br>$I_{OH}$ = –2.0 mA | $V_{OH}$ | $OV_{DD}$ - 0.5 | — | V |
| Output Low Voltage 3.3V I/O Pads<br>$I_{OL}$ = 2.0mA | $V_{OL}$ | — | 0.5 | V |
| Input Hysteresis 3.3V I/O Pads | $V_{HYS}$ | 0.06 x $V_{DD}$ | — | mV |
| Input High Voltage SSTL 3.3V/2.5V[3] | $V_{IH}$ | $V_{REF}$ + 0.3 | $SDV_{DD}$ + 0.3 | V |
| Input Low Voltage SSTL 3.3V/2.5V[3] | $V_{IL}$ | $V_{SS}$ - 0.3 | $V_{REF}$ - 0.3 | V |
| Output High Voltage SSTL 3.3V/2.5V[4]<br>$I_{OH}$ = –5.0 mA | $V_{OH}$ | $SDV_{DD}$ - 0.25V | — | V |
| Output Low Voltage SSTL 3.3V/2.5V[4]<br>$I_{OL}$ = 5.0 mA | $V_{OL}$ | — | 0.35 | V |
| Input Leakage Current<br>$V_{in}$ = $V_{DD}$ or $V_{SS}$, Input-only pins | $I_{in}$ | -1.0 | 1.0 | µA |
| High Impedance (Off-State) Leakage Current<br>$V_{in}$ = $V_{DD}$ or $V_{SS}$, All input/output and output pins | $I_{OZ}$ | -1.0 | 1.0 | µA |
| Weak Internal Pull Up Device Current, tested at $V_{IL}$ Max.[5] | $I_{APU}$ | -10 | -130 | µA |
| Input Capacitance [6]<br>All input-only pins<br>All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | <br>7<br>7 | pF |

## 8.5 Oscillator and Phase Lock Loop (PLLMRFM) Electrical Specifications

**Table 11. PLL Electrical Specifications[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| PLL Reference Frequency Range<br>Crystal reference<br>External reference<br>1:1 Mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$) | <br>$f_{ref\_crystal}$<br>$f_{ref\_ext}$<br>$f_{ref\_1:1}$ | <br>8<br>8<br>24 | <br>25<br>25<br>83 | MHz |
| Core frequency<br>CLKOUT Frequency [2]<br>External reference<br>On-Chip PLL Frequency | $f_{core}$<br><br><br>$f_{sys/2}$ | <br><br>0<br>$f_{ref}$ / 32 | 166<br><br>83<br>83 | MHz<br><br>MHz<br>MHz |
| Loss of Reference Frequency [3, 5] | $f_{LOR}$ | 100 | 1000 | kHz |
| Self Clocked Mode Frequency [4, 5] | $f_{SCM}$ | TBD | TBD | MHz |
| Crystal Start-up Time [5, 6] | $t_{cst}$ | — | 10 | ms |
| EXTAL Input High Voltage<br>Crystal Mode<br>All other modes (Dual Controller (1:1), Bypass, External) | $V_{IHEXT}$<br>$V_{IHEXT}$ | <br>TBD<br>TBD | <br>TBD<br>TBD | V |
| EXTAL Input Low Voltage<br>Crystal Mode<br>All other modes (Dual Controller (1:1), Bypass, External) | $V_{ILEXT}$<br>$V_{ILEXT}$ | <br>TBD<br>TBD | <br>TBD<br>TBD | V |
| XTAL Output High Voltage<br>$I_{OH}$ = 1.0 mA | $V_{OH}$ | <br>TBD | <br>— | V |
| XTAL Output Low Voltage<br>$I_{OL}$ = 1.0 mA | $V_{OL}$ | <br>— | <br>TBD | V |
| XTAL Load Capacitance[7] | | 5 | 30 | pF |
| PLL Lock Time [8] | $t_{lpll}$ | — | 750 | µs |
| Power-up To Lock Time [6, 9]<br>With Crystal Reference<br>Without Crystal Reference[10] | $t_{lplk}$ | <br>—<br>— | <br>11<br>750 | <br>ms<br>µs |
| 1:1 Mode Clock Skew (between CLKOUT and EXTAL) [11] | $t_{skew}$ | -1 | 1 | ns |
| Duty Cycle of reference [5] | $t_{dc}$ | 40 | 60 | % $f_{sys/2}$ |
| Frequency un-LOCK Range | $f_{UL}$ | -3.8 | 4.1 | % $f_{sys/2}$ |
| Frequency LOCK Range | $f_{LCK}$ | -1.7 | 2.0 | % $f_{sys/2}$ |
| CLKOUT Period Jitter, [5, 6, 9,12, 13] Measured at $f_{sys/2}$ Max<br>Peak-to-peak Jitter (Clock edge to clock edge)<br>Long Term Jitter (Averaged over 2 ms interval) | $C_{jitter}$ | <br>—<br>— | <br>5<br>.01 | % $f_{sys/2}$ |
| Frequency Modulation Range Limit[14], [15]<br>($f_{sys/2}$Max must not be exceeded) | $C_{mod}$ | 0.8 | 2.2 | % $f_{sys/2}$ |
| ICO Frequency. $f_{ico} = f_{ref} * 2 * (MFD+2)$[16] | $f_{ico}$ | 48 | 83 | MHz |

1 All values given are initial design targets and subject to change.
2 All internal registers retain data at 0 Hz.
3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.

4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below $f_{LOR}$ with default MFD/RFD settings.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 Proper PC board layout procedures must be followed to achieve specifications.
7 Load capacitance determined from crystal manufacturer specifications and includes circuit board parasitics.
8 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
9 Assuming a reference is available at power up, lock time is measured from the time $V_{DD}$ and $V_{DDPLL}$ are valid to $\overline{RSTOUT}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
10 $t_{lpll} = (64 * 4 * 5 + 5 \times \tau) \times T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6} \times 2(MFD + 2)$
11 PLL is operating in 1:1 PLL mode.
12 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DDPLL}$ and $V_{SSPLL}$ and variation in crystal oscillator frequency increase the jitter percentage for a given interval.
13 Based on slow system clock of 33MHz maximum frequency.
14 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100KHz.
15 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.
16 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

## 8.6 External Interface Timing Characteristics

Table 12 lists processor bus input timings.

**NOTE**

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

**Table 12. Processor Bus Input Timing Specifications**

| Name | Characteristic[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| B0 | CLKOUT | $t_{CYC}$ | 12 | — | ns |
| **Control Inputs** | | | | | |
| B1a | Control input valid to CLKOUT high[2] | $t_{CVCH}$ | 9 | — | ns |
| B1b | $\overline{BKPT}$ valid to CLKOUT high[3] | $t_{BKVCH}$ | 9 | — | ns |
| B2a | CLKOUT high to control inputs invalid[2] | $t_{CHCII}$ | 0 | — | ns |
| B2b | CLKOUT high to asynchronous control input $\overline{BKPT}$ invalid[3] | $t_{BKNCH}$ | 0 | — | ns |
| **Data Inputs** | | | | | |
| B4 | Data input (D[31:16]) valid to CLKOUT high | $t_{DIVCH}$ | 4 | — | ns |
| B5 | CLKOUT high to data input (D[31:16]) invalid | $t_{CHDII}$ | 0 | — | ns |

1 Timing specifications have been indicated taking into account the full drive strength for the pads.
2 $\overline{TEA}$ and $\overline{TA}$ pins are being referred to as control inputs.
3 Refer to figure A-19.

Timings listed in Table 12 are shown in Figure 7.

* The timings are also valid for inputs sampled on the negative clock edge.

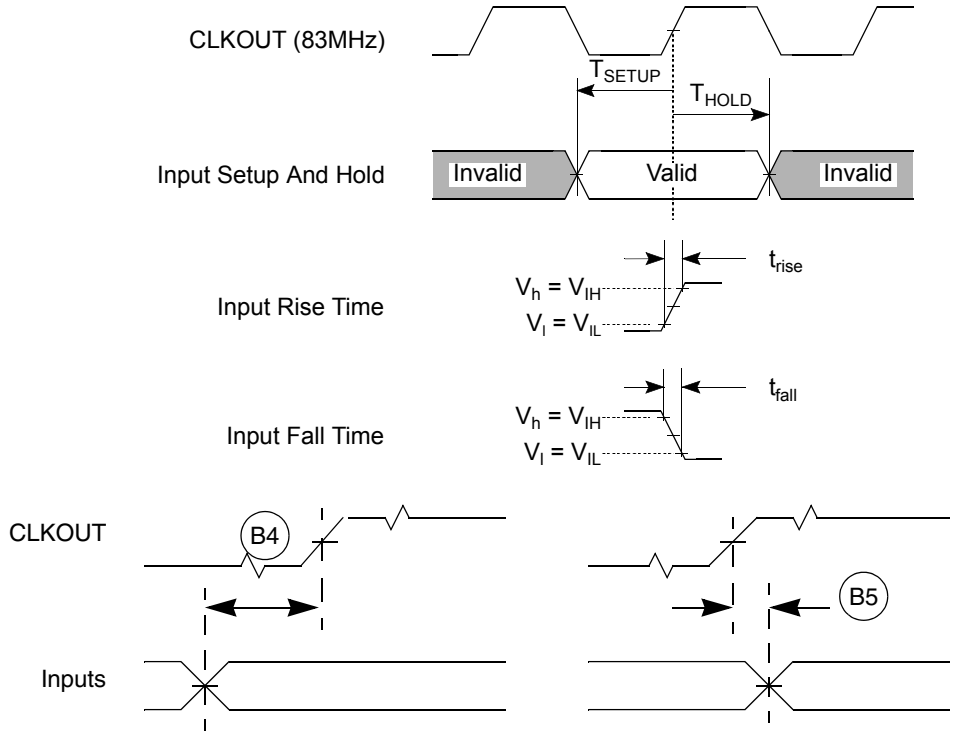



**Figure 7. General Input Timing Requirements**

## 8.7 Processor Bus Output Timing Specifications

Table 13 lists processor bus output timings.

**Table 13. External Bus Output Timing Specifications**

| Name | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **Control Outputs** | | | | | |
| B6a | CLKOUT high to chip selects ($\overline{CS}$[7:0]) valid[1] | $t_{CHCV}$ | — | $0.5t_{CYC}$ + 5.5 | ns |
| B6b | CLKOUT high to byte enables ($\overline{BS}$[3:2]) valid[1] | $t_{CHBV}$ | — | $0.5t_{CYC}$ + 5.5 | ns |
| B6c | CLKOUT high to output enable ($\overline{OE}$) valid[1] | $t_{CHOV}$ | — | $0.5t_{CYC}$ + 5.5 | ns |
| B7 | CLKOUT high to control output ($\overline{BS}$[3:2], $\overline{OE}$) invalid | $t_{CHCOI}$ | $0.5t_{CYC}$ + 1.0 | — | ns |
| B7a | CLKOUT high to chip selects invalid | $t_{CHCI}$ | $0.5t_{CYC}$ + 1.0 | — | ns |
| **Address and Attribute Outputs** | | | | | |
| B8 | CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, TSIZ[1:0], $\overline{TIP}$, R/$\overline{W}$) valid | $t_{CHAV}$ | — | 9 | ns |
| B9 | CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, TSIZ[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid | $t_{CHAI}$ | 1.0 | — | ns |

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 13.

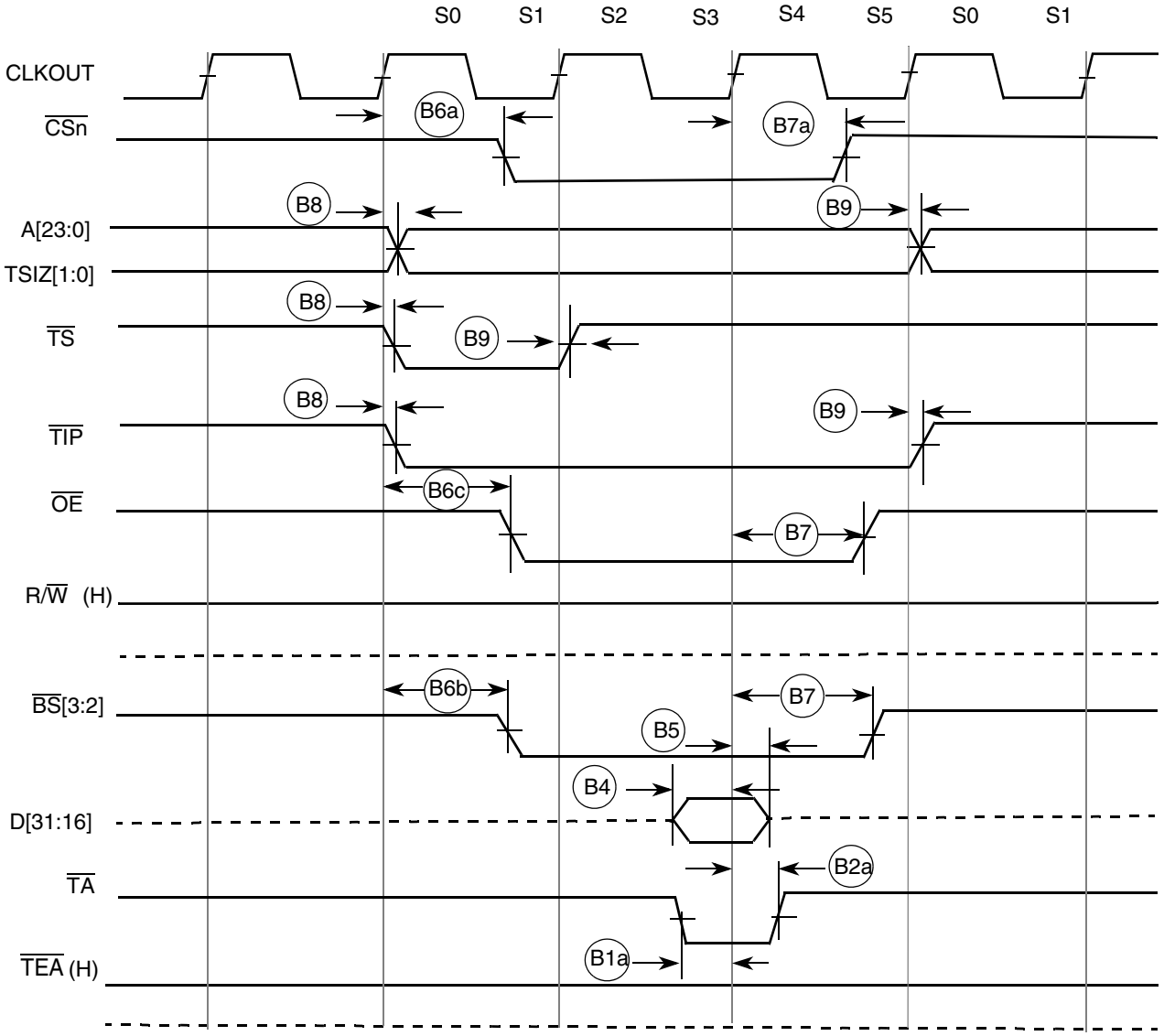



**Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$**

Figure 10 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 13.

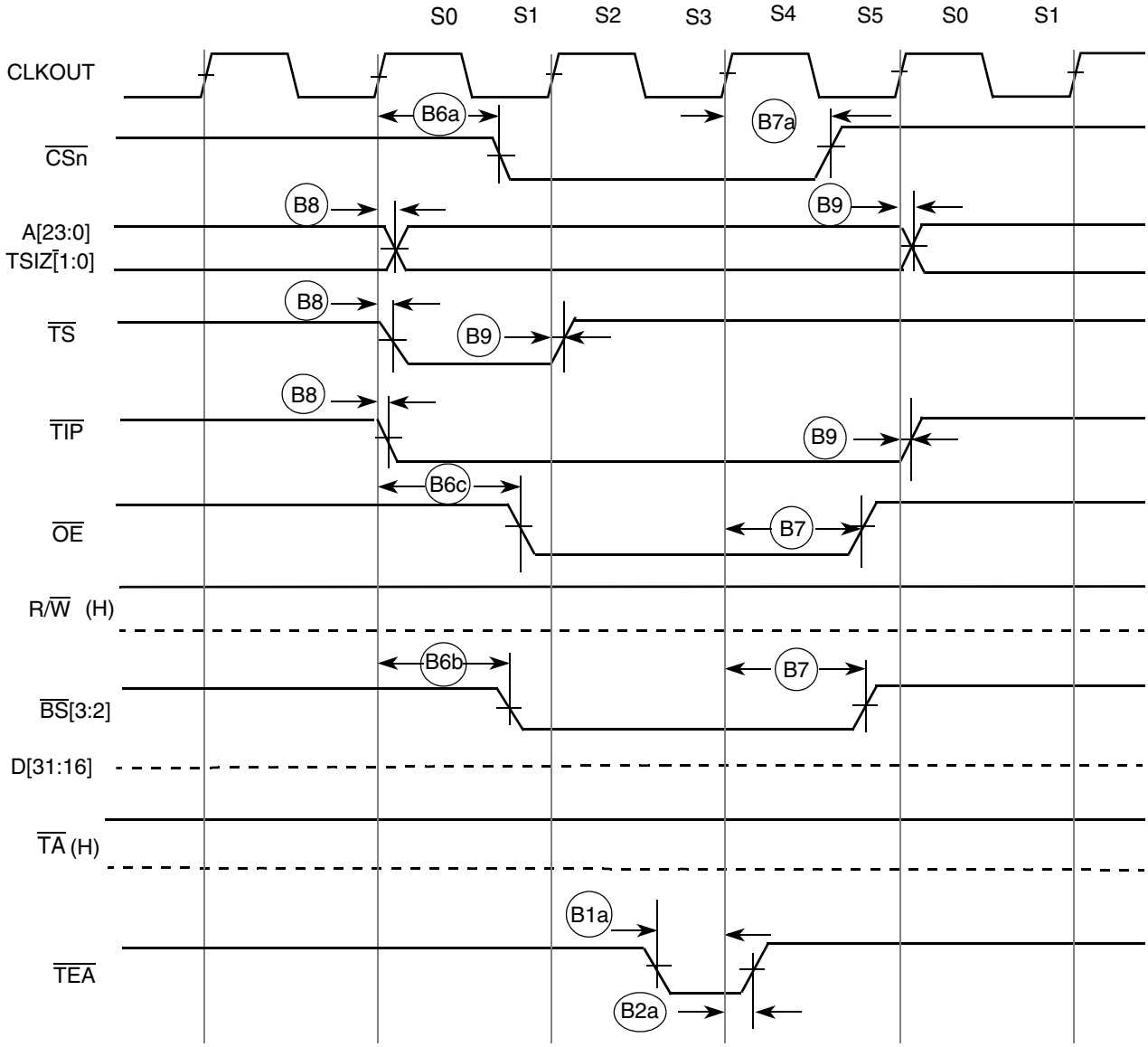



**Figure 10. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$**

**Table 15. DDR Timing (continued)**

| NUM | Characteristic[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| DD13 | DQS input read preamble width ($t_{RPRE}$) | $t_{RPRE}$ | 0.9 | 1.1 | $t_{CK}$ |
| DD14 | DQS input read postamble width ($t_{RPST}$) | $t_{RPST}$ | 0.4 | 0.6 | $t_{CK}$ |
| DD15 | DQS output write preamble width ($t_{WPRE}$) | $t_{WPRE}$ | 0.25 | — | $t_{CK}$ |
| DD16 | DQS output write postamble width ($t_{WPST}$) | $t_{WPST}$ | 0.4 | 0.6 | $t_{CK}$ |

1 All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2 DDR_CLKOUT operates at half the frequency of the PLLMRFM output and the ColdFire core.
3 $t_{CKH}$ + $t_{CKL}$ must be less than or equal to $t_{CK}$.
4 D[31:24] is relative to $\overline{\text{SD\_DQS3}}$ and D[23:16] is relative to $\overline{\text{SD\_DQS2}}$.
5 The first data beat is valid before the first rising edge of $\overline{\text{SD\_DQS}}$ and after the $\overline{\text{SD\_DQS}}$ write preamble. The remaining data beats are valid for each subsequent $\overline{\text{SD\_DQS}}$ edge
6 Data input skew is derived from each $\overline{\text{SD\_DQS}}$ clock edge. It begins with a $\overline{\text{SD\_DQS}}$ transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).
7 Data input hold is derived from each $\overline{\text{SD\_DQS}}$ clock edge. It begins with a $\overline{\text{SD\_DQS}}$ transition and ends when the first data line becomes invalid.

Figure 13 shows a DDR SDRAM write cycle.

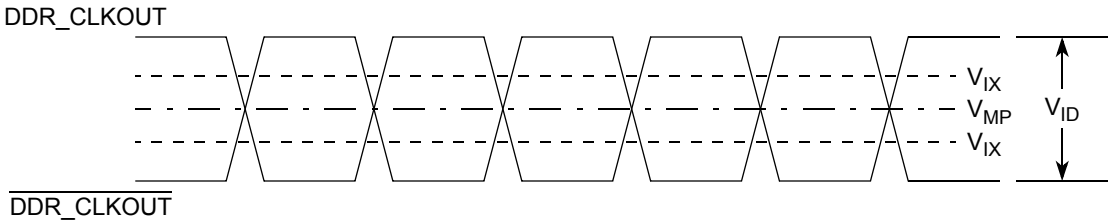



**Figure 12. DDR_CLKOUT and $\overline{\text{DDR\_CLKOUT}}$ Crossover Timing**

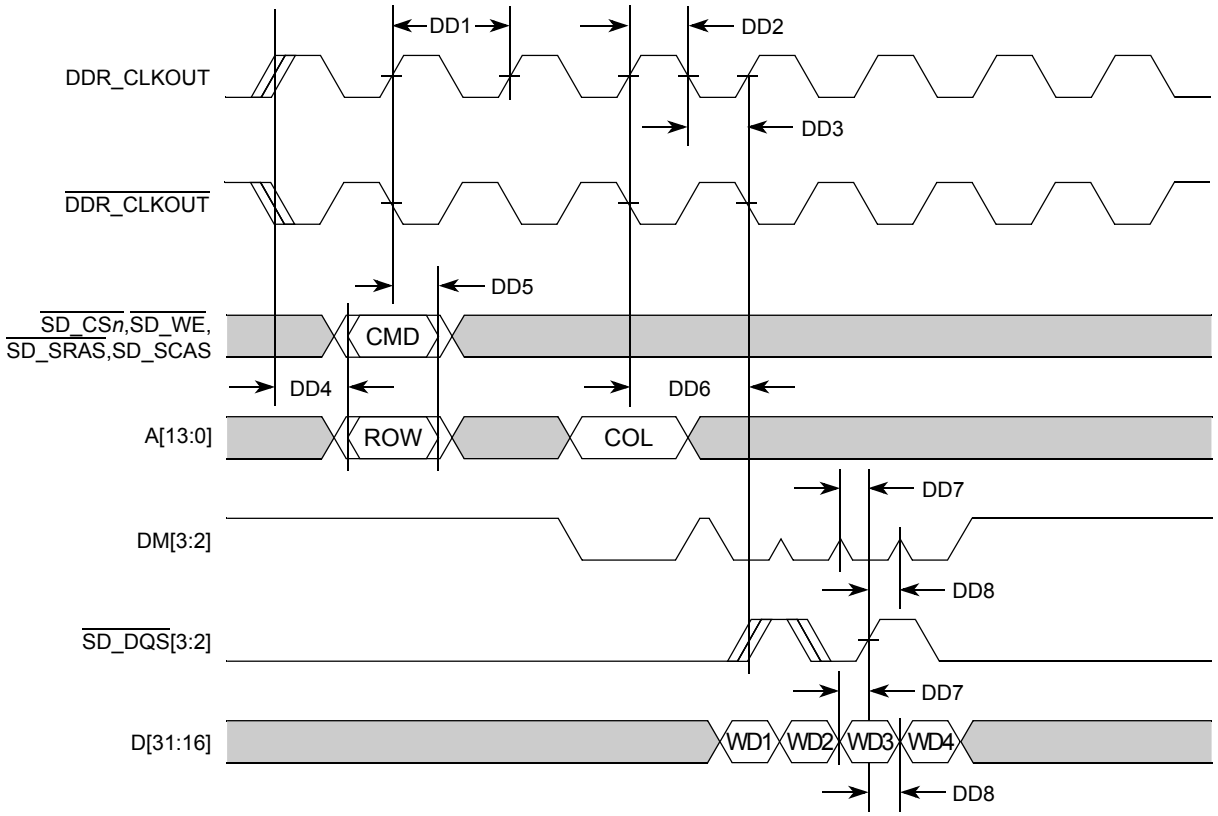



**Figure 13. DDR Write Timing**

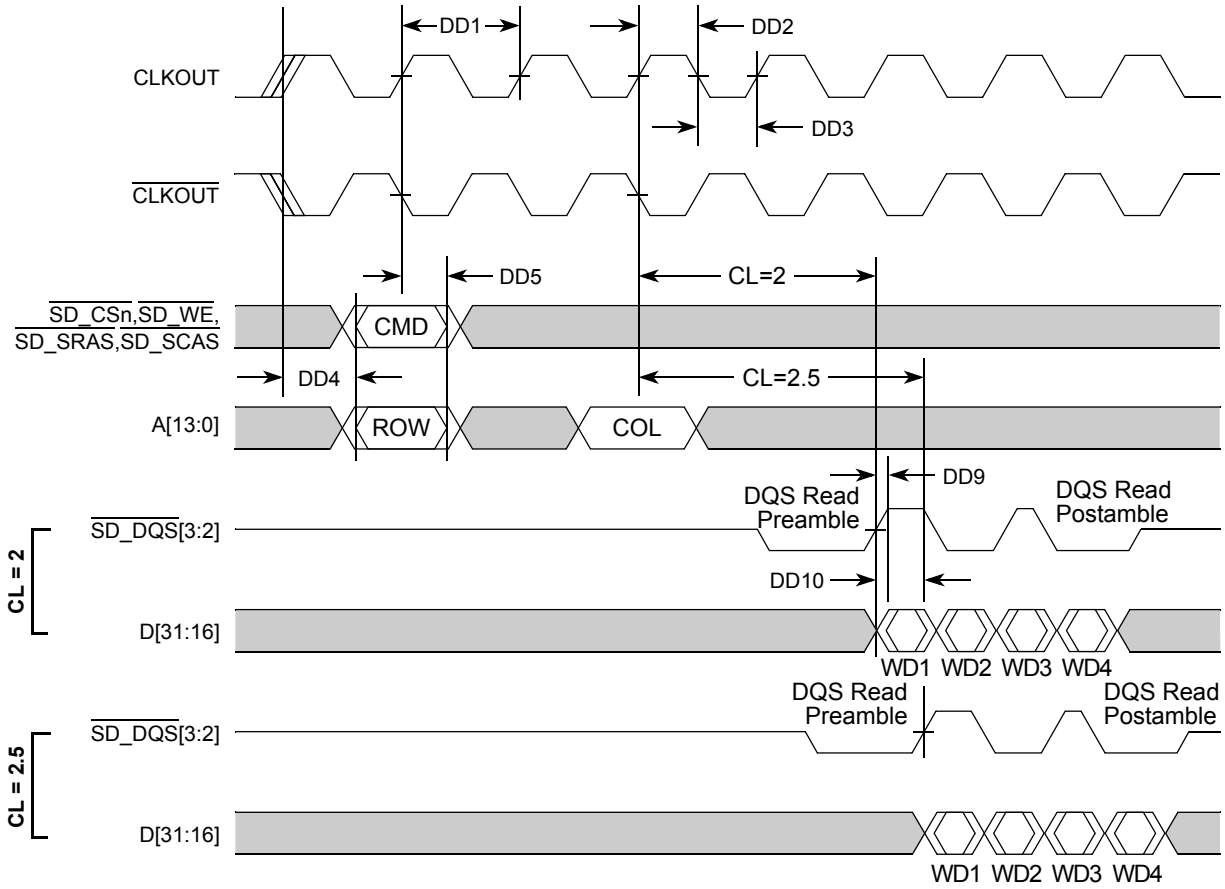



**Figure 14. DDR Read Timing**

## 8.9 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR control, timers, UARTS, FEC0, FEC1, Interrupts and USB interfaces. When in GPIO mode the timing specification for these pins is given in Table 16 and Figure 15.

**Table 16. GPIO Timing**

| NUM | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| G1 | CLKOUT High to GPIO Output Valid | $t_{CHPOV}$ | — | 10 | ns |
| G2 | CLKOUT High to GPIO Output Invalid | $t_{CHPOI}$ | 1.0 | — | ns |
| G3 | GPIO Input Valid to CLKOUT High | $t_{PVCH}$ | 9 | — | ns |
| G4 | CLKOUT High to GPIO Input Invalid | $t_{CHPI}$ | 1.5 | — | ns |

## 8.11.5 USB Interface AC Timing Specifications

Table 22 lists USB Interface timings.

**Table 22. USB Interface Timing**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| US1 | USB_CLK frequency of operation | 48 | 48 | MHz |
| US2 | USB_CLK fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 2 | ns |
| US3 | USB_CLK rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | 2 | ns |
| US4 | USB_CLK duty cycle (at 0.5 x O $V_{DD}$) | 45 | 55 | % |
| **Data Inputs** | | | | |
| US5 | USB_RP, USB_RN, USB_RXD valid to USB_CLK high | 6 | — | ns |
| US6 | USB_CLK high to USB_RP, USB_RN, USB_RXD invalid | 6 | — | ns |
| **Data Outputs** | | | | |
| US7 | USB_CLK high to USB_TP, USB_TN, USB_SUSP valid | — | 12 | ns |
| US8 | USB_CLK high to USB_TP, USB_TN, USB_SUSP invalid | 3 | — | ns |

Figure 20 shows USB interface timings listed in Table 22.

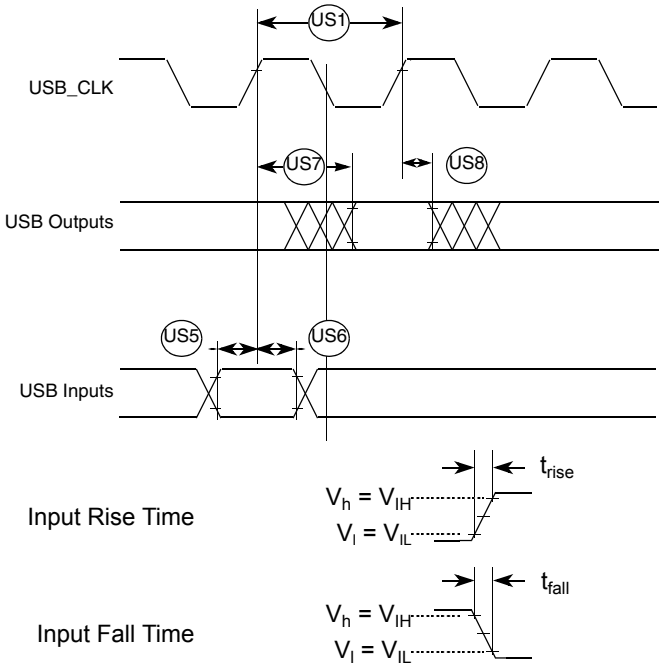



**Figure 20. USB Signals Timing Diagram**