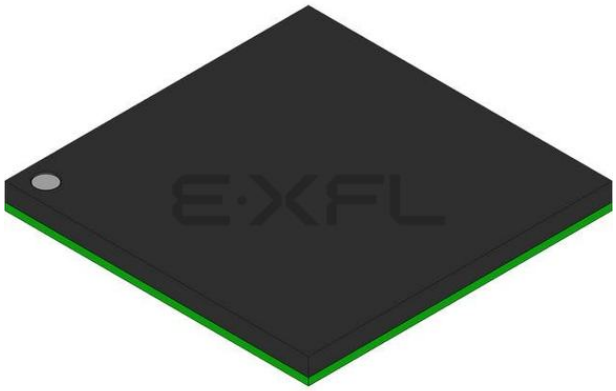

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, WDT
Number of I/O	69
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5274lcvm166

In addition, the MCF5275 family features an enhanced multiply accumulate unit (EMAC), large on-chip memory (64 Kbytes SRAM, 16 Kbytes configurable cache), and a 16-bit DDR SDRAM memory controller.

These devices are ideal for cost-sensitive applications requiring significant control processing for file management, connectivity, data buffering, and user interface, as well as signal processing in a variety of key markets such as security, imaging, networking, gaming, and medical. This leading package of integration and high performance allows fast time to market through easy code reuse and extensive third party tool support.

To locate any published errata or updates for this document, refer to the ColdFire products website at http://www.freescale.com/coldfire.

1 MCF5275 Family Configurations

Table 1. MCF5275 Family Configurations

Module	MCF5274L	MCF5275L	MCF5274	MCF5275
ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•
System Clock	up to 166 MHz			
Performance (Dhrystone 2.1 MIPS)	up to 159			
Instruction/Data Cache	16 Kbytes (configurable)			
Static RAM (SRAM)	64 Kbytes			
Interrupt Controllers (INTC)	2	2	2	2
Edge Port Module (EPORT)	•	•	•	•
External Interface Module (EIM)	•	•	•	•
4-channel Direct-Memory Access (DMA)	•	•	•	•
DDR SDRAM Controller	•	•	•	•
Fast Ethernet Controller (FEC)	1	1	2	2
Watchdog Timer Module (WDT)	•	•	•	•
4-channel Programmable Interval Timer Module (PIT)	•	•	•	•
32-bit DMA Timers	4	4	4	4
USB	•	•	•	•
QSPI	•	•	•	•
UART(s)	3	3	3	3
I^2C	•	•	•	•
PWM	4	4	4	4
General Purpose I/O Module (GPIO)	•	•	•	•
CIM = Chip Configuration Module + Reset Controller Module	•	•	•	•
Debug BDM	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•
Hardware Encryption	—	•	—	•
Package	196 MAPBGA		256 MAPBGA	

4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF5275 signals, consult the *MCF5275 Reference Manual* (MCF5275RM).

Table 2 lists the signals for the MCF5275 in functional group order. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts," for package diagrams.

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 2. MCF5274 and MCF5275 Signal Information and Muxing

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
Reset						
$\overline{\text{RESET}}$	—	—	—	I	N15	K12
$\overline{\text{RSTOUT}}$	—	—	—	O	N14	L12
Clock						
EXTAL	—	—	—	I	L16	M14
XTAL	—	—	—	O	M16	N14
CLKOUT	—	—	—	O	T12	P9
Mode Selection						
CLKMOD[1:0]	—	—	—	I	N13, P13	M11, N11
$\overline{\text{RCON}}$	—	—	—	I	P8	M6
External Memory Interface and Ports						
A[23:21]	PADDR[7:5]	$\overline{\text{CS}}$[6:4]	—	O	A11, B11, C11	A8, B8, C8
A[20:0]	—	—	—	O	A12, B12, C12, A13, B13, C13, A14, B14, C14, B15, C15, B16, C16, D14, D15, E14:16, F14:16	B9, D9, C9, C10, B10, A11, C11, B11, A12, D11, C12, B13, C13, D12, E11, D13, E12, F11, D14, E13, F13

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
D[31:16]	—	—	—	O	M1, N1, N2, N3, P1, P2, R1, R2, P3, R3, T3, N4, P4, R4, T4, N5	J3, L1, K2, K3, M1, L2, L3, L4, K4, J4, M2, N1, N2, M3, M4, N3
$\overline{BS}$[3:2]	$\overline{PBS}$[3:2]	$\overline{CAS}$[3:2]	—	O	M3, R5	K1, L5
$\overline{OE}$	PBUSCTL[7]	—	—	O	K1	H4
$\overline{TA}$	PBUSCTL[6]	—	—	I	L13	K14
$\overline{TEA}$	PBUSCTL[5]	$\overline{DREQ1}$	—	I	T8	—
R/$\overline{W}$	PBUSCTL[4]	—	—	O	P7	L6
TSIZ1	PBUSCTL[3]	DACK1	—	O	D16	B14
TSIZ0	PBUSCTL[2]	DACK0	—	O	G16	E14
$\overline{TS}$	PBUSCTL[1]	DACK2	—	O	L4	H2
$\overline{TIP}$	PBUSCTL[0]	$\overline{DREQ0}$	—	O	P6	—
Chip Selects						
$\overline{CS}$[7:1]	PCS[7:1]	—	—	O	D10:13, E13, F13, N7	D8, A9, A10, D10, B12, C14, P4
$\overline{CS0}$	—	—	—	O	R6	N5
DDR SDRAM Controller						
DDR_CLKOUT	—	—	—	O	T7	P6
$\overline{DDR\_CLKOUT}$	—	—	—	O	T6	P5
$\overline{SD\_CS}$[1:0]	PSDRAM[7:6]	$\overline{CS}$[3:2]	—	O	M2, T5	H3, M5
$\overline{SD\_SRAS}$	PSDRAM[5]	—	—	O	L2	H1
$\overline{SD\_SCAS}$	PSDRAM[4]	—	—	O	L1	G3
$\overline{SD\_WE}$	PSDRAM[3]	—	—	O	K2	G4
SD_A10	—	—	—	O	N6	N4
$\overline{SD\_DQS}$[3:2]	PSDRAM[2:1]	—	—	I/O	M4, P5	J2, P3
SD_CKE	PSDRAM[0]	—	—	O	L3	J1
SD_VREF	—	—	—	I	A15, T2	A13, P2
External Interrupts Port						
$\overline{IRQ}$[7:5]	PIRQ[7:5]	—	—	I	G13, H16, H15	F14, G13, G14
$\overline{IRQ}$[4]	PIRQ[4]	$\overline{DREQ2}$	—	I	H14	H11
$\overline{IRQ}$[3:2]	PIRQ[3:2]	$\overline{DREQ}$[3:2]	—	I	J14, J13	H14, H12

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
VSSPLL	—	—	—	I	K16	L13
VSS	—	—	—	I	A1, A10, A16, E5, E12, F6, F11, G7:10, H7:10, J1, J7:10, K7:10, L6, L11, M5, N16, R7, T1, T16	F7, F8, G6:9, H6:9, J7, J8
OVDD	—	—	—	I	E6:8, F5, F7, F8, G5, G6, H5, H6, J11, J12, K11, K12, L9, L10, L12, M9:11	E5:7, F5, F6, H10, J9, J10, K8:10
VDD	—	—	—	I	D8, H13, K4, N8	D6, G5, G12, L7
SD_VDD	—	—	—	I	E9:11, F9, F10, F12, G11, G12, H11, H12, J5, J6, K5, K6, L5, L7, L8, M6, M7, M8	E8:10, F9, F10, G10, H5, J5, J6, K5:7

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5275.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33uF, 0.1 µF, and 0.01 µF across each power supply

6.3 196 MAPBGA Pinout

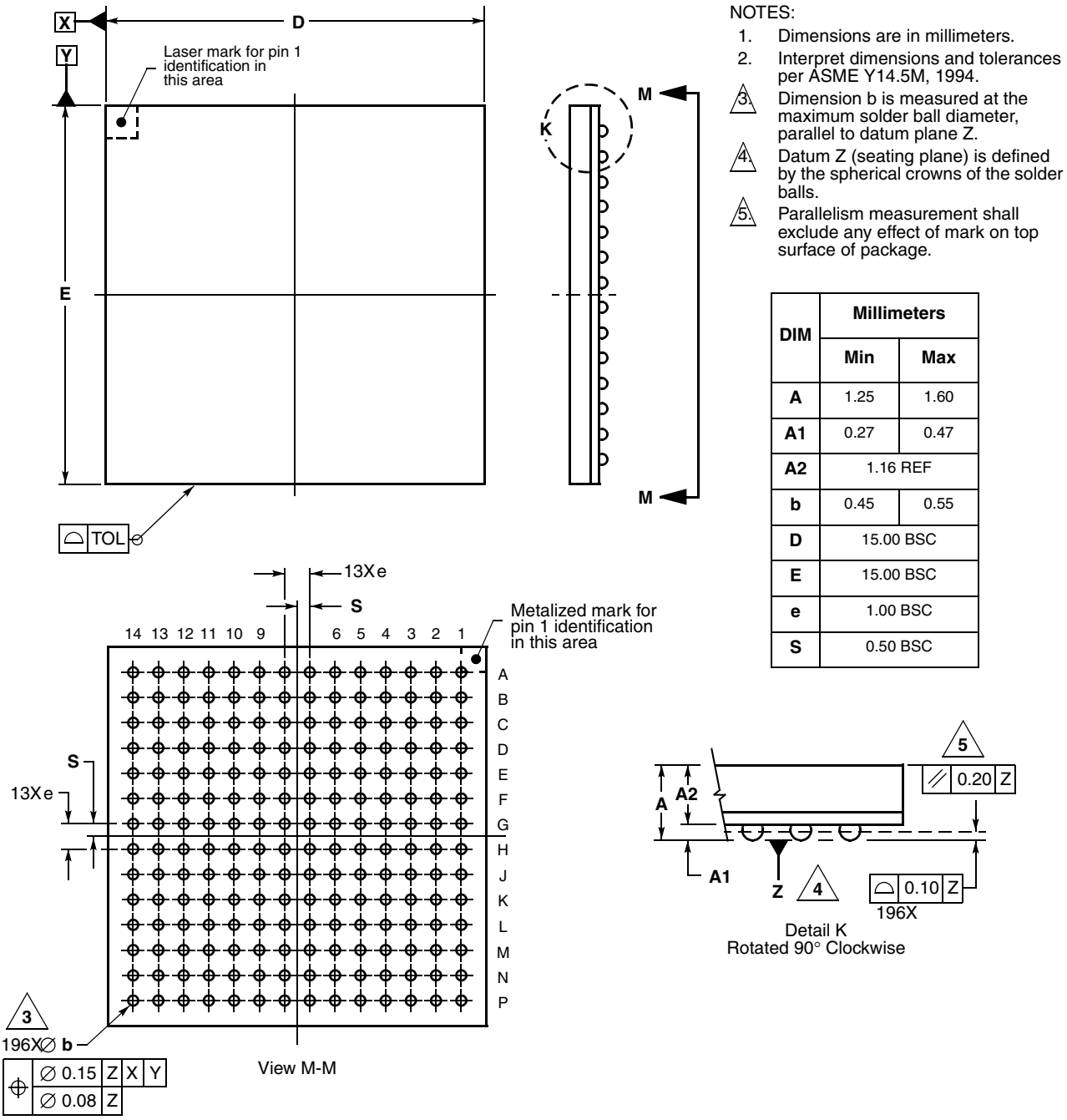
Figure 5 is a consolidated MCF5274L/75L pinout for the 196 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	FEC0_ CRS	FEC0_ MDIO	U0RXD	U0TXD	U1RXD	I2C_SCL	A23	$\overline{\text{CS6}}$	$\overline{\text{CS5}}$	A15	A12	SD_ VREF	NC	A
B	FEC0_ RXD2	FEC0_ RXD1	FEC0_ RXCLK	FEC0_ COL	$\overline{\text{U0RTS}}$	$\overline{\text{U1RTS}}$	I2C_SDA	A22	A20	A16	A13	$\overline{\text{CS3}}$	A9	TSIZ1	B
C	FEC0_ TXCLK	FEC0_ TXER	FEC0_ TXEN	FEC0_ RXDV	FEC0_ MDC	$\overline{\text{U0CTS}}$	$\overline{\text{U1CTS}}$	A21	A18	A17	A14	A10	A8	$\overline{\text{CS2}}$	C
D	FEC0_ TXD3	FEC0_ TXD0	FEC0_ TXD1	FEC0_ RXD3	FEC0_ RXD0	VDD	U1TXD	$\overline{\text{CS7}}$	A19	$\overline{\text{CS4}}$	A11	A7	A5	A2	D
E	DT0IN	DT0OUT	FEC0_ TXD2	FEC0_ RXER	OVDD	OVDD	OVDD	SD_VDD2	SD_VDD2	SD_VDD2	A6	A4	A1	TSIZ0	E
F	DT1IN	DT1OUT	DT2IN	DT2OUT	OVDD	OVDD	VSS	VSS	SD_VDD2	SD_VDD2	A3	USB_CLK	A0	$\overline{\text{IRQ7}}$	F
G	DT3OUT	DT3IN	$\overline{\text{SD_CAS}}$	$\overline{\text{SD_WE}}$	VDD	VSS	VSS	VSS	VSS	SD_VDD2	USB_ SPEED	VDD	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ5}}$	G
H	$\overline{\text{SD_SRAS}}$	$\overline{\text{TS}}$	$\overline{\text{SD_CS1}}$	$\overline{\text{OE}}$	SD_VDD1	VSS	VSS	VSS	VSS	OVDD	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ2}}$	USB_RN	$\overline{\text{IRQ3}}$	H
J	SD_CKE	SD_DQS3	D31	D22	SD_VDD1	SD_VDD1	VSS	VSS	OVDD	OVDD	USB_RP	USB_TP	$\overline{\text{IRQ1}}$	USB_TN	J
K	$\overline{\text{BS3}}$	D29	D28	D23	SD_VDD1	SD_VDD1	SD_VDD1	OVDD	OVDD	OVDD	TDO/DSO	$\overline{\text{RESET}}$	USB_ TXEN	$\overline{\text{TA}}$	K
L	D30	D26	D25	D24	$\overline{\text{BS2}}$	R/$\overline{\text{W}}$	VDD	PST2	DDATA0	QSPI_ DOUT	QSPI_CLK	$\overline{\text{RSTOUT}}$	VSSPLL	USB_RXD	L
M	D27	D21	D18	D17	$\overline{\text{SD_CS0}}$	$\overline{\text{RCON}}$	DDATA3	PST1	QSPI_ CS0	QSPI_DIN	CLKMOD1	TDI/DSI	VDDPLL	EXTAL	M
N	D20	D19	D16	SD_A10	$\overline{\text{CS0}}$	TEST	DDATA2	PST0	QSPI_ CS2	QSPI_ CS1	CLKMOD0	TMS/$\overline{\text{BKPT}}$	USB_ SUSP	XTAL	N
P	NC	SD_ VREF	SD_DQS2	$\overline{\text{CS1}}$	$\overline{\text{DDR_CLK OUT}}$	DDR_CLK OUT	PST3	DDATA1	CLKOUT	QSPI_ CS3	JTAG_EN	TCLK/PST CLK	$\overline{\text{TRST}}$/DSC LK	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 5. MCF5274L and MCF5275L Pinout (196 MAPBGA)

6.4 Package Dimensions - 196 MAPBGA

Figure 6 shows MCF5275 196 MAPBGA package dimensions.



DIM	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 6. 196 MAPBGA Package Dimensions

7 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5274LVM166	MCF5274L RISC Microprocessor	196 MAPBGA	166 MHz	0° to +70° C
MCF5274LCVM166				-40° to +85° C
MCF5274VM166	MCF5274 RISC Microprocessor	256 MAPBGA	166 MHz	0° to +70° C
MCF5274CVM166				-40° to +85° C
MCF5275LCVM166	MCF5275L RISC Microprocessor	196 MAPBGA	166 MHz	-40° to +85° C
MCF5275CVM166	MCF5275 RISC Microprocessor	256 MAPBGA	166 MHz	-40° to +85° C

8 Electrical Characteristics

This appendix contains electrical specification tables and reference timing diagrams for the MCF5275 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5275.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

8.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
I/O Pad Supply Voltage (3.3V)	OV_{DD}	– 0.3 to +4.0	V
Memory Interface SSTL 2.5V Pad Supply Voltage	SDV_{DD}	– 0.3 to + 2.8	V
Memory Interface SSTL 3.3V Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., V_{SS} or O V_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and O V_{DD}.

5 Power supply must maintain regulation within operating O V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > O V_{DD}) is greater than I_{DD}, the injection current may flow out of O V_{DD} and could result in external power supply going out of regulation. Ensure the external O V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock).Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

8.2 Thermal Characteristics

Table 8 lists thermal resistance values

Table 8. Thermal characteristics

Characteristic		Symbol	256MBGA	196MBGA	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	26[1,2]	32[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	23[1,2]	29[1,2]	°C/W
Junction to board		θ_{JB}	15[3]	20[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	°C/W
Junction to top of package	Natural convection	Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

Θ_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

8.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V
ESD Target for Machine Model	MM	200	V
HBM Circuit Description	R_{series}	1500	Ω
	C	100	pF
MM Circuit Description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) positive pulses negative pulses	 — —	 3 3	—
Interval of Pulses	—	1	sec

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 13. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Data Outputs					
B11	CLKOUT high to data output (D[31:16]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:16]) invalid	t_{CHDOI}	1.0	—	ns
B13	CLKOUT high to data output (D[31:16]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}$, $\overline{BS}$, and $\overline{OE}$ transition after the falling edge of CLKOUT.

Read/write bus timings listed in Table 13 are shown in Figure 8, Figure 9, and Figure 10.

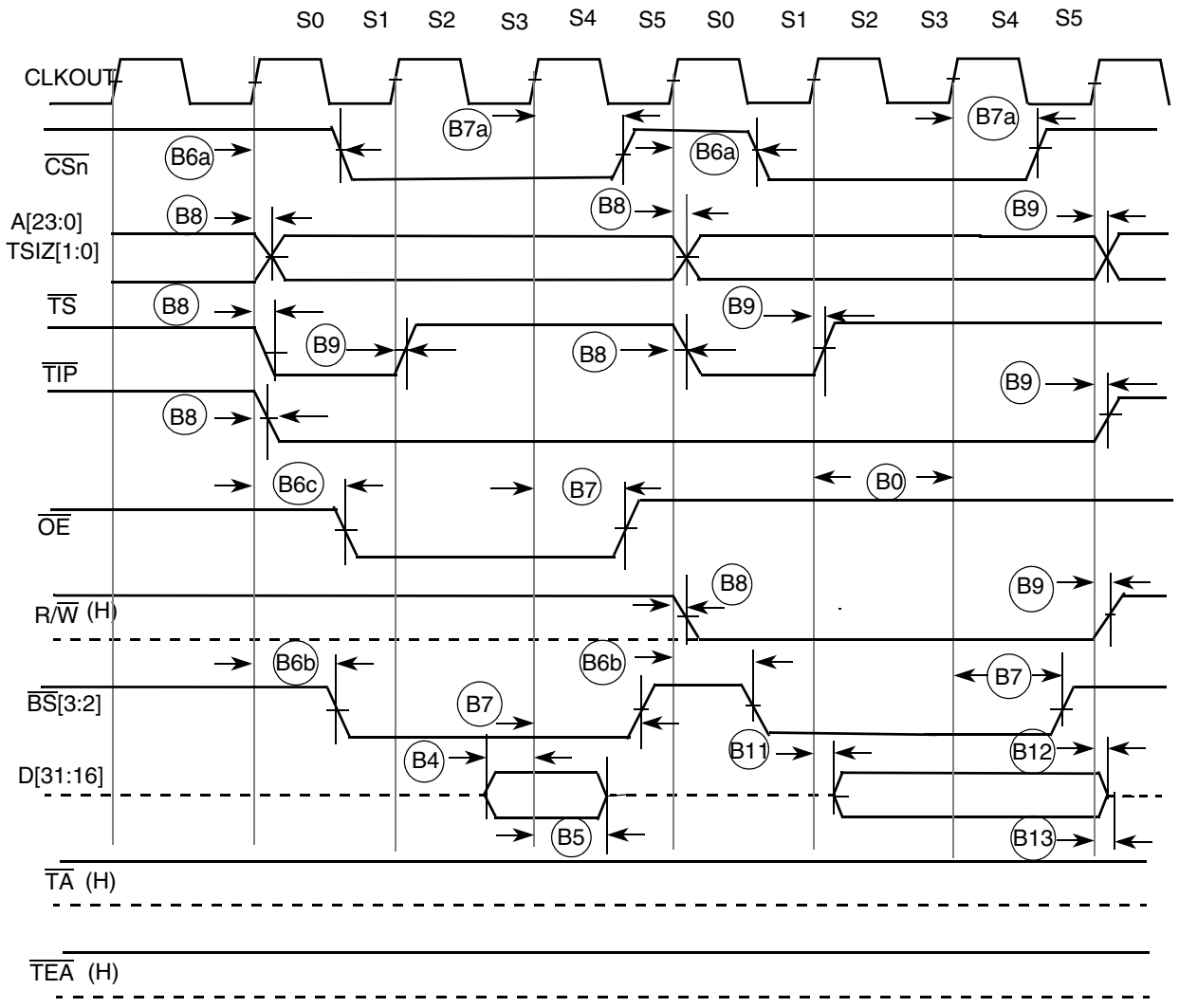


Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 13.

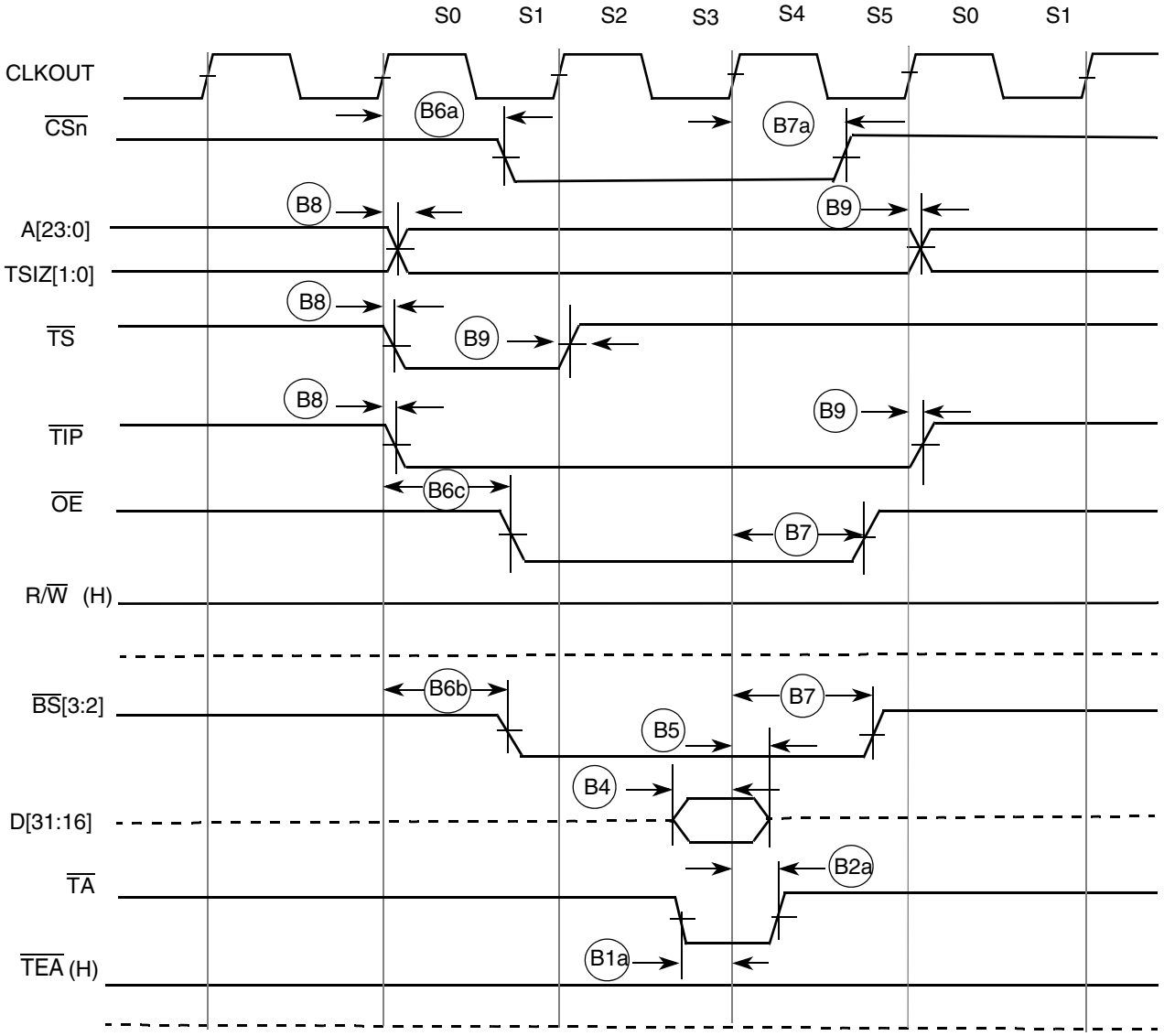


Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$

8.8 DDR SDRAM AC Timing Characteristics

The DDR SDRAM controller uses SSTL2 and I/O drivers. Class I or Class II drive strength is available and is user programmable. DDR Clock timing specifications are given in Table 14 and Figure 11.

Table 14. DDR Clock Timing Specifications[1]

Symbol	Characteristic	Min	Max	Unit
V_{MP}	Clock output mid-point voltage	1.05	1.45	V
V_{OUT}	Clock output voltage level	-0.3	SDV_{DD} + 0.3	V
V_{ID}	Clock output differential voltage (peak to peak swing)	0.7	SDV_{DD} + 0.6	V
V_{IX}	Clock crossing point voltage	1.05	1.45	V

1 SD V_{DD} is nominally 2.5V.

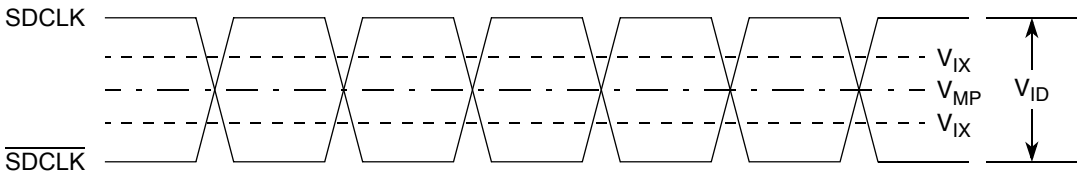


Figure 11. DDR Clock Timing Diagram

When using the DDR SDRAM controller the timing numbers in Table 15 must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the two DQS byte lanes.

Table 15. DDR Timing

NUM	Characteristic[1]	Symbol	Min	Max	Unit
	Frequency of operation[2]		TBD	83	MHz
DD1	Clock Period (DDR_CLKOUT)	t_{CK}	12	TBD	ns
DD2	Pulse Width High[3]	t_{CKH}	0.45	0.55	t_{CK}
DD3	Pulse Width Low[3]	t_{CKI}	0.45	0.55	t_{CK}
DD4	DDR_CLKOUT high to DDR address, SD_CKE, SD_CS[1:0], SD_SCAS, SD_SRAS, SD_WE valid	t_{CMV}	—	0.5 x t_{CK} + 1	ns
DD5	DDR_CLKOUT high to DDR address, SD_CKE, $\overline{\text{SD\_CS}}$, $\overline{\text{SD\_SCAS}}$, $\overline{\text{SD\_SRAS}}$, $\overline{\text{SD\_WE}}$ invalid	t_{CMH}	2	—	ns
DD6	Write command to first $\overline{\text{SD\_DQS}}$ Latching Transition	t_{DQSS}	—	1.25	t_{CK}
DD7	$\overline{\text{SD\_DQS}}$ high to Data and DM valid (write) - setup[4,5]	t_{QS}	1.5	—	ns
DD8	$\overline{\text{SD\_DQS}}$ high to Data and DM invalid (write) - hold[4]	t_{QH}	1	—	ns
DD9	$\overline{\text{SD\_DQS}}$ high to Data valid (read) - setup[6]	t_{IS}	—	1	ns
DD10	$\overline{\text{SD\_DQS}}$ high to Data invalid (read) - hold[7]	t_{IH}	0.25 x t_{CK} + 1	—	ns
DD11	$\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - setup	t_{DSS}	0.5	—	ns
DD12	$\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - hold	t_{DSH}	0.5	—	ns

Table 15. DDR Timing (continued)

NUM	Characteristic[1]	Symbol	Min	Max	Unit
DD13	DQS input read preamble width (t_{RPRE})	t_{RPRE}	0.9	1.1	t_{CK}
DD14	DQS input read postamble width (t_{RPST})	t_{RPST}	0.4	0.6	t_{CK}
DD15	DQS output write preamble width (t_{WPRE})	t_{WPRE}	0.25	—	t_{CK}
DD16	DQS output write postamble width (t_{WPST})	t_{WPST}	0.4	0.6	t_{CK}

1 All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2 DDR_CLKOUT operates at half the frequency of the PLLMRFM output and the ColdFire core.
3 t_{CKH} + t_{CKL} must be less than or equal to t_{CK}.
4 D[31:24] is relative to $\overline{\text{SD\_DQS3}}$ and D[23:16] is relative to $\overline{\text{SD\_DQS2}}$.
5 The first data beat is valid before the first rising edge of $\overline{\text{SD\_DQS}}$ and after the $\overline{\text{SD\_DQS}}$ write preamble. The remaining data beats are valid for each subsequent $\overline{\text{SD\_DQS}}$ edge
6 Data input skew is derived from each $\overline{\text{SD\_DQS}}$ clock edge. It begins with a $\overline{\text{SD\_DQS}}$ transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).
7 Data input hold is derived from each $\overline{\text{SD\_DQS}}$ clock edge. It begins with a $\overline{\text{SD\_DQS}}$ transition and ends when the first data line becomes invalid.

Figure 13 shows a DDR SDRAM write cycle.

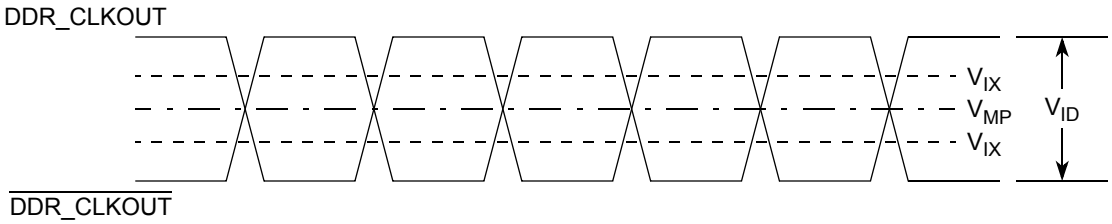


Figure 12. DDR_CLKOUT and $\overline{\text{DDR\_CLKOUT}}$ Crossover Timing

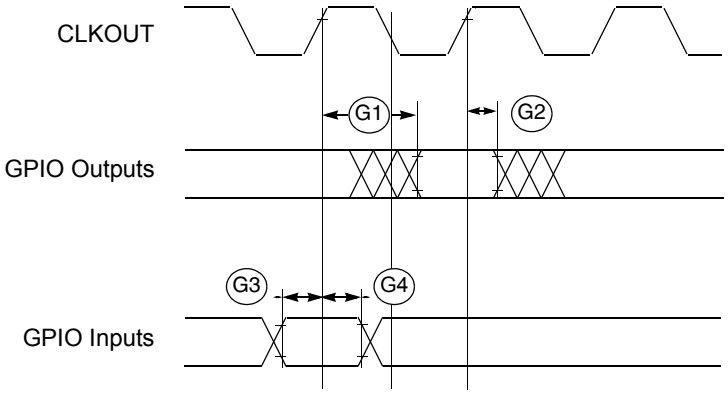


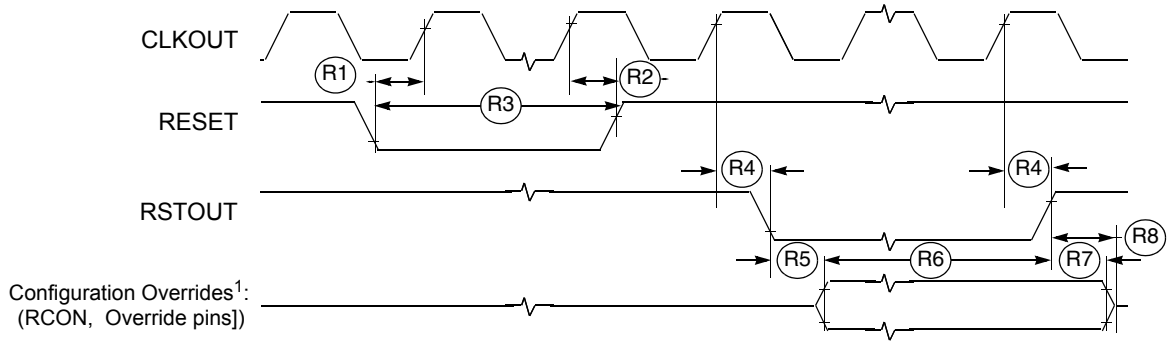
Figure 15. GPIO Timing

8.10 Reset and Configuration Override Timing

Table 17. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1 x t_{CYC}	ns

1 All AC timing is shown with respect to 50% OV_{DD} levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.



1. Refer to the Coldfire Integration Module (CIM) section for more information.

RESET and Configuration Override Timing

8.11 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 5.0 V or 3.3 V.

8.11.1 MII Receive Signal Timing (FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER, and FEC*n*_RXCLK)

The receiver functions correctly up to a FEC*n*_RXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC*n*_RXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER to FEC*n*_RXCLK setup	5	—	ns
M2	FEC*n*_RXCLK to FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER hold	5	—	ns
M3	FEC*n*_RXCLK pulse width high	35%	65%	FEC*n*_RXCLK period
M4	FEC*n*_RXCLK pulse width low	35%	65%	FEC*n*_RXCLK period

Figure 16 shows MII receive signal timings listed in Table 18.

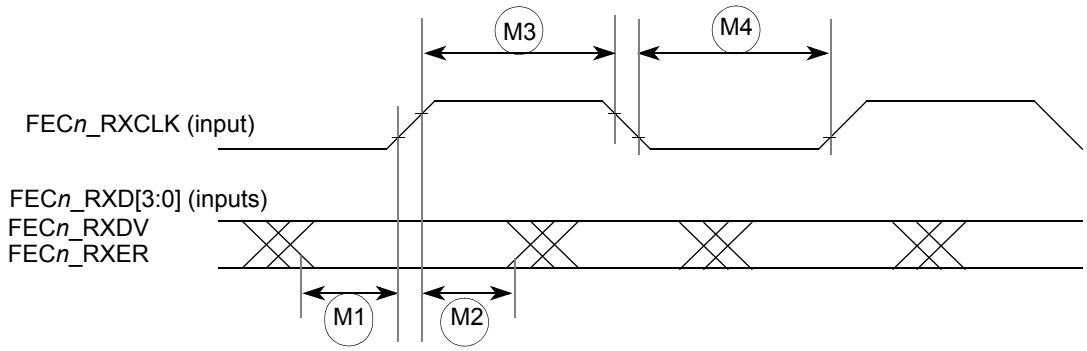


Figure 16. MII Receive Signal Timing Diagram

8.11.2 MII Transmit Signal Timing (FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER, FEC*n*_TXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC*n*_TXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC*n*_TXCLK frequency.

Table 19. MII Transmit Channel Timing

Num	Characteristic	Min	Max	Unit
M5	FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER invalid	5	—	ns
M6	FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER valid	—	25	ns
M7	FEC*n*_TXCLK pulse width high	35%	65%	FEC*n*_TXCLK period
M8	FEC*n*_TXCLK pulse width low	35%	65%	FEC*n*_TXCLK period

Figure 17 shows MII transmit signal timings listed in Table 19.

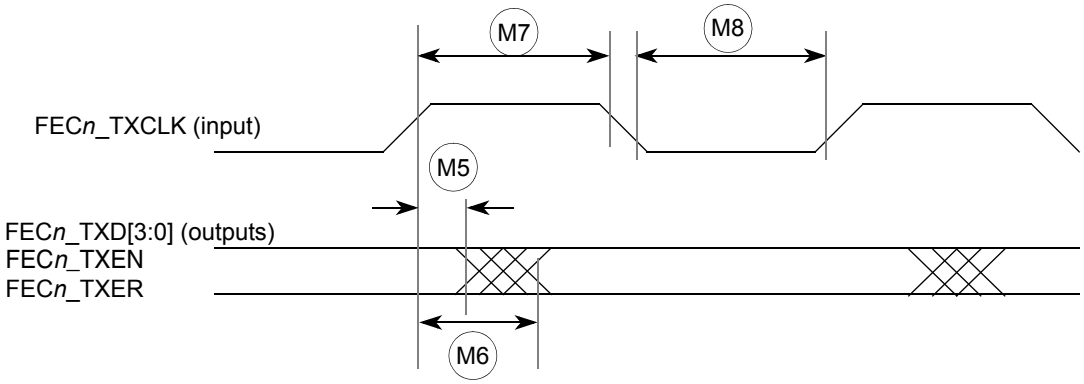


Figure 17. MII Transmit Signal Timing Diagram

8.11.3 MII Async Inputs Signal Timing (FEC*n*_CRS and FEC*n*_COL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Asynchronous Input Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC*n*_CRS, FEC*n*_COL minimum pulse width	1.5	—	FEC*n*_TXCLK period

Figure 18 shows MII asynchronous input timings listed in Table 20.

Figure 18. MII Async Inputs Timing Diagram

8.12 I²C Input/Output Timing Specifications

Table 23 lists specifications for the I²C input timing parameters shown in Figure 21.

Table 23. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2 x t_{CYC}	—	ns
I2	Clock low period	8 x t_{CYC}	—	ns
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4 x t_{CYC}	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2 x t_{CYC}	—	ns
I9	Stop condition setup time	2 x t_{CYC}	—	ns

Table 24 lists specifications for the I²C output timing parameters shown in Figure 21.

Table 24. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6 x t_{CYC}	—	ns
I2 [1]	Clock low period	10 x t_{CYC}	—	ns
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7 x t_{CYC}	—	ns
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10 x t_{CYC}	—	ns
I7 [1]	Data setup time	2 x t_{CYC}	—	ns
I8 [1]	Start condition setup time (for repeated start condition only)	20 x t_{CYC}	—	ns
I9 [1]	Stop condition setup time	10 x t_{CYC}	—	ns

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 24. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 24 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

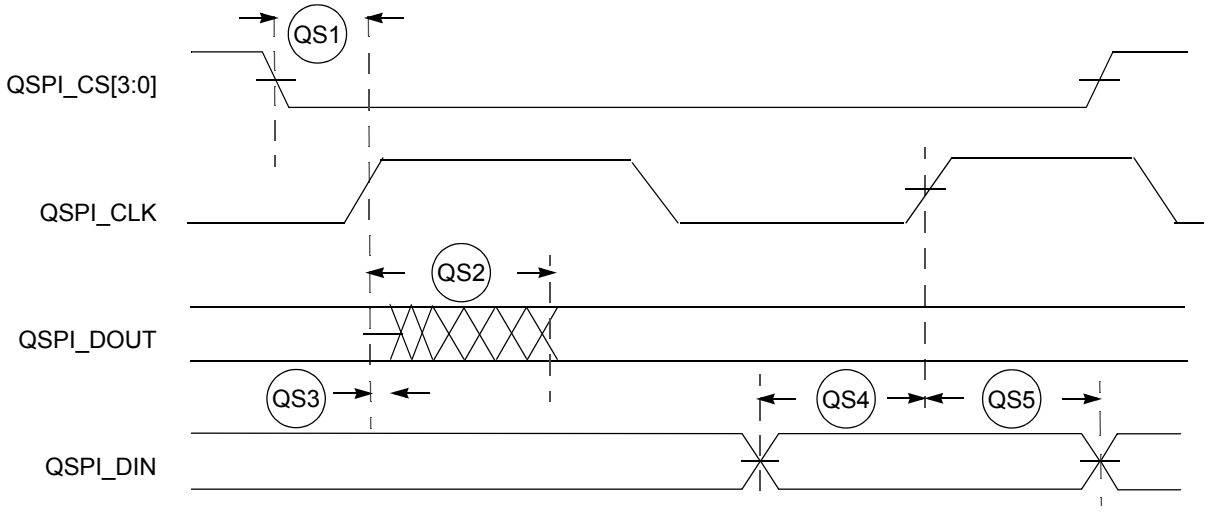


Figure 22. QSPI Timing

8.15 JTAG and Boundary Scan Timing

Table 27. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4 x t_{CYC}	—	ns
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

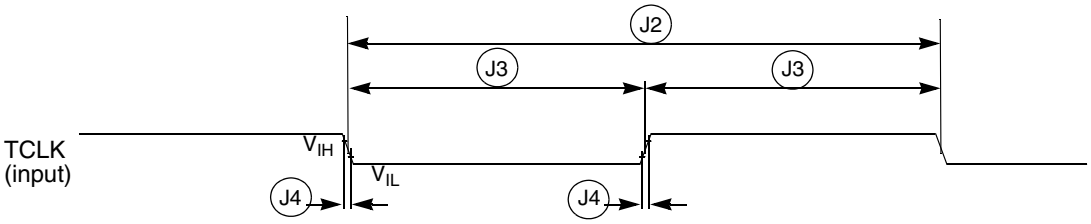


Figure 23. Test Clock Input Timing

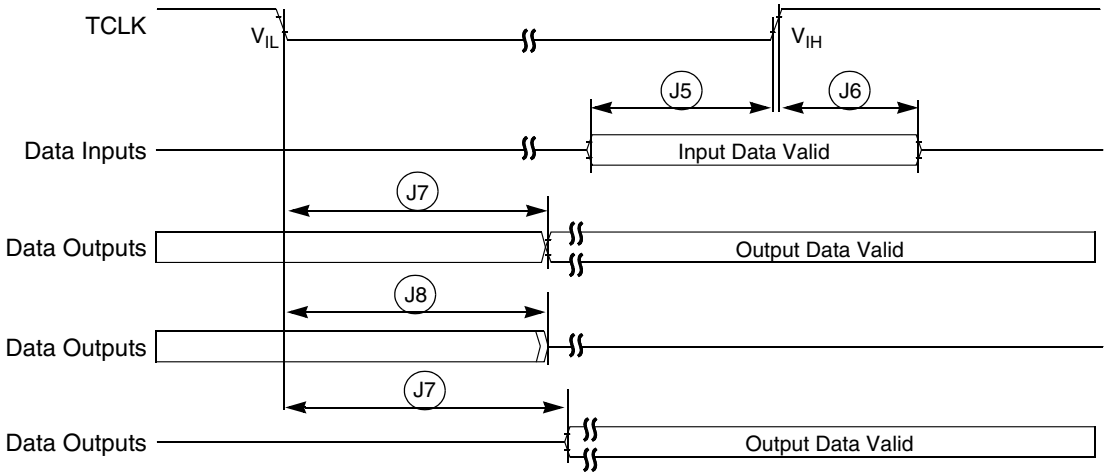


Figure 24. Boundary Scan (JTAG) Timing

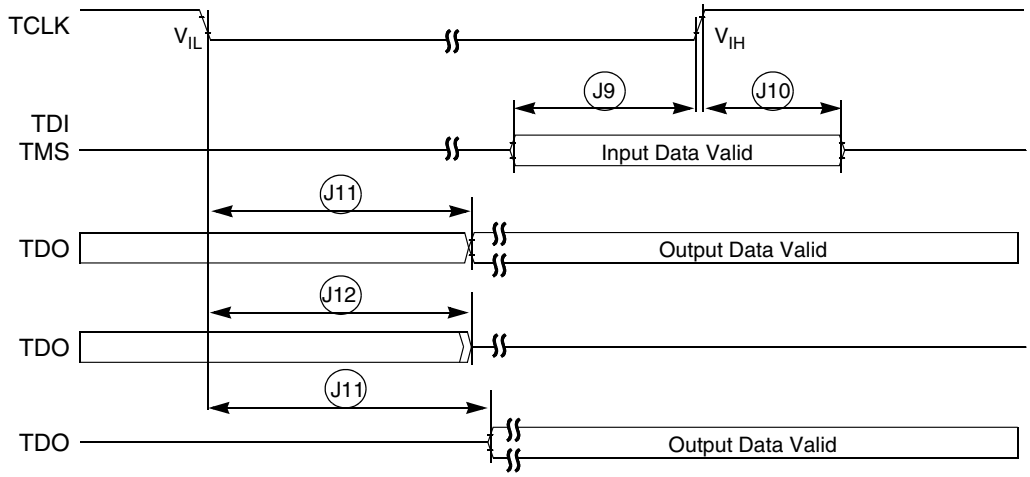


Figure 25. Test Access Port Timing

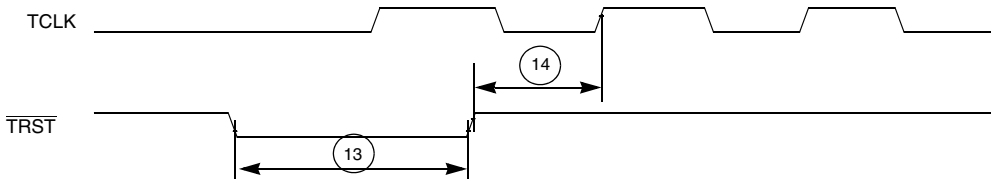


Figure 26. TRST Timing

8.16 Debug AC Timing Specifications

Table 28 lists specifications for the debug AC timing parameters shown in Figure 28.

Table 28. Debug AC Timing Specification

Num	Characteristic	166 MHz		Units
		Min	Max	
D0	PSTCLK cycle time	—	0.5	t_{CYC}
D1	PST, DDATA to PSTCLK setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.0	—	ns
D3	DSI-to-DSCLK setup	1 x t_{CYC}	—	ns
D4 [1]	DSCLK-to-DSO hold	4 x t_{CYC}	—	ns
D5	DSCLK cycle time	5 x t_{CYC}	—	ns
D6	$\overline{BKPT}$ input data setup time to PSTCLK Rise	4	—	ns
D7	$\overline{BKPT}$ input data hold time to PSTCLK Rise	1.5	—	ns
D8	PSTCLK high to $\overline{BKPT}$ high Z	0.0	10.0	ns

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

Figure 27 shows real-time trace timing for the values in Table 28.

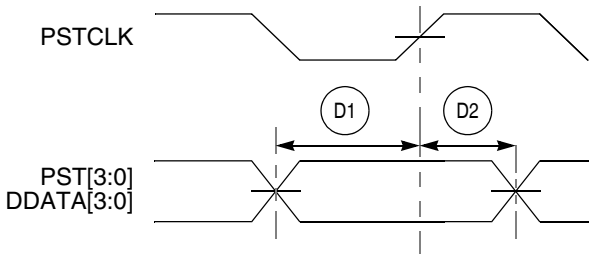


Figure 27. Real-Time Trace AC Timing

Figure 28 shows BDM serial port AC timing for the values in Table 28.

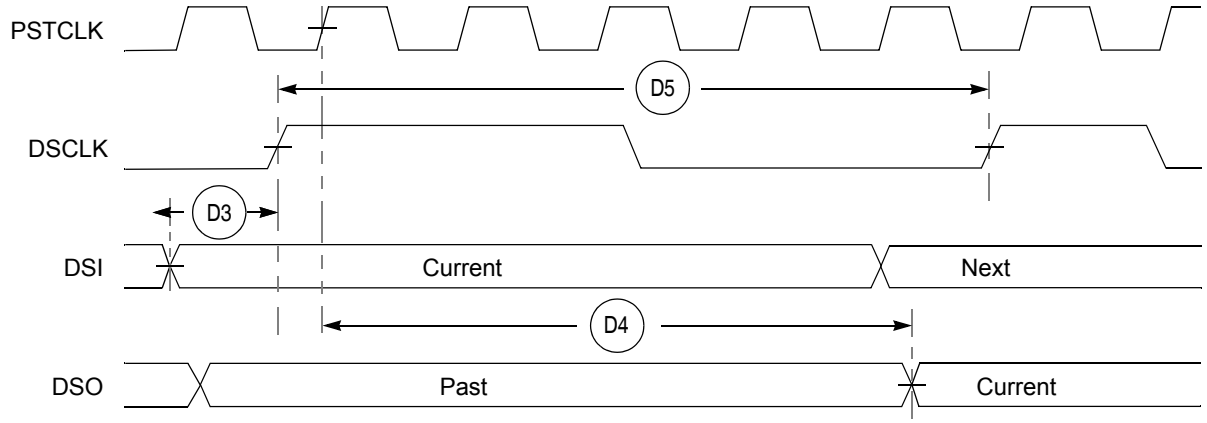


Figure 28. BDM Serial Port AC Timing