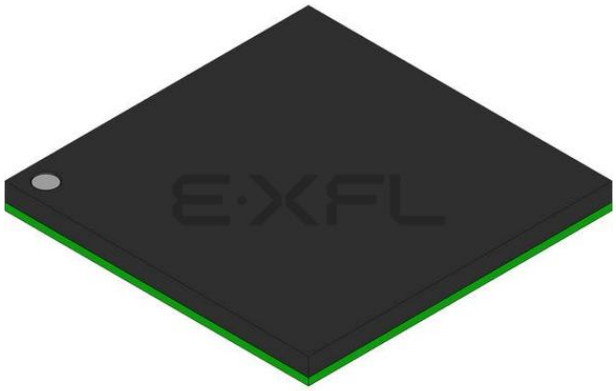


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, WDT
Number of I/O	61
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5274lvm166j

2 Block Diagram

The superset device in the MCF5275 family comes in a 256 Mold Array Plastic Ball Grid Array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5275, the superset device.

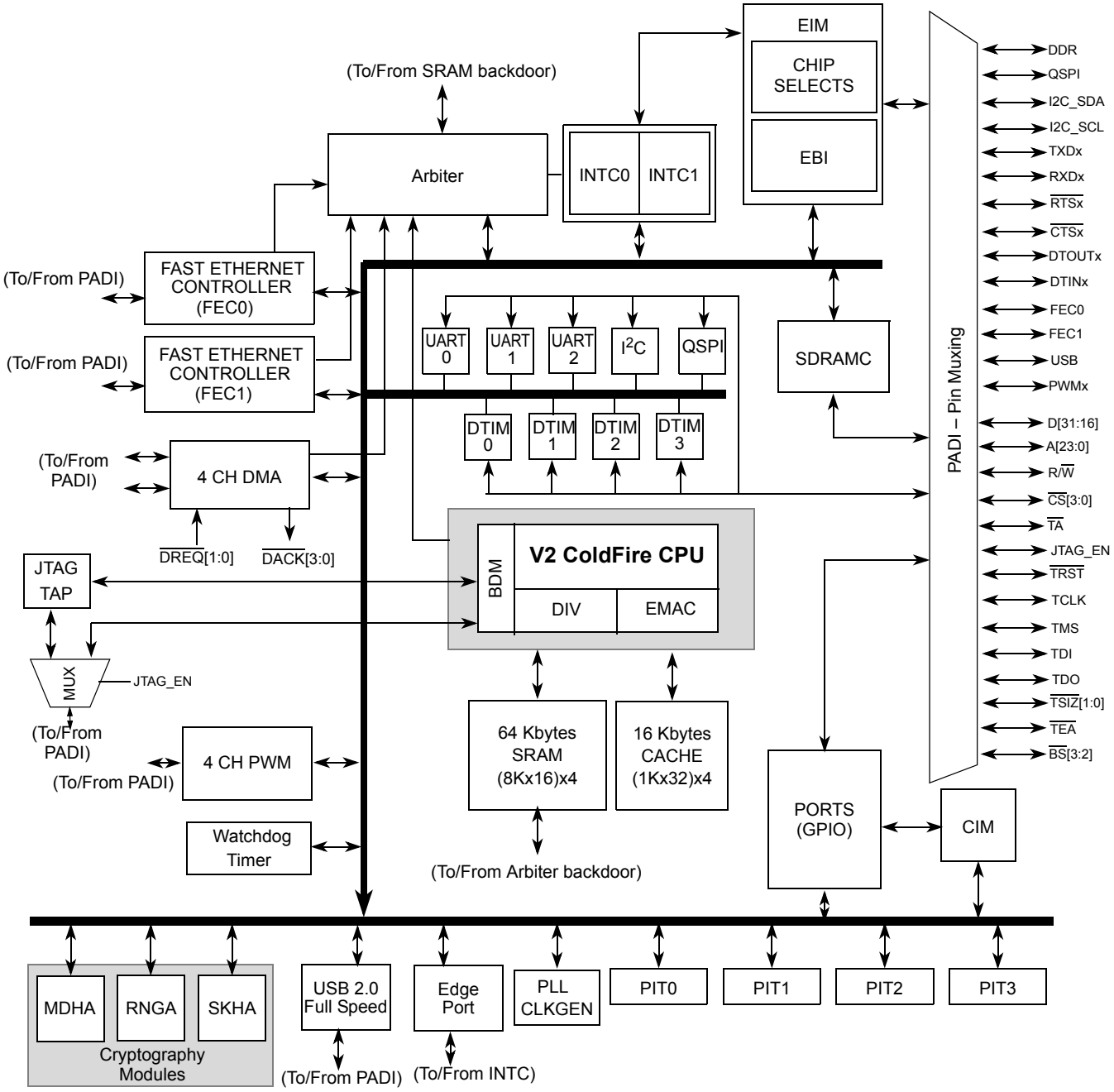


Figure 1. MCF5275 Block Diagram

3 Features

For a detailed feature list see the *MCF5275 Reference Manual* (MCF5275RM).

4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF5275 signals, consult the *MCF5275 Reference Manual* (MCF5275RM).

Table 2 lists the signals for the MCF5275 in functional group order. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts," for package diagrams.

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 2. MCF5274 and MCF5275 Signal Information and Muxing

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
Reset						
$\overline{\text{RESET}}$	—	—	—	I	N15	K12
$\overline{\text{RSTOUT}}$	—	—	—	O	N14	L12
Clock						
EXTAL	—	—	—	I	L16	M14
XTAL	—	—	—	O	M16	N14
CLKOUT	—	—	—	O	T12	P9
Mode Selection						
CLKMOD[1:0]	—	—	—	I	N13, P13	M11, N11
$\overline{\text{RCON}}$	—	—	—	I	P8	M6
External Memory Interface and Ports						
A[23:21]	PADDR[7:5]	$\overline{\text{CS}}$[6:4]	—	O	A11, B11, C11	A8, B8, C8
A[20:0]	—	—	—	O	A12, B12, C12, A13, B13, C13, A14, B14, C14, B15, C15, B16, C16, D14, D15, E14:16, F14:16	B9, D9, C9, C10, B10, A11, C11, B11, A12, D11, C12, B13, C13, D12, E11, D13, E12, F11, D14, E13, F13

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
D[31:16]	—	—	—	O	M1, N1, N2, N3, P1, P2, R1, R2, P3, R3, T3, N4, P4, R4, T4, N5	J3, L1, K2, K3, M1, L2, L3, L4, K4, J4, M2, N1, N2, M3, M4, N3
$\overline{BS}$[3:2]	$\overline{PBS}$[3:2]	$\overline{CAS}$[3:2]	—	O	M3, R5	K1, L5
$\overline{OE}$	PBUSCTL[7]	—	—	O	K1	H4
$\overline{TA}$	PBUSCTL[6]	—	—	I	L13	K14
$\overline{TEA}$	PBUSCTL[5]	$\overline{DREQ1}$	—	I	T8	—
R/$\overline{W}$	PBUSCTL[4]	—	—	O	P7	L6
TSIZ1	PBUSCTL[3]	DACK1	—	O	D16	B14
TSIZ0	PBUSCTL[2]	DACK0	—	O	G16	E14
$\overline{TS}$	PBUSCTL[1]	DACK2	—	O	L4	H2
$\overline{TIP}$	PBUSCTL[0]	$\overline{DREQ0}$	—	O	P6	—
Chip Selects						
$\overline{CS}$[7:1]	PCS[7:1]	—	—	O	D10:13, E13, F13, N7	D8, A9, A10, D10, B12, C14, P4
$\overline{CS0}$	—	—	—	O	R6	N5
DDR SDRAM Controller						
DDR_CLKOUT	—	—	—	O	T7	P6
$\overline{DDR\_CLKOUT}$	—	—	—	O	T6	P5
$\overline{SD\_CS}$[1:0]	PSDRAM[7:6]	$\overline{CS}$[3:2]	—	O	M2, T5	H3, M5
$\overline{SD\_SRAS}$	PSDRAM[5]	—	—	O	L2	H1
$\overline{SD\_SCAS}$	PSDRAM[4]	—	—	O	L1	G3
$\overline{SD\_WE}$	PSDRAM[3]	—	—	O	K2	G4
SD_A10	—	—	—	O	N6	N4
$\overline{SD\_DQS}$[3:2]	PSDRAM[2:1]	—	—	I/O	M4, P5	J2, P3
SD_CKE	PSDRAM[0]	—	—	O	L3	J1
SD_VREF	—	—	—	I	A15, T2	A13, P2
External Interrupts Port						
$\overline{IRQ}$[7:5]	PIRQ[7:5]	—	—	I	G13, H16, H15	F14, G13, G14
$\overline{IRQ}$[4]	PIRQ[4]	$\overline{DREQ2}$	—	I	H14	H11
$\overline{IRQ}$[3:2]	PIRQ[3:2]	$\overline{DREQ}$[3:2]	—	I	J14, J13	H14, H12

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
I²C						
I2C_SDA	PFECI2C[1]	U2RXD	—	I/O	B10	B7
I2C_SCL	PFECI2C[0]	U2TXD	—	I/O	C10	A7
DMA						
DACK[3:0] and $\overline{\text{DREQ}}$[3:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: PCS3/PWM3 for DACK3, PCS2/PWM2 for DACK2, TSIZ1 for DACK1, TSIZ0 for DACK0, $\overline{\text{IRQ3}}$ for $\overline{\text{DREQ3}}$, $\overline{\text{IRQ2}}$ and $\overline{\text{TA}}$ for $\overline{\text{DREQ2}}$, $\overline{\text{TEA}}$ for $\overline{\text{DREQ1}}$, and $\overline{\text{TIP}}$ for $\overline{\text{DREQ0}}$.					—	—
QSPI						
QSPI_CS[3:2]	PQSPI[6:5]	PWM[3:2]	DACK[3:2]	O	R13, N12	P10, N9
QSPI_CS1	PQSPI[4]	—	—	O	T14	N10
QSPI_CS0	PQSPI[3]	—	—	O	P12	M9
QSPI_CLK	PQSPI[2]	I2C_SCL	—	O	T15	L11
QSPI_DIN	PQSPI[1]	I2C_SDA	—	I	T13	M10
QSPI_DOUT	PQSPI[0]	—	—	O	R12	L10
UARTs						
U2RXD	PUARTH[3]	—	—	I	T9	—
U2TXD	PUARTH[2]	—	—	O	R9	—
$\overline{\text{U2CTS}}$	PUARTH[1]	PWM1	—	I	P9	—
$\overline{\text{U2RTS}}$	PUARTH[0]	PWM0	—	O	R8	—
U1RXD	PUARTL[7]	—	—	I	A9	A6
U1TXD	PUARTL[6]	—	—	O	B9	D7
$\overline{\text{U1CTS}}$	PUARTL[5]	—	—	I	C9	C7
$\overline{\text{U1RTS}}$	PUARTL[4]	—	—	O	D9	B6
U0RXD	PUARTL[3]	—	—	I	A8	A4
U0TXD	PUARTL[2]	—	—	O	B8	A5
$\overline{\text{U0CTS}}$	PUARTL[1]	—	—	I	C8	C6
$\overline{\text{U0RTS}}$	PUARTL[0]	—	—	O	D7	B5
USB						
USB_SPEED	PUSBH[0]	—	—	I/O	G14	G11
USB_CLK	PUSBL[7]	—	—	I	G15	F12

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
USB_RN	PUSBL[6]	—	—	I	J16	H13
USB_RP	PUSBL[5]	—	—	I	J15	J11
USB_RXD	PUSBL[4]	—	—	I	L15	L14
USB_SUSP	PUSBL[3]	—	—	O	M13	N13
USB_TN	PUSBL[2]	—	—	O	K14	J14
USB_TP	PUSBL[1]	—	—	O	K15	J12
USB_TXEN	PUSBL[0]	—	—	O	L14	K13
Timers (and PWMs)						
DT3IN	PTIMERH[3]	DT3OUT	$\overline{\text{U2RTS}}$	I	J4	G2
DT3OUT	PTIMERH[2]	PWM3	$\overline{\text{U2CTS}}$	O	K3	G1
DT2IN	PTIMERH[1]	DT2OUT	—	I	J2	F3
DT2OUT	PTIMERH[0]	PWM2	—	O	J3	F4
DT1IN	PTIMERL[3]	DT1OUT	—	I	H1	F1
DT1OUT	PTIMERL[2]	PWM1	—	O	H2	F2
DT0IN	PTIMERL[1]	DT0OUT	—	I	H3	E1
DT0OUT	PTIMERL[0]	PWM0	—	O	G3	E2
BDM/JTAG[2]						
DSCLK	—	$\overline{\text{TRST}}$	—	I	P14	P13
PSTCLK	—	TCLK	—	O	P16	P12
$\overline{\text{BKPT}}$	—	TMS	—	I	R15	N12
DSI	—	TDI	—	I	R16	M12
DSO	—	TDO	—	O	P15	K11
JTAG_EN	—	—	—	I	R14	P11
DDATA[3:0]	—	—	—	O	P10, N10, P11, N11	M7, N7, P8, L9
PST[3:0]	—	—	—	O	T10, R10, T11, R11	P7, L8, M8, N8
Test						
TEST	—	—	—	I	N9	N6
PLL_TEST	—	—	—	I	M14	—
Power Supplies						
VDDPLL	—	—	—	I	M15	M13

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
VSSPLL	—	—	—	I	K16	L13
VSS	—	—	—	I	A1, A10, A16, E5, E12, F6, F11, G7:10, H7:10, J1, J7:10, K7:10, L6, L11, M5, N16, R7, T1, T16	F7, F8, G6:9, H6:9, J7, J8
OVDD	—	—	—	I	E6:8, F5, F7, F8, G5, G6, H5, H6, J11, J12, K11, K12, L9, L10, L12, M9:11	E5:7, F5, F6, H10, J9, J10, K8:10
VDD	—	—	—	I	D8, H13, K4, N8	D6, G5, G12, L7
SD_VDD	—	—	—	I	E9:11, F9, F10, F12, G11, G12, H11, H12, J5, J6, K5, K6, L5, L7, L8, M6, M7, M8	E8:10, F9, F10, G10, H5, J5, J6, K5:7

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5275.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33uF, 0.1 µF, and 0.01 µF across each power supply

5.7 Interface Recommendations

5.7.1 DDR SDRAM Controller

5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

Table 3. Synchronous DRAM Signal Connections

Signal	Description
$\overline{\text{SD\_SRAS}}$	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SDRAM\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals.
$\overline{\text{SD\_SCAS}}$	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM.
$\overline{\text{SD\_WE}}$	DRAM read/write. Asserted for write operations and negated for read operations.
$\overline{\text{SD\_CS}}$[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF5275. One $\overline{\text{SDRAM\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
$\overline{\text{BS}}$[3:2]	Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:2] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
DDR_CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5275 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

The FEC supports an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF5275 Pin
Transmit clock	FEC*n*_TXCLK
Transmit enable	FEC*n*_TXEN
Transmit data	FEC*n*_TXD[3:0]
Transmit error	FEC*n*_TXER

6 Mechanicals/Pinouts

6.1 256 MAPBGA Pinout

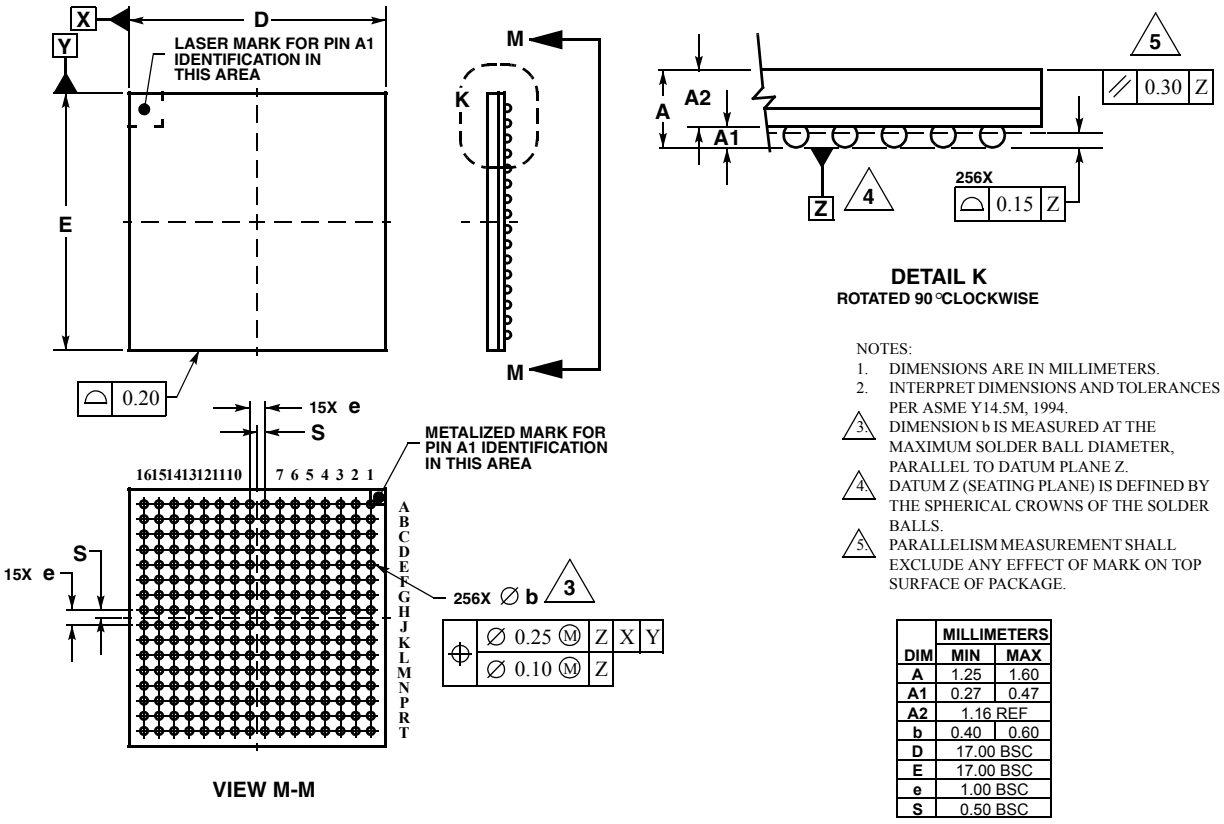
Figure 3 is a consolidated MCF5274/75 pinout for the 256 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FEC1_ RXD1	FEC1_ RXDV	FEC1_ CRS	FEC1_ COL	FEC0_ COL	FEC0_ MDIO	U0RXD	U1RXD	VSS	A23	A20	A17	A14	SD_ VREF	VSS	A
B	FEC1_ RXD3	FEC1_ RXD2	FEC1_ RXD0	FEC1_ RXCLK	FEC0_ RXDV	FEC0_ RXCLK	FEC0_ MDC	U0TXD	U1TXD	I2C_ SDA	A22	A19	A16	A13	A11	A9	B
C	FEC1_ TXCLK	FEC1_ RXER	FEC0_ TXCLK	FEC0_ RXER	FEC0_ RXD2	FEC0_ RXD0	FEC0_ CRS	$\overline{\text{U0CTS}}$	$\overline{\text{U1CTS}}$	I2C_ SCL	A21	A18	A15	A12	A10	A8	C
D	FEC1_ TXER	FEC1_ TXEN	FEC0_ TXER	FEC0_ TXEN	FEC0_ RXD3	FEC0_ RXD1	$\overline{\text{U0RTS}}$	VDD	$\overline{\text{U1RTS}}$	$\overline{\text{CS7}}$	$\overline{\text{CS6}}$	$\overline{\text{CS5}}$	$\overline{\text{CS4}}$	A7	A6	TSIZ1	D
E	FEC1_ TXD3	FEC1_ TXD2	FEC0_ TXD3	NC	VSS	OVDD	OVDD	OVDD	SD_VDD	SD_VDD	SD_VDD	VSS	$\overline{\text{CS3}}$	A5	A4	A3	E
F	FEC1_ TXD0	FEC1_ TXD1	FEC0_ TXD2	FEC0_ TXD1	OVDD	VSS	OVDD	OVDD	SD_VDD	SD_VDD	VSS	SD_VDD	$\overline{\text{CS2}}$	A2	A1	A0	F
G	FEC1_ MDIO	FEC1_ MDC	DT0OUT	FEC0_ TXD0	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	$\overline{\text{IRQ7}}$	USB_ SPEED	USB_ CLK	TSIZ0	G
H	DT1IN	DT1OUT	DT0IN	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	VDD	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ6}}$	H
J	VSS	DT2IN	DT2OUT	DT3IN	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ3}}$	USB_RP	USB_RN	J
K	$\overline{\text{OE}}$	$\overline{\text{SD_WE}}$	DT3OUT	VDD	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\text{IRQ1}}$	USB_TN	USB_TP	VSSPLL	K
L	$\overline{\text{SD_ SCAS}}$	$\overline{\text{SD_ SRAS}}$	SD_CKE	$\overline{\text{TS}}$	SD_VDD	VSS	SD_VDD	SD_VDD	OVDD	OVDD	VSS	OVDD	$\overline{\text{TA}}$	USB_ TXEN	USB_ RXD	EXTAL	L
M	D31	$\overline{\text{SD_CS1}}$	$\overline{\text{BS3}}$	SD_DQS3	VSS	SD_VDD	SD_VDD	SD_VDD	OVDD	OVDD	OVDD	NC	USB_ SUSP	PLL_ TEST	VDDPLL	XTAL	M
N	D30	D29	D28	D20	D16	SD_A10	$\overline{\text{CS1}}$	VDD	TEST	DDATA2	DDATA0	QSPI_ CS2	CLK MOD1	$\overline{\text{RSTOUT}}$	$\overline{\text{RESET}}$	VSS	N
P	D27	D26	D23	D19	SD_DQS2	$\overline{\text{TIP}}$	R/$\overline{\text{W}}$	$\overline{\text{RCON}}$	$\overline{\text{U2CTS}}$	DDATA3	DDATA1	QSPI_ CS0	CLK MOD0	$\overline{\text{TRST}}$/ DSCLK	TDO/ DSO	TCLK/ PSTCLK	P
R	D25	D24	D22	D18	$\overline{\text{BS2}}$	$\overline{\text{CS0}}$	VSS	$\overline{\text{U2RTS}}$	U2TXD	PST2	PST0	QSPI_ DOUT	QSPI_ CS3	JTAG_ EN	TMS/ $\overline{\text{BKPT}}$	TDI/DSI	R
T	VSS	SD_ VREF	D21	D17	$\overline{\text{SD_CS0}}$	$\overline{\text{DDR_CLK OUT}}$	DDR_CLK OUT	$\overline{\text{TEA}}$	U2RXD	PST3	PST1	CLKOUT	QSPI_ DIN	QSPI_ CS1	QSPI_ CLK	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. MCF5274 and MCF5275 Pinout (256 MAPBGA)

6.2 Package Dimensions - 256 MAPBGA

Figure 6 shows MCF5275 256 MAPBGA package dimensions.



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

DIM	MILLIMETERS MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 4. 256 MAPBGA Package Dimensions

7 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5274LVM166	MCF5274L RISC Microprocessor	196 MAPBGA	166 MHz	0° to +70° C
MCF5274LCVM166				-40° to +85° C
MCF5274VM166	MCF5274 RISC Microprocessor	256 MAPBGA	166 MHz	0° to +70° C
MCF5274CVM166				-40° to +85° C
MCF5275LCVM166	MCF5275L RISC Microprocessor	196 MAPBGA	166 MHz	-40° to +85° C
MCF5275CVM166	MCF5275 RISC Microprocessor	256 MAPBGA	166 MHz	-40° to +85° C

8 Electrical Characteristics

This appendix contains electrical specification tables and reference timing diagrams for the MCF5275 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5275.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

8.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
I/O Pad Supply Voltage (3.3V)	OV_{DD}	– 0.3 to +4.0	V
Memory Interface SSTL 2.5V Pad Supply Voltage	SDV_{DD}	– 0.3 to + 2.8	V
Memory Interface SSTL 3.3V Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., V_{SS} or O V_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and O V_{DD}.

5 Power supply must maintain regulation within operating O V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > O V_{DD}) is greater than I_{DD}, the injection current may flow out of O V_{DD} and could result in external power supply going out of regulation. Ensure the external O V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock).Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

8.2 Thermal Characteristics

Table 8 lists thermal resistance values

Table 8. Thermal characteristics

Characteristic		Symbol	256MBGA	196MBGA	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	26[1,2]	32[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	23[1,2]	29[1,2]	°C/W
Junction to board		θ_{JB}	15[3]	20[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	°C/W
Junction to top of package	Natural convection	Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

Θ_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

8.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V
ESD Target for Machine Model	MM	200	V
HBM Circuit Description	R_{series}	1500	Ω
	C	100	pF
MM Circuit Description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) positive pulses negative pulses	 — —	 3 3	—
Interval of Pulses	—	1	sec

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

8.4 DC Electrical Specifications

Table 10. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	V_{DD}	1.4	1.6	V
I/O Pad Supply Voltage	OV_{DD}	3.0	3.6	V
PLL Supply Voltage	V_{DDPLL}	3.0	3.6	V
SSTL I/O Pad Supply Voltage	SDV_{DD}	2.3	2.7	V
SSTL I/O Pad Supply Voltage	SDV_{DD}	3.0	3.6	V
SSTL Memory pads reference voltage (SD V_{DD} = 2.5V)	V_{REF}	0.5 SD V_{DD}	—[2]	V
SSTL Memory pads reference voltage (SD V_{DD} = 3.3V)	V_{REF}	0.45 SD V_{DD}	—[2]	V
Input High Voltage 3.3V I/O Pads	V_{IH}	0.7 x OV_{DD}	OV_{DD} + 0.3	V
Input Low Voltage 3.3V I/O Pads	V_{IL}	V_{SS} – 0.3	0.35 x OV_{DD}	V
Output High Voltage 3.3V I/O Pads I_{OH} = –2.0 mA	V_{OH}	OV_{DD} - 0.5	—	V
Output Low Voltage 3.3V I/O Pads I_{OL} = 2.0mA	V_{OL}	—	0.5	V
Input Hysteresis 3.3V I/O Pads	V_{HYS}	0.06 x V_{DD}	—	mV
Input High Voltage SSTL 3.3V/2.5V[3]	V_{IH}	V_{REF} + 0.3	SDV_{DD} + 0.3	V
Input Low Voltage SSTL 3.3V/2.5V[3]	V_{IL}	V_{SS} - 0.3	V_{REF} - 0.3	V
Output High Voltage SSTL 3.3V/2.5V[4] I_{OH} = –5.0 mA	V_{OH}	SDV_{DD} - 0.25V	—	V
Output Low Voltage SSTL 3.3V/2.5V[4] I_{OL} = 5.0 mA	V_{OL}	—	0.35	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	-1.0	1.0	µA
High Impedance (Off-State) Leakage Current V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	-1.0	1.0	µA
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[5]	I_{APU}	-10	-130	µA
Input Capacitance [6] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

Table 10. DC Electrical Specifications[1] (continued)

Characteristic	Symbol	Min	Max	Unit
Load Capacitance[7] Low Drive Strength High Drive Strength	C_L	 — —	 25 50	pF
Core Operating Supply Current[8] Master Mode WAIT DOZE STOP	I_{DD}	 — — — —	 175 15 10 100	 mA mA mA µA
I/O Pad Operating Supply Current Master Mode Low Power Modes	OI_{DD}	 — —	 250 250	 mA µA
DC Injection Current [3, 9, 10, 11] $V_{NEGCLAMP}$ =V_{SS}– 0.3 V, $V_{POSCLAMP}$ = V_{DD} + 0.3 Single Pin Limit Total MCU Limit, Includes sum of all stressed pins	I_{IC}	 -1.0 -10	 1.0 10	mA

1 Refer to Table 11 for additional PLL specifications.

2 V_{REF} is specified as a nominal value only instead of a range, so no maximum value is listed.

3 This specification is guaranteed by design and is not 100% tested.

4 The actual V_{OH} and V_{OL} values for SSTL pads are dependent on the termination and drive strength used. The specifications numbers assume no parallel termination.

5 Refer to the MCF5274 signals chapter for pins having weak internal pull-up devices.

6 This parameter is characterized before qualification rather than 100% tested.

7 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.

8 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

9 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

10 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

11 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

8.5 Oscillator and Phase Lock Loop (PLLMRFM) Electrical Specifications

Table 11. PLL Electrical Specifications[1]

Characteristic	Symbol	Min	Max	Unit
PLL Reference Frequency Range Crystal reference External reference 1:1 Mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 25 25 83	MHz
Core frequency CLKOUT Frequency [2] External reference On-Chip PLL Frequency	f_{core} $f_{sys/2}$	 0 f_{ref} / 32	166 83 83	MHz MHz MHz
Loss of Reference Frequency [3, 5]	f_{LOR}	100	1000	kHz
Self Clocked Mode Frequency [4, 5]	f_{SCM}	TBD	TBD	MHz
Crystal Start-up Time [5, 6]	t_{cst}	—	10	ms
EXTAL Input High Voltage Crystal Mode All other modes (Dual Controller (1:1), Bypass, External)	V_{IHEXT} V_{IHEXT}	 TBD TBD	 TBD TBD	V
EXTAL Input Low Voltage Crystal Mode All other modes (Dual Controller (1:1), Bypass, External)	V_{ILEXT} V_{ILEXT}	 TBD TBD	 TBD TBD	V
XTAL Output High Voltage I_{OH} = 1.0 mA	V_{OH}	 TBD	 —	V
XTAL Output Low Voltage I_{OL} = 1.0 mA	V_{OL}	 —	 TBD	V
XTAL Load Capacitance[7]		5	30	pF
PLL Lock Time [8]	t_{lpll}	—	750	µs
Power-up To Lock Time [6, 9] With Crystal Reference Without Crystal Reference[10]	t_{lplk}	 — —	 11 750	 ms µs
1:1 Mode Clock Skew (between CLKOUT and EXTAL) [11]	t_{skew}	-1	1	ns
Duty Cycle of reference [5]	t_{dc}	40	60	% $f_{sys/2}$
Frequency un-LOCK Range	f_{UL}	-3.8	4.1	% $f_{sys/2}$
Frequency LOCK Range	f_{LCK}	-1.7	2.0	% $f_{sys/2}$
CLKOUT Period Jitter, [5, 6, 9,12, 13] Measured at $f_{sys/2}$ Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	 — —	 5 .01	% $f_{sys/2}$
Frequency Modulation Range Limit[14], [15] ($f_{sys/2}$Max must not be exceeded)	C_{mod}	0.8	2.2	% $f_{sys/2}$
ICO Frequency. $f_{ico} = f_{ref} * 2 * (MFD+2)$[16]	f_{ico}	48	83	MHz

1 All values given are initial design targets and subject to change.
2 All internal registers retain data at 0 Hz.
3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.

Table 13. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Data Outputs					
B11	CLKOUT high to data output (D[31:16]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:16]) invalid	t_{CHDOI}	1.0	—	ns
B13	CLKOUT high to data output (D[31:16]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}$, $\overline{BS}$, and $\overline{OE}$ transition after the falling edge of CLKOUT.

Read/write bus timings listed in Table 13 are shown in Figure 8, Figure 9, and Figure 10.

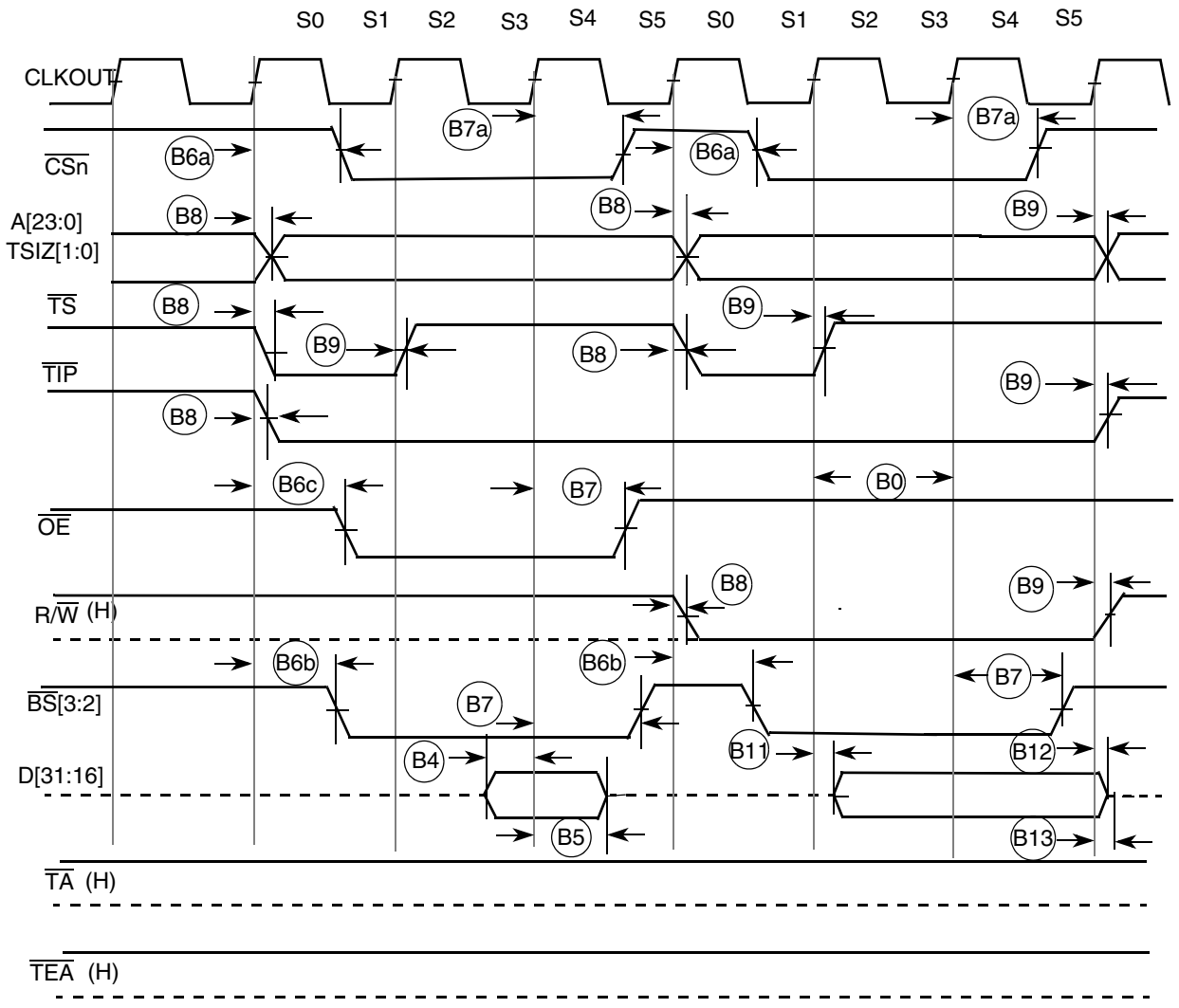


Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 13.

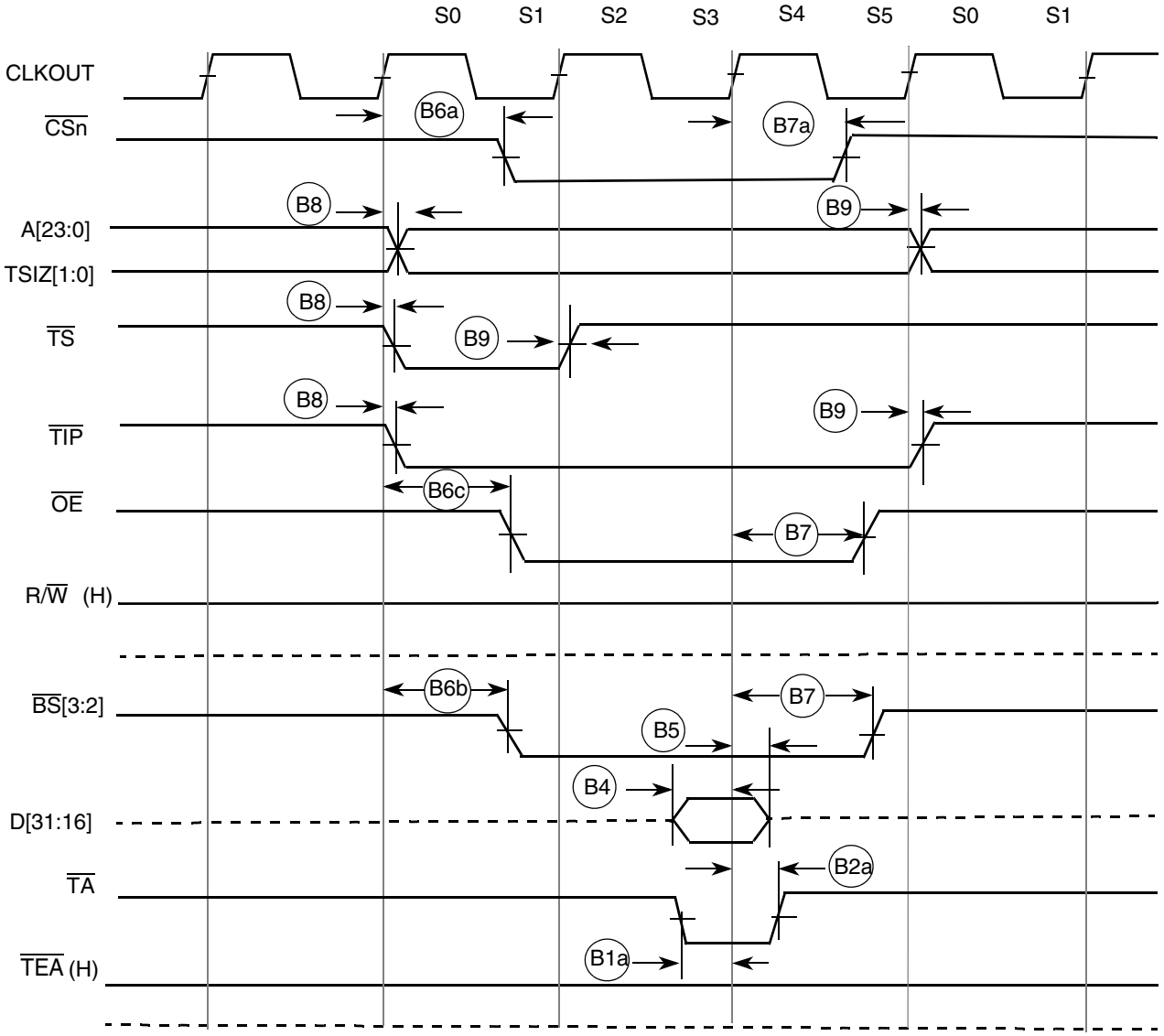


Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$

8.8 DDR SDRAM AC Timing Characteristics

The DDR SDRAM controller uses SSTL2 and I/O drivers. Class I or Class II drive strength is available and is user programmable. DDR Clock timing specifications are given in Table 14 and Figure 11.

Table 14. DDR Clock Timing Specifications[1]

Symbol	Characteristic	Min	Max	Unit
V_{MP}	Clock output mid-point voltage	1.05	1.45	V
V_{OUT}	Clock output voltage level	-0.3	SDV_{DD} + 0.3	V
V_{ID}	Clock output differential voltage (peak to peak swing)	0.7	SDV_{DD} + 0.6	V
V_{IX}	Clock crossing point voltage	1.05	1.45	V

1 SD V_{DD} is nominally 2.5V.

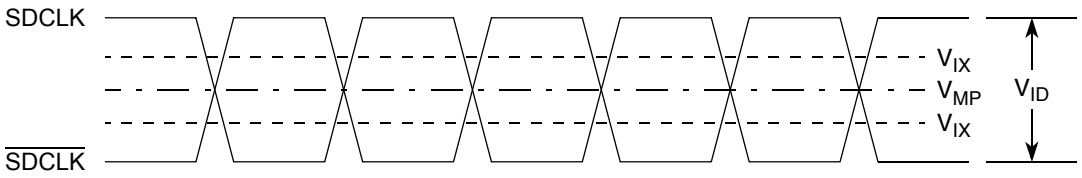


Figure 11. DDR Clock Timing Diagram

When using the DDR SDRAM controller the timing numbers in Table 15 must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the two DQS byte lanes.

Table 15. DDR Timing

NUM	Characteristic[1]	Symbol	Min	Max	Unit
	Frequency of operation[2]		TBD	83	MHz
DD1	Clock Period (DDR_CLKOUT)	t_{CK}	12	TBD	ns
DD2	Pulse Width High[3]	t_{CKH}	0.45	0.55	t_{CK}
DD3	Pulse Width Low[3]	t_{CKI}	0.45	0.55	t_{CK}
DD4	DDR_CLKOUT high to DDR address, SD_CKE, SD_CS[1:0], SD_SCAS, SD_SRAS, SD_WE valid	t_{CMV}	—	0.5 x t_{CK} + 1	ns
DD5	DDR_CLKOUT high to DDR address, SD_CKE, $\overline{\text{SD\_CS}}$, $\overline{\text{SD\_SCAS}}$, $\overline{\text{SD\_SRAS}}$, $\overline{\text{SD\_WE}}$ invalid	t_{CMH}	2	—	ns
DD6	Write command to first $\overline{\text{SD\_DQS}}$ Latching Transition	t_{DQSS}	—	1.25	t_{CK}
DD7	$\overline{\text{SD\_DQS}}$ high to Data and DM valid (write) - setup[4,5]	t_{QS}	1.5	—	ns
DD8	$\overline{\text{SD\_DQS}}$ high to Data and DM invalid (write) - hold[4]	t_{QH}	1	—	ns
DD9	$\overline{\text{SD\_DQS}}$ high to Data valid (read) - setup[6]	t_{IS}	—	1	ns
DD10	$\overline{\text{SD\_DQS}}$ high to Data invalid (read) - hold[7]	t_{IH}	0.25 x t_{CK} + 1	—	ns
DD11	$\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - setup	t_{DSS}	0.5	—	ns
DD12	$\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - hold	t_{DSH}	0.5	—	ns

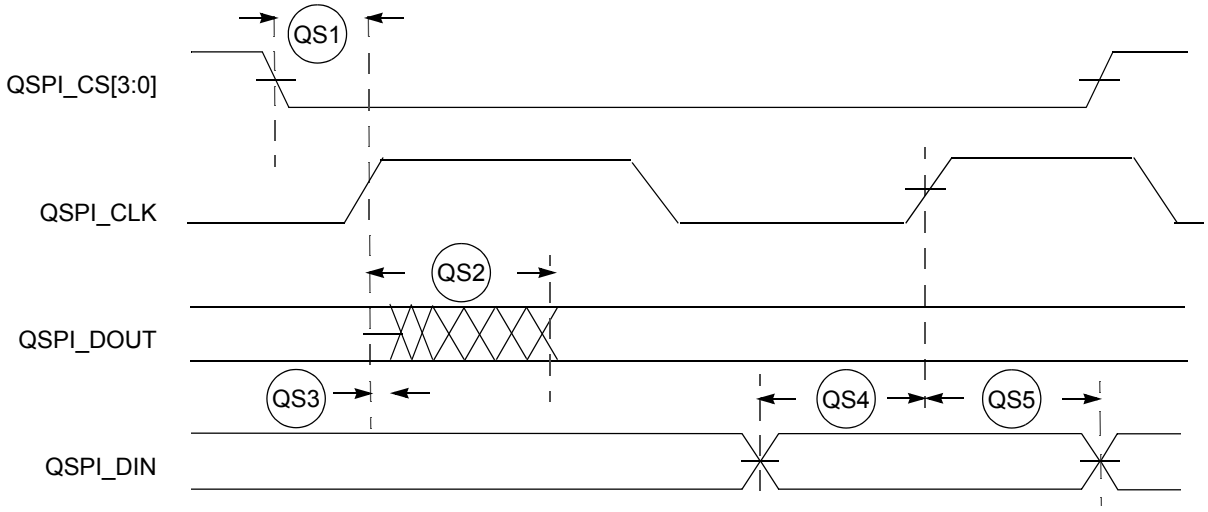


Figure 22. QSPI Timing

8.15 JTAG and Boundary Scan Timing

Table 27. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4 x t_{CYC}	—	ns
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

8.16 Debug AC Timing Specifications

Table 28 lists specifications for the debug AC timing parameters shown in Figure 28.

Table 28. Debug AC Timing Specification

Num	Characteristic	166 MHz		Units
		Min	Max	
D0	PSTCLK cycle time	—	0.5	t_{CYC}
D1	PST, DDATA to PSTCLK setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.0	—	ns
D3	DSI-to-DSCLK setup	1 x t_{CYC}	—	ns
D4 [1]	DSCLK-to-DSO hold	4 x t_{CYC}	—	ns
D5	DSCLK cycle time	5 x t_{CYC}	—	ns
D6	$\overline{BKPT}$ input data setup time to PSTCLK Rise	4	—	ns
D7	$\overline{BKPT}$ input data hold time to PSTCLK Rise	1.5	—	ns
D8	PSTCLK high to $\overline{BKPT}$ high Z	0.0	10.0	ns

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

Figure 27 shows real-time trace timing for the values in Table 28.

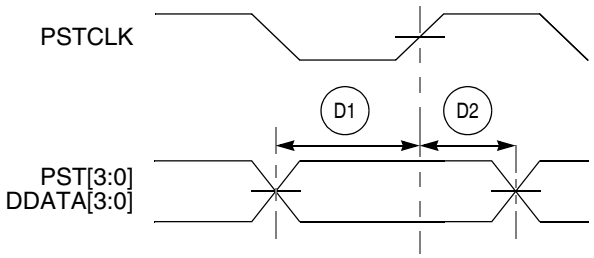


Figure 27. Real-Time Trace AC Timing

Figure 28 shows BDM serial port AC timing for the values in Table 28.

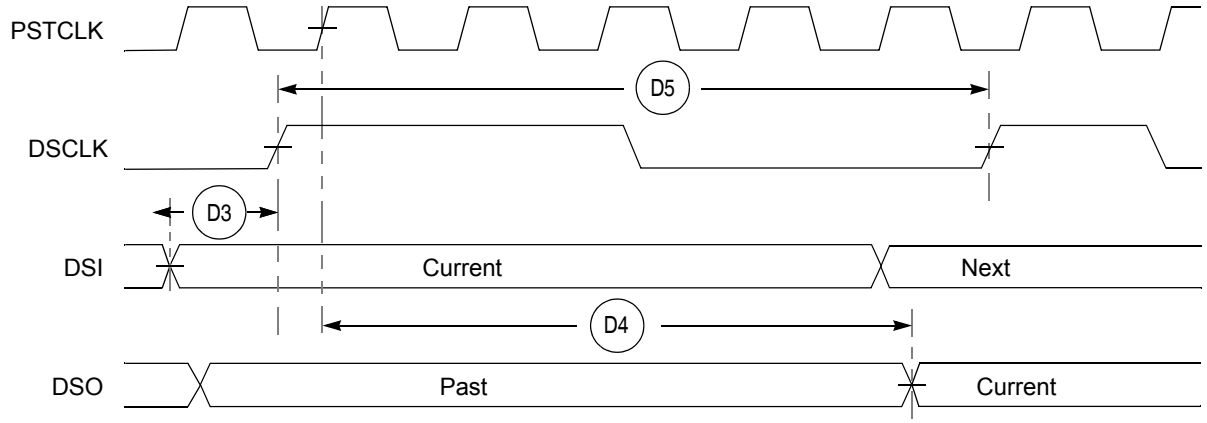


Figure 28. BDM Serial Port AC Timing