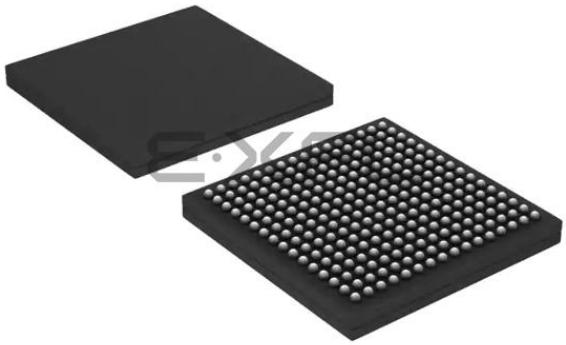

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, WDT
Number of I/O	69
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5274vm166

In addition, the MCF5275 family features an enhanced multiply accumulate unit (EMAC), large on-chip memory (64 Kbytes SRAM, 16 Kbytes configurable cache), and a 16-bit DDR SDRAM memory controller.

These devices are ideal for cost-sensitive applications requiring significant control processing for file management, connectivity, data buffering, and user interface, as well as signal processing in a variety of key markets such as security, imaging, networking, gaming, and medical. This leading package of integration and high performance allows fast time to market through easy code reuse and extensive third party tool support.

To locate any published errata or updates for this document, refer to the ColdFire products website at http://www.freescale.com/coldfire.

1 MCF5275 Family Configurations

Table 1. MCF5275 Family Configurations

Module	MCF5274L	MCF5275L	MCF5274	MCF5275
ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•
System Clock	up to 166 MHz			
Performance (Dhrystone 2.1 MIPS)	up to 159			
Instruction/Data Cache	16 Kbytes (configurable)			
Static RAM (SRAM)	64 Kbytes			
Interrupt Controllers (INTC)	2	2	2	2
Edge Port Module (EPORT)	•	•	•	•
External Interface Module (EIM)	•	•	•	•
4-channel Direct-Memory Access (DMA)	•	•	•	•
DDR SDRAM Controller	•	•	•	•
Fast Ethernet Controller (FEC)	1	1	2	2
Watchdog Timer Module (WDT)	•	•	•	•
4-channel Programmable Interval Timer Module (PIT)	•	•	•	•
32-bit DMA Timers	4	4	4	4
USB	•	•	•	•
QSPI	•	•	•	•
UART(s)	3	3	3	3
I^2C	•	•	•	•
PWM	4	4	4	4
General Purpose I/O Module (GPIO)	•	•	•	•
CIM = Chip Configuration Module + Reset Controller Module	•	•	•	•
Debug BDM	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•
Hardware Encryption	—	•	—	•
Package	196 MAPBGA		256 MAPBGA	

2 Block Diagram

The superset device in the MCF5275 family comes in a 256 Mold Array Plastic Ball Grid Array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5275, the superset device.

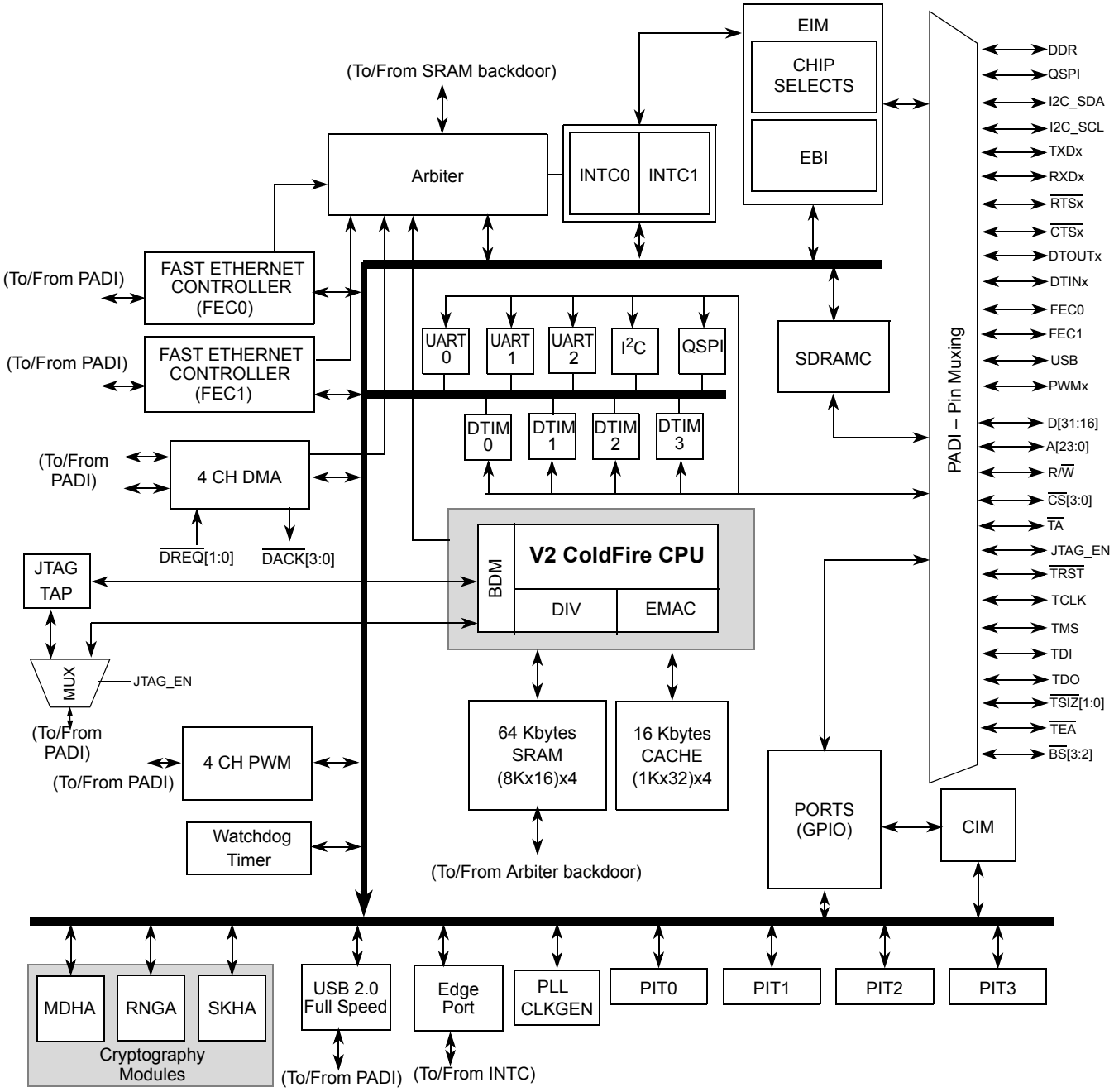


Figure 1. MCF5275 Block Diagram

3 Features

For a detailed feature list see the *MCF5275 Reference Manual* (MCF5275RM).

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
VSSPLL	—	—	—	I	K16	L13
VSS	—	—	—	I	A1, A10, A16, E5, E12, F6, F11, G7:10, H7:10, J1, J7:10, K7:10, L6, L11, M5, N16, R7, T1, T16	F7, F8, G6:9, H6:9, J7, J8
OVDD	—	—	—	I	E6:8, F5, F7, F8, G5, G6, H5, H6, J11, J12, K11, K12, L9, L10, L12, M9:11	E5:7, F5, F6, H10, J9, J10, K8:10
VDD	—	—	—	I	D8, H13, K4, N8	D6, G5, G12, L7
SD_VDD	—	—	—	I	E9:11, F9, F10, F12, G11, G12, H11, H12, J5, J6, K5, K6, L5, L7, L8, M6, M7, M8	E8:10, F9, F10, G10, H5, J5, J6, K5:7

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

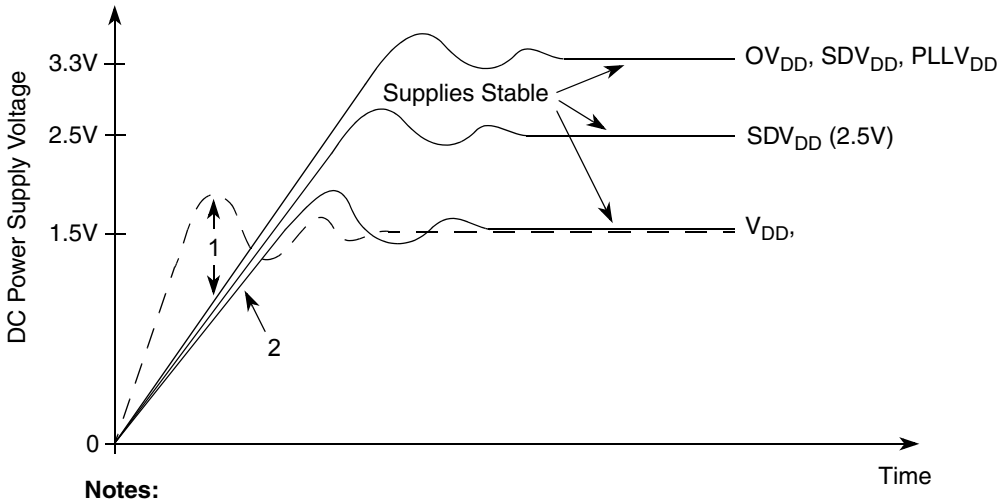
- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5275.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33uF, 0.1 µF, and 0.01 µF across each power supply

5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O V_{DD} (OV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} ($PLLV_{DD}$), and Core V_{DD} (V_{DD}).



Notes:
1. VDD should not exceed OVDD, SDVDD or PLLVDD by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/SDVDD/PLLVDD up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, SDVDD, VDD, or PLLVDD) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 2. Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and OV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and OV_{DD} are specified relative to V_{DD}.

5.2.1.1 Power Up Sequence

If OV_{DD}/SDV_{DD} are powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD}/SDV_{DD} powers up before V_{DD} must powered up. V_{DD} should not lead the OV_{DD}, SDV_{DD}, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or high current will be in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 µs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 µs or slower rise time for all supplies.
2. V_{DD}/$PLLV_{DD}$ and OV_{DD}/SDV_{DD} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD}/SD V_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

6 Mechanicals/Pinouts

6.1 256 MAPBGA Pinout

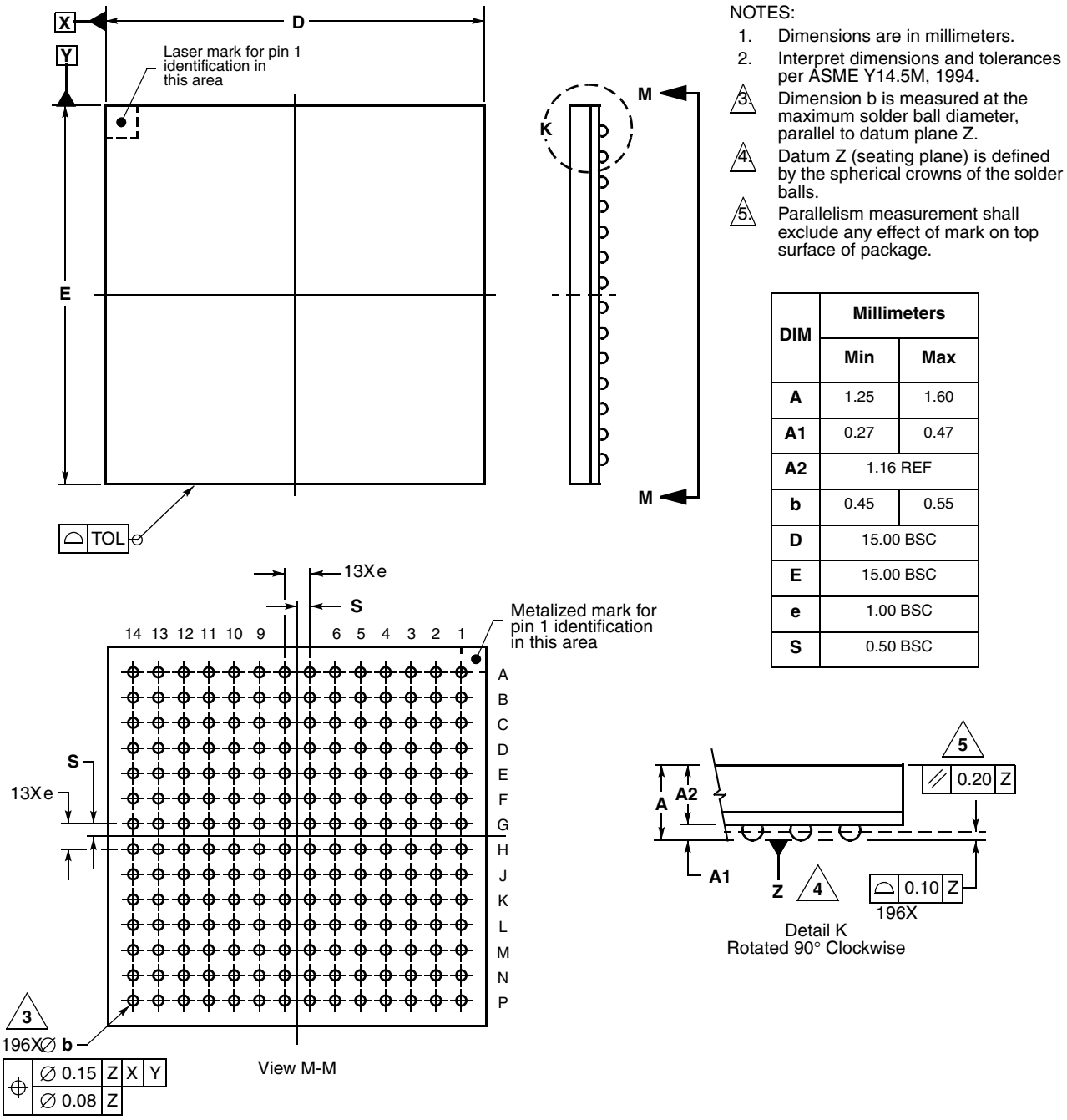
Figure 3 is a consolidated MCF5274/75 pinout for the 256 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FEC1_ RXD1	FEC1_ RXDV	FEC1_ CRS	FEC1_ COL	FEC0_ COL	FEC0_ MDIO	U0RXD	U1RXD	VSS	A23	A20	A17	A14	SD_ VREF	VSS	A
B	FEC1_ RXD3	FEC1_ RXD2	FEC1_ RXD0	FEC1_ RXCLK	FEC0_ RXDV	FEC0_ RXCLK	FEC0_ MDC	U0TXD	U1TXD	I2C_ SDA	A22	A19	A16	A13	A11	A9	B
C	FEC1_ TXCLK	FEC1_ RXER	FEC0_ TXCLK	FEC0_ RXER	FEC0_ RXD2	FEC0_ RXD0	FEC0_ CRS	$\overline{\text{U0CTS}}$	$\overline{\text{U1CTS}}$	I2C_ SCL	A21	A18	A15	A12	A10	A8	C
D	FEC1_ TXER	FEC1_ TXEN	FEC0_ TXER	FEC0_ TXEN	FEC0_ RXD3	FEC0_ RXD1	$\overline{\text{U0RTS}}$	VDD	$\overline{\text{U1RTS}}$	$\overline{\text{CS7}}$	$\overline{\text{CS6}}$	$\overline{\text{CS5}}$	$\overline{\text{CS4}}$	A7	A6	TSIZ1	D
E	FEC1_ TXD3	FEC1_ TXD2	FEC0_ TXD3	NC	VSS	OVDD	OVDD	OVDD	SD_VDD	SD_VDD	SD_VDD	VSS	$\overline{\text{CS3}}$	A5	A4	A3	E
F	FEC1_ TXD0	FEC1_ TXD1	FEC0_ TXD2	FEC0_ TXD1	OVDD	VSS	OVDD	OVDD	SD_VDD	SD_VDD	VSS	SD_VDD	$\overline{\text{CS2}}$	A2	A1	A0	F
G	FEC1_ MDIO	FEC1_ MDC	DT0OUT	FEC0_ TXD0	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	$\overline{\text{IRQ7}}$	USB_ SPEED	USB_ CLK	TSIZ0	G
H	DT1IN	DT1OUT	DT0IN	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	VDD	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ6}}$	H
J	VSS	DT2IN	DT2OUT	DT3IN	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ3}}$	USB_RP	USB_RN	J
K	$\overline{\text{OE}}$	$\overline{\text{SD_WE}}$	DT3OUT	VDD	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\text{IRQ1}}$	USB_TN	USB_TP	VSSPLL	K
L	$\overline{\text{SD_ SCAS}}$	$\overline{\text{SD_ SRAS}}$	SD_CKE	$\overline{\text{TS}}$	SD_VDD	VSS	SD_VDD	SD_VDD	OVDD	OVDD	VSS	OVDD	$\overline{\text{TA}}$	USB_ TXEN	USB_ RXD	EXTAL	L
M	D31	$\overline{\text{SD_CS1}}$	$\overline{\text{BS3}}$	SD_DQS3	VSS	SD_VDD	SD_VDD	SD_VDD	OVDD	OVDD	OVDD	NC	USB_ SUSP	PLL_ TEST	VDDPLL	XTAL	M
N	D30	D29	D28	D20	D16	SD_A10	$\overline{\text{CS1}}$	VDD	TEST	DDATA2	DDATA0	QSPI_ CS2	CLK MOD1	$\overline{\text{RSTOUT}}$	$\overline{\text{RESET}}$	VSS	N
P	D27	D26	D23	D19	SD_DQS2	$\overline{\text{TIP}}$	R/$\overline{\text{W}}$	$\overline{\text{RCON}}$	$\overline{\text{U2CTS}}$	DDATA3	DDATA1	QSPI_ CS0	CLK MOD0	$\overline{\text{TRST}}$/ DSCLK	TDO/ DSO	TCLK/ PSTCLK	P
R	D25	D24	D22	D18	$\overline{\text{BS2}}$	$\overline{\text{CS0}}$	VSS	$\overline{\text{U2RTS}}$	U2TXD	PST2	PST0	QSPI_ DOUT	QSPI_ CS3	JTAG_ EN	TMS/ $\overline{\text{BKPT}}$	TDI/DSI	R
T	VSS	SD_ VREF	D21	D17	$\overline{\text{SD_CS0}}$	$\overline{\text{DDR_CLK OUT}}$	DDR_CLK OUT	$\overline{\text{TEA}}$	U2RXD	PST3	PST1	CLKOUT	QSPI_ DIN	QSPI_ CS1	QSPI_ CLK	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. MCF5274 and MCF5275 Pinout (256 MAPBGA)

6.4 Package Dimensions - 196 MAPBGA

Figure 6 shows MCF5275 196 MAPBGA package dimensions.



DIM	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 6. 196 MAPBGA Package Dimensions

7 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5274LVM166	MCF5274L RISC Microprocessor	196 MAPBGA	166 MHz	0° to +70° C
MCF5274LCVM166				-40° to +85° C
MCF5274VM166	MCF5274 RISC Microprocessor	256 MAPBGA	166 MHz	0° to +70° C
MCF5274CVM166				-40° to +85° C
MCF5275LCVM166	MCF5275L RISC Microprocessor	196 MAPBGA	166 MHz	-40° to +85° C
MCF5275CVM166	MCF5275 RISC Microprocessor	256 MAPBGA	166 MHz	-40° to +85° C

8 Electrical Characteristics

This appendix contains electrical specification tables and reference timing diagrams for the MCF5275 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5275.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

8.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
I/O Pad Supply Voltage (3.3V)	OV_{DD}	– 0.3 to +4.0	V
Memory Interface SSTL 2.5V Pad Supply Voltage	SDV_{DD}	– 0.3 to + 2.8	V
Memory Interface SSTL 3.3V Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

P_{INT} = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

8.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V
ESD Target for Machine Model	MM	200	V
HBM Circuit Description	R_{series}	1500	Ω
	C	100	pF
MM Circuit Description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) positive pulses negative pulses	 — —	 3 3	—
Interval of Pulses	—	1	sec

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

8.4 DC Electrical Specifications

Table 10. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	V_{DD}	1.4	1.6	V
I/O Pad Supply Voltage	OV_{DD}	3.0	3.6	V
PLL Supply Voltage	V_{DDPLL}	3.0	3.6	V
SSTL I/O Pad Supply Voltage	SDV_{DD}	2.3	2.7	V
SSTL I/O Pad Supply Voltage	SDV_{DD}	3.0	3.6	V
SSTL Memory pads reference voltage (SD V_{DD} = 2.5V)	V_{REF}	0.5 SD V_{DD}	—[2]	V
SSTL Memory pads reference voltage (SD V_{DD} = 3.3V)	V_{REF}	0.45 SD V_{DD}	—[2]	V
Input High Voltage 3.3V I/O Pads	V_{IH}	0.7 x OV_{DD}	OV_{DD} + 0.3	V
Input Low Voltage 3.3V I/O Pads	V_{IL}	V_{SS} – 0.3	0.35 x OV_{DD}	V
Output High Voltage 3.3V I/O Pads I_{OH} = –2.0 mA	V_{OH}	OV_{DD} - 0.5	—	V
Output Low Voltage 3.3V I/O Pads I_{OL} = 2.0mA	V_{OL}	—	0.5	V
Input Hysteresis 3.3V I/O Pads	V_{HYS}	0.06 x V_{DD}	—	mV
Input High Voltage SSTL 3.3V/2.5V[3]	V_{IH}	V_{REF} + 0.3	SDV_{DD} + 0.3	V
Input Low Voltage SSTL 3.3V/2.5V[3]	V_{IL}	V_{SS} - 0.3	V_{REF} - 0.3	V
Output High Voltage SSTL 3.3V/2.5V[4] I_{OH} = –5.0 mA	V_{OH}	SDV_{DD} - 0.25V	—	V
Output Low Voltage SSTL 3.3V/2.5V[4] I_{OL} = 5.0 mA	V_{OL}	—	0.35	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	-1.0	1.0	µA
High Impedance (Off-State) Leakage Current V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	-1.0	1.0	µA
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[5]	I_{APU}	-10	-130	µA
Input Capacitance [6] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

Table 13. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Data Outputs					
B11	CLKOUT high to data output (D[31:16]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:16]) invalid	t_{CHDOI}	1.0	—	ns
B13	CLKOUT high to data output (D[31:16]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}$, $\overline{BS}$, and $\overline{OE}$ transition after the falling edge of CLKOUT.

Read/write bus timings listed in Table 13 are shown in Figure 8, Figure 9, and Figure 10.

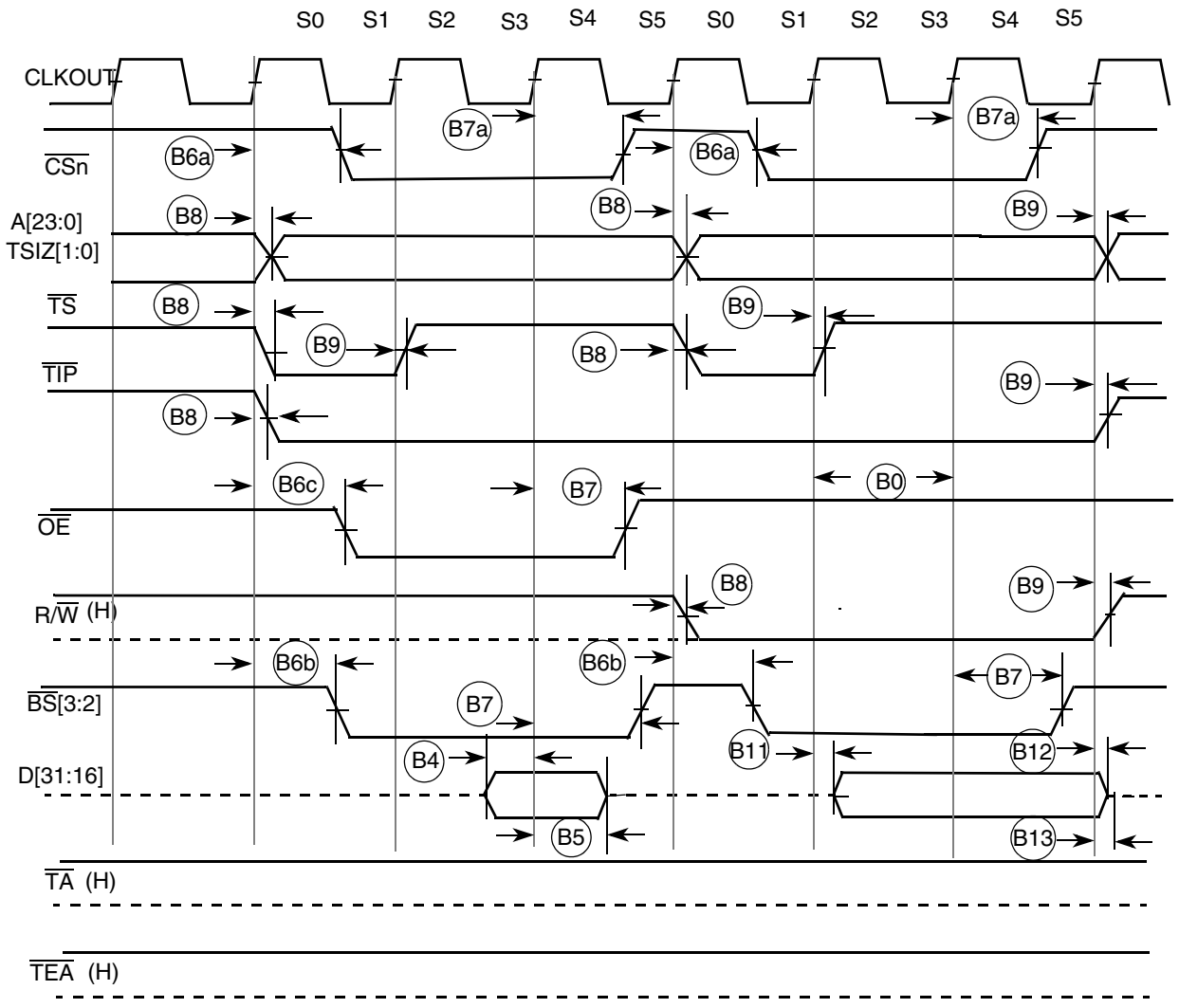


Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 13.

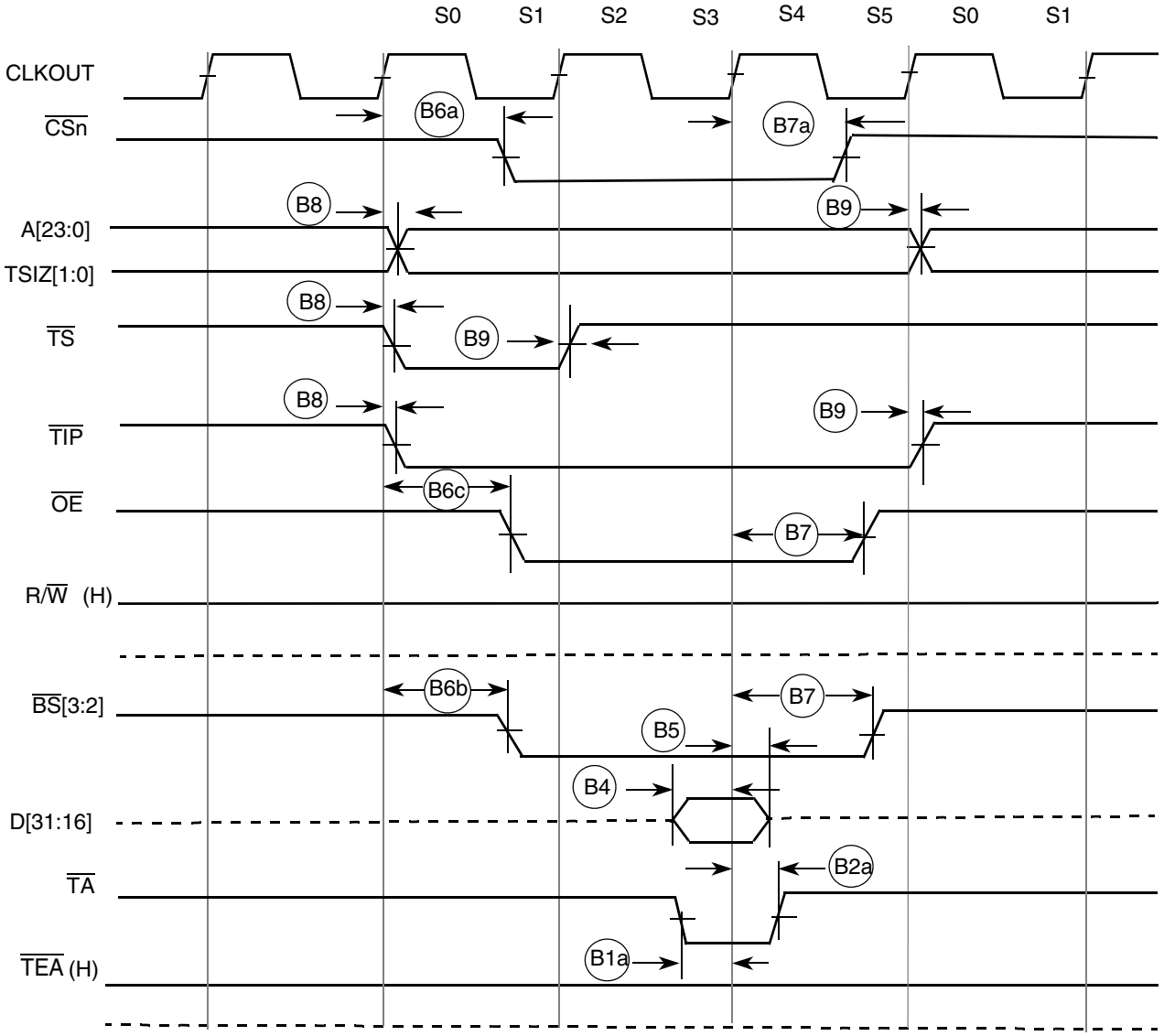


Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$

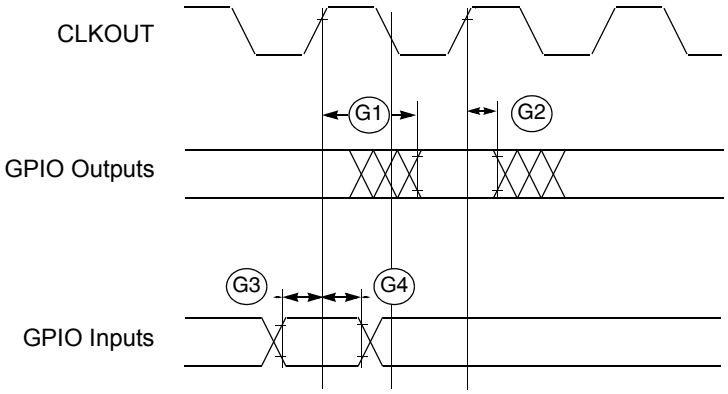


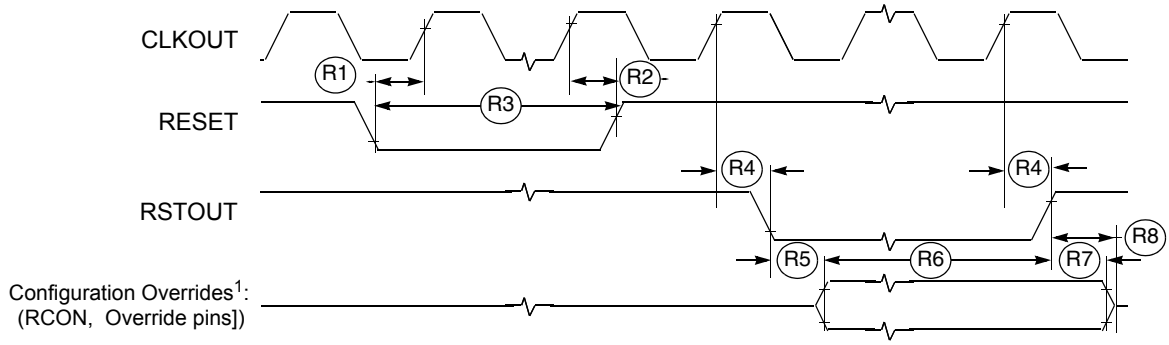
Figure 15. GPIO Timing

8.10 Reset and Configuration Override Timing

Table 17. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1 x t_{CYC}	ns

1 All AC timing is shown with respect to 50% OV_{DD} levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.



1. Refer to the Coldfire Integration Module (CIM) section for more information.

RESET and Configuration Override Timing

8.11 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 5.0 V or 3.3 V.

8.11.1 MII Receive Signal Timing (FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER, and FEC*n*_RXCLK)

The receiver functions correctly up to a FEC*n*_RXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC*n*_RXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER to FEC*n*_RXCLK setup	5	—	ns
M2	FEC*n*_RXCLK to FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER hold	5	—	ns
M3	FEC*n*_RXCLK pulse width high	35%	65%	FEC*n*_RXCLK period
M4	FEC*n*_RXCLK pulse width low	35%	65%	FEC*n*_RXCLK period

Figure 16 shows MII receive signal timings listed in Table 18.

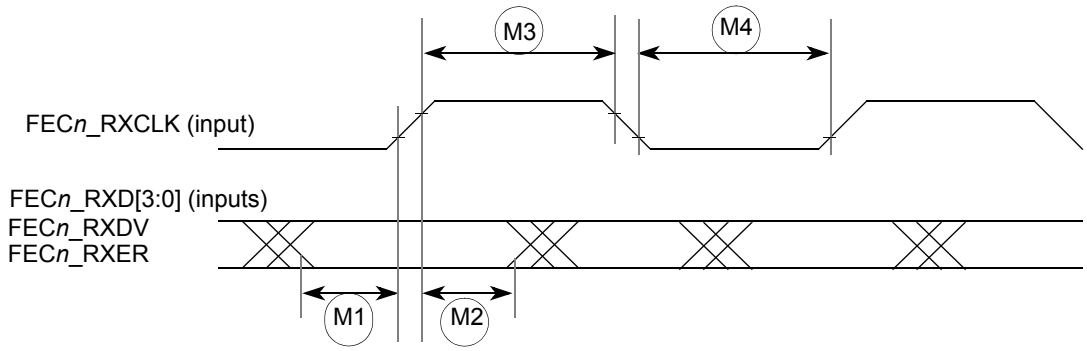


Figure 16. MII Receive Signal Timing Diagram

8.11.2 MII Transmit Signal Timing (FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER, FEC*n*_TXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC*n*_TXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC*n*_TXCLK frequency.

Table 19. MII Transmit Channel Timing

Num	Characteristic	Min	Max	Unit
M5	FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER invalid	5	—	ns
M6	FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER valid	—	25	ns
M7	FEC*n*_TXCLK pulse width high	35%	65%	FEC*n*_TXCLK period
M8	FEC*n*_TXCLK pulse width low	35%	65%	FEC*n*_TXCLK period

Figure 17 shows MII transmit signal timings listed in Table 19.

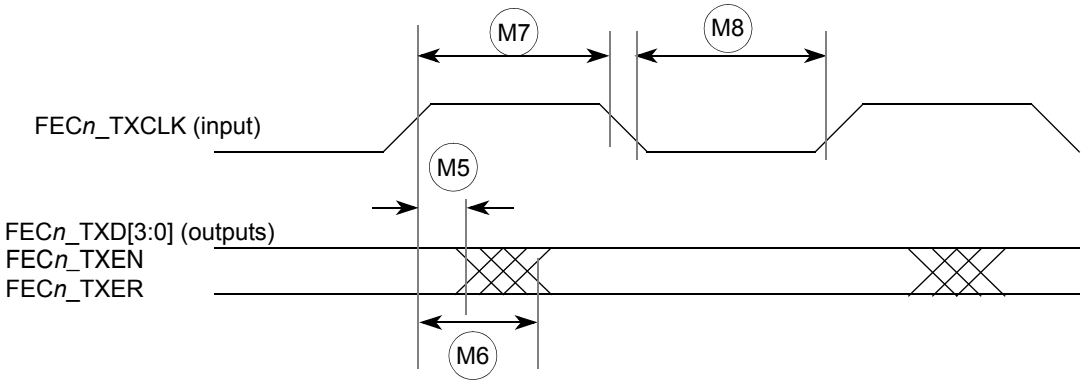


Figure 17. MII Transmit Signal Timing Diagram

8.11.3 MII Async Inputs Signal Timing (FEC*n*_CRS and FEC*n*_COL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Asynchronous Input Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC*n*_CRS, FEC*n*_COL minimum pulse width	1.5	—	FEC*n*_TXCLK period

Figure 18 shows MII asynchronous input timings listed in Table 20.

Figure 18. MII Async Inputs Timing Diagram

8.11.4 MII Serial Management Channel Timing (FEC*n*_MDIO and FEC*n*_MDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC*n*_MDC falling edge to FEC*n*_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC*n*_MDC falling edge to FEC*n*_MDIO output valid (max prop delay)	—	25	ns
M12	FEC*n*_MDIO (input) to FEC*n*_MDC rising edge setup	10	—	ns
M13	FEC*n*_MDIO (input) to FEC*n*_MDC rising edge hold	0	—	ns
M14	FEC*n*_MDC pulse width high	40%	60%	MDC period
M15	FEC*n*_MDC pulse width low	40%	60%	MDC period

Figure 19 shows MII serial management channel timings listed in Table 21.

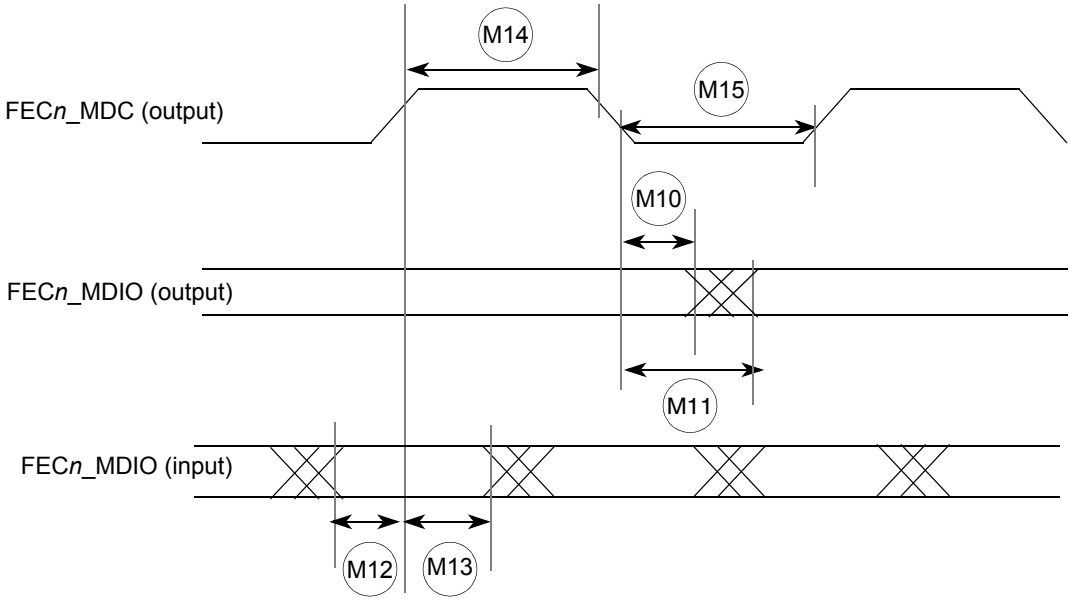


Figure 19. MII Serial Management Channel Timing Diagram

8.11.5 USB Interface AC Timing Specifications

Table 22 lists USB Interface timings.

Table 22. USB Interface Timing

Num	Characteristic	Min	Max	Units
US1	USB_CLK frequency of operation	48	48	MHz
US2	USB_CLK fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	2	ns
US3	USB_CLK rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	2	ns
US4	USB_CLK duty cycle (at 0.5 x O V_{DD})	45	55	%
Data Inputs				
US5	USB_RP, USB_RN, USB_RXD valid to USB_CLK high	6	—	ns
US6	USB_CLK high to USB_RP, USB_RN, USB_RXD invalid	6	—	ns
Data Outputs				
US7	USB_CLK high to USB_TP, USB_TN, USB_SUSP valid	—	12	ns
US8	USB_CLK high to USB_TP, USB_TN, USB_SUSP invalid	3	—	ns

Figure 20 shows USB interface timings listed in Table 22.

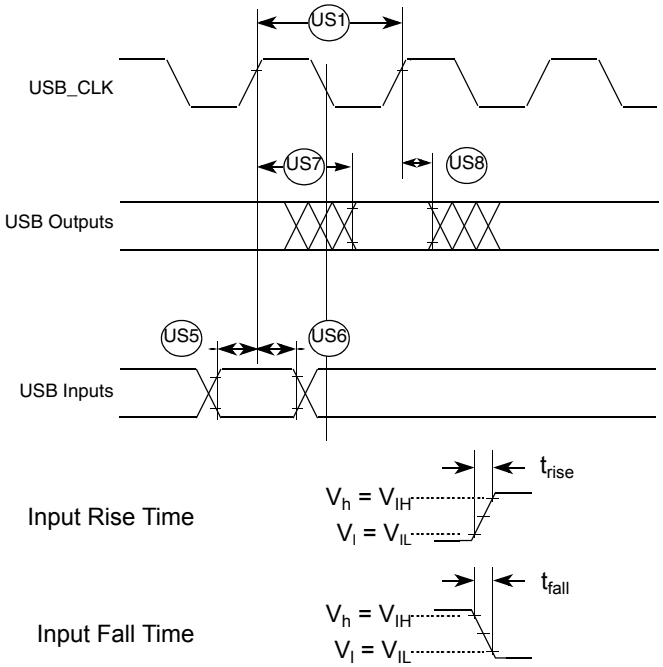


Figure 20. USB Signals Timing Diagram

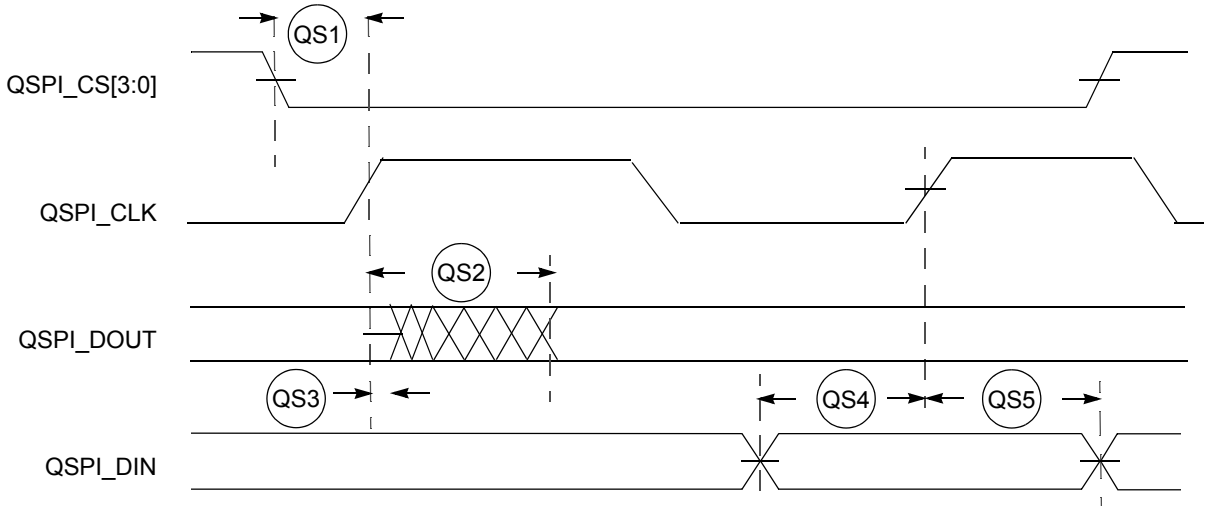


Figure 22. QSPI Timing

8.15 JTAG and Boundary Scan Timing

Table 27. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4 x t_{CYC}	—	ns
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

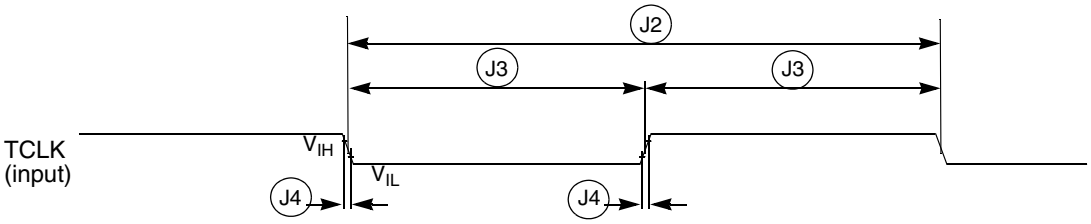


Figure 23. Test Clock Input Timing

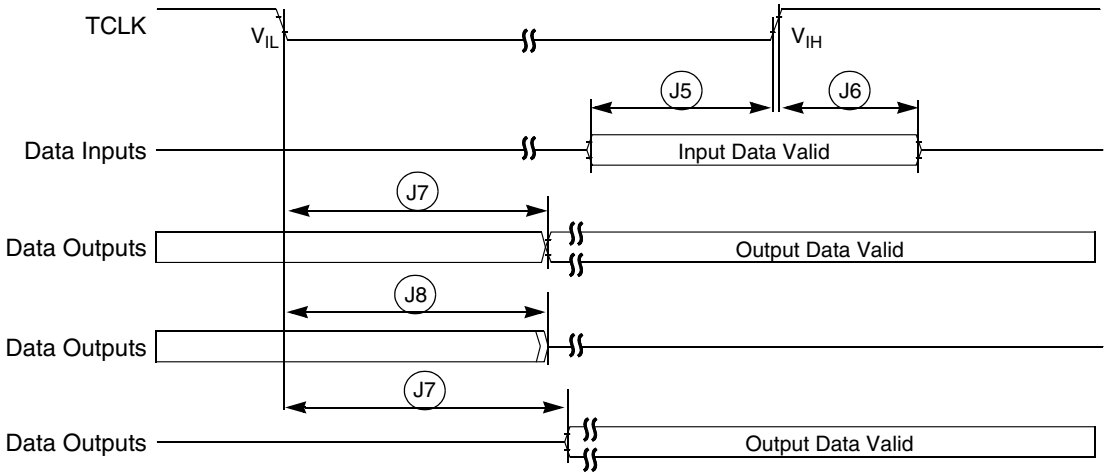


Figure 24. Boundary Scan (JTAG) Timing

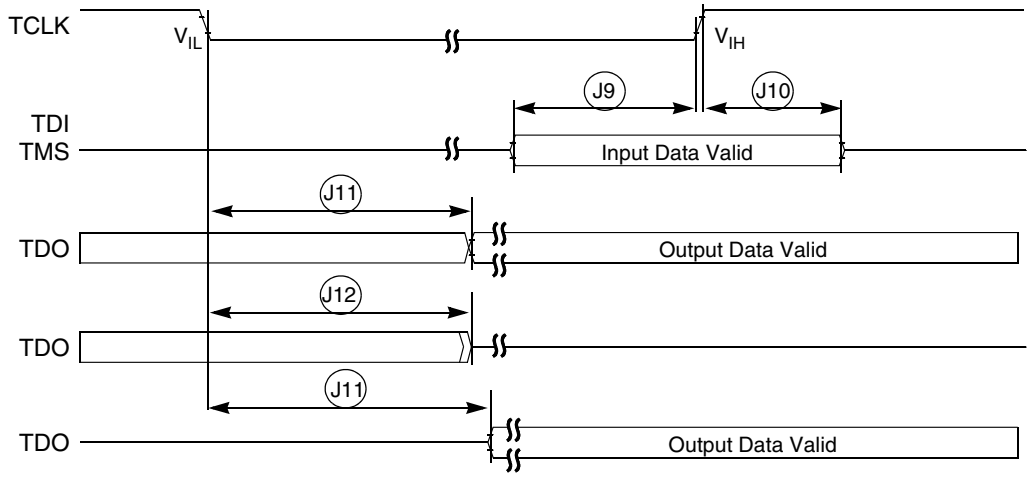


Figure 25. Test Access Port Timing

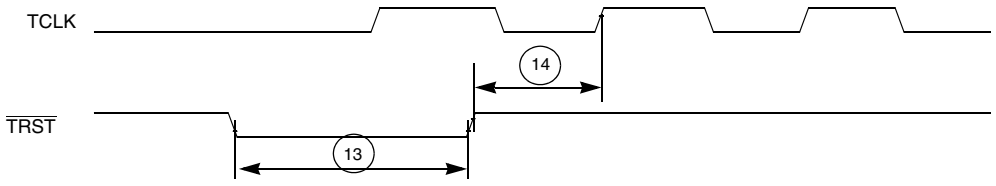


Figure 26. TRST Timing

8.16 Debug AC Timing Specifications

Table 28 lists specifications for the debug AC timing parameters shown in Figure 28.

Table 28. Debug AC Timing Specification

Num	Characteristic	166 MHz		Units
		Min	Max	
D0	PSTCLK cycle time	—	0.5	t_{CYC}
D1	PST, DDATA to PSTCLK setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.0	—	ns
D3	DSI-to-DSCLK setup	1 x t_{CYC}	—	ns
D4 [1]	DSCLK-to-DSO hold	4 x t_{CYC}	—	ns
D5	DSCLK cycle time	5 x t_{CYC}	—	ns
D6	$\overline{BKPT}$ input data setup time to PSTCLK Rise	4	—	ns
D7	$\overline{BKPT}$ input data hold time to PSTCLK Rise	1.5	—	ns
D8	PSTCLK high to $\overline{BKPT}$ high Z	0.0	10.0	ns

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

Figure 27 shows real-time trace timing for the values in Table 28.

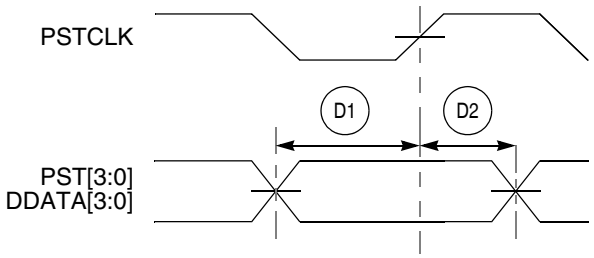


Figure 27. Real-Time Trace AC Timing

Figure 28 shows BDM serial port AC timing for the values in Table 28.

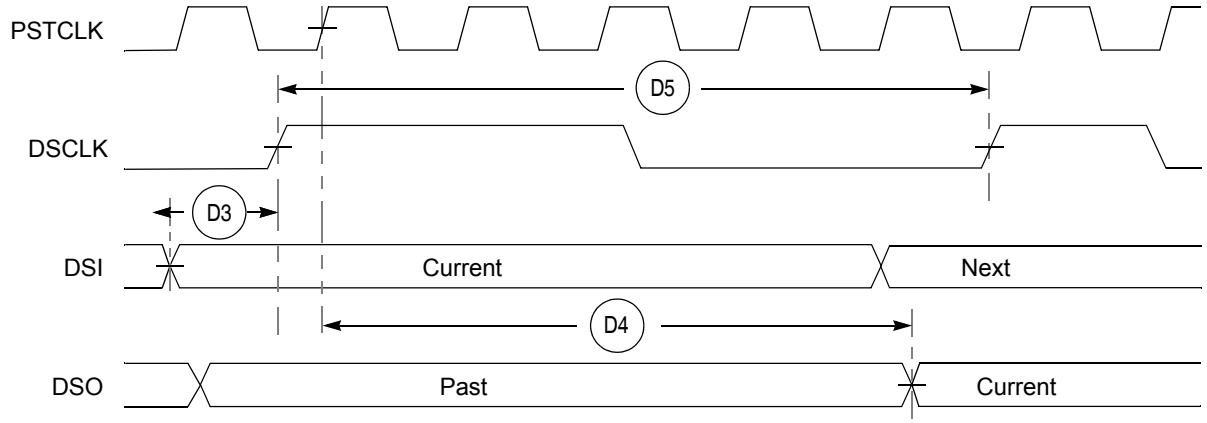


Figure 28. BDM Serial Port AC Timing

9 Documentation

Documentation regarding the MCF5275 and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

10 Revision History

Table 29 provides a revision history for this hardware specification.

Table 29. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.
1	Added Figure 6.
1.1	Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	Removed Overview, Features, Signal Descriptions, Modes of Operation, and Address Multiplexing sections. This information can be found in the MCF5275 Reference Manual. Removed list of documentation in Section 9, "Documentation.". An up-to-date list is always available on our web site. Changed CLKOUT -> PSTCLK in Section 8.16, "Debug AC Timing Specifications." Table 10: Update V_{DD} spec from 1.35-1.65 to 1.4-1.6. Table 13: Timings B6a, B6b, B6c, B7, B7a, B9, B12 updated: B6a, B6b, B6c maximum changed from "$0.5t_{CYC}$ + 5" to "$0.5t_{CYC}$ + 5.5" B7, B7a minimum changed from "$0.5t_{CYC}$ + 1.5" to "$0.5t_{CYC}$ + 1.0" B9, B11 minimum changed from "1.5" to "1.0"
1.3	Added Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions." Added thermal characteristics for 196 MAPBGA in Table 8. Updated package dimensions drawing, Figure 6.
2	Removed second sentence from Section 8.11.1, "MII Receive Signal Timing (FECn_RXD[3:0], FECn_RXDV, FECn_RXER, and FECn_RXCLK)," and Section 8.11.2, "MII Transmit Signal Timing (FECn_TXD[3:0], FECn_TXEN, FECn_TXER, FECn_TXCLK)," regarding no minimum frequency requirement for TXCLK. Removed third and fourth paragraphs from Section 8.11.2, "MII Transmit Signal Timing (FECn_TXD[3:0], FECn_TXEN, FECn_TXER, FECn_TXCLK)," as this feature is not supported on this device.
3	Corrected Ordering Information, Table 6. Figure 2: Moved $PLLV_{DD}$ from 1.5V to 3.3V supply line and corrected relevant text in sections below table. Table 10: Corrected maximum "Input High Voltage 3.3V I/O Pads", V_{IH} specification.
4	Table 10, added PLL supply voltage row