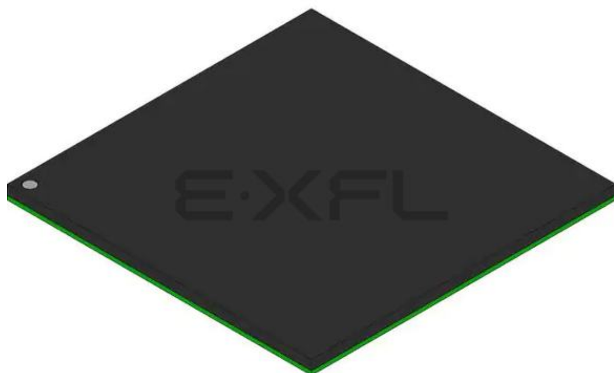

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, WDT
Number of I/O	69
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5275cvm166

2 Block Diagram

The superset device in the MCF5275 family comes in a 256 Mold Array Plastic Ball Grid Array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5275, the superset device.

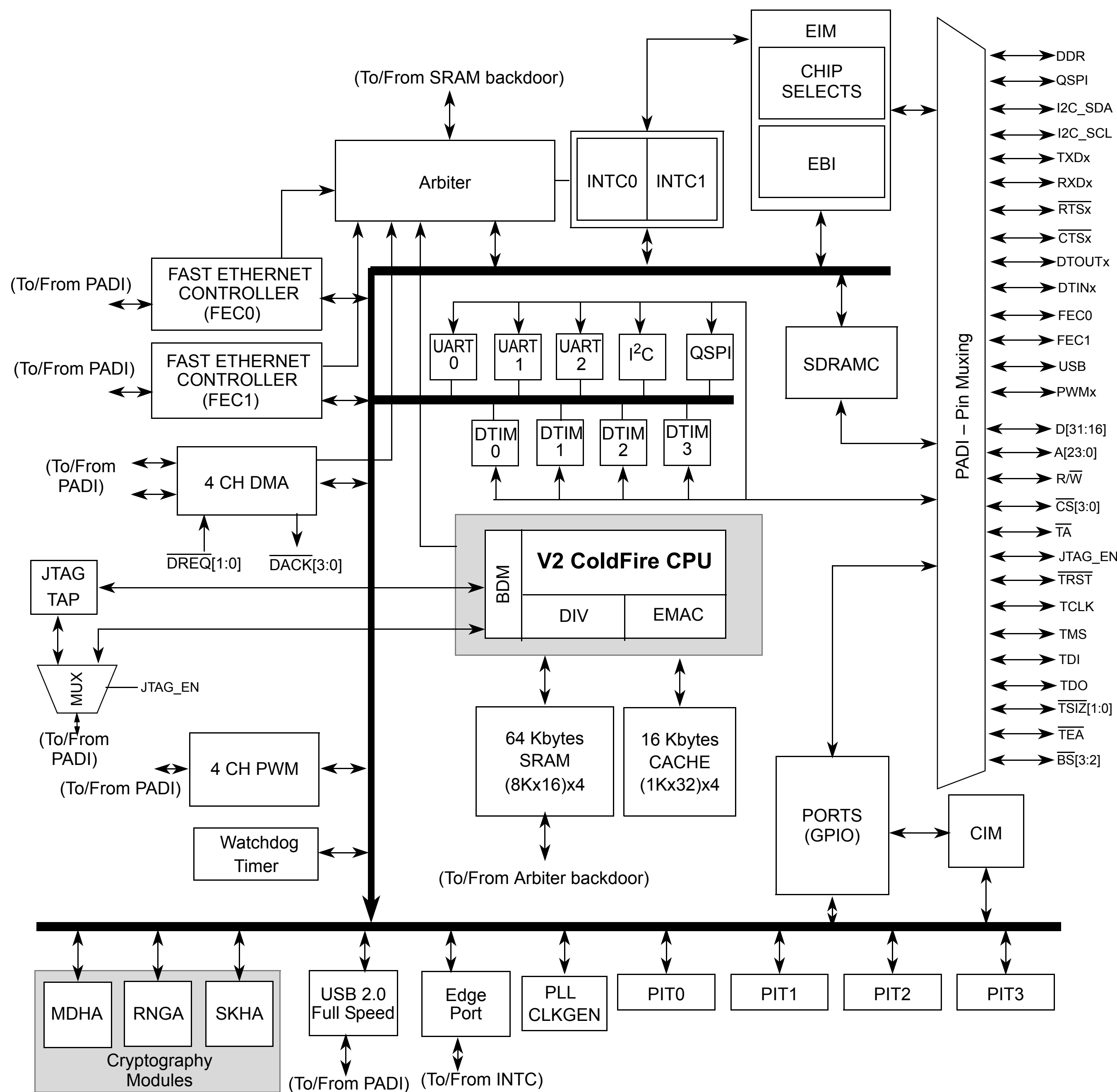


Figure 1. MCF5275 Block Diagram

3 Features

For a detailed feature list see the *MCF5275 Reference Manual* (MCF5275RM).

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
I²C						
I2C_SDA	PFECI2C[1]	U2RXD	—	I/O	B10	B7
I2C_SCL	PFECI2C[0]	U2TXD	—	I/O	C10	A7
DMA						
DACK[3:0] and DREQ[3:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: PCS3/PWM3 for DACK3, PCS2/PWM2 for DACK2, TSIZ1 for DACK1, TSIZ0 for DACK0, IRQ3 for DREQ3, IRQ2 and TA for DREQ2, TEA for DREQ1, and TIP for DREQ0.					—	—
QSPI						
QSPI_CS[3:2]	PQSPI[6:5]	PWM[3:2]	DACK[3:2]	O	R13, N12	P10, N9
QSPI_CS1	PQSPI[4]	—	—	O	T14	N10
QSPI_CS0	PQSPI[3]	—	—	O	P12	M9
QSPI_CLK	PQSPI[2]	I2C_SCL	—	O	T15	L11
QSPI_DIN	PQSPI[1]	I2C_SDA	—	I	T13	M10
QSPI_DOUT	PQSPI[0]	—	—	O	R12	L10
UARTs						
U2RXD	PUARTH[3]	—	—	I	T9	—
U2TXD	PUARTH[2]	—	—	O	R9	—
U2CTS	PUARTH[1]	PWM1	—	I	P9	—
U2RTS	PUARTH[0]	PWM0	—	O	R8	—
U1RXD	PUARTL[7]	—	—	I	A9	A6
U1TXD	PUARTL[6]	—	—	O	B9	D7
U1CTS	PUARTL[5]	—	—	I	C9	C7
U1RTS	PUARTL[4]	—	—	O	D9	B6
U0RXD	PUARTL[3]	—	—	I	A8	A4
U0TXD	PUARTL[2]	—	—	O	B8	A5
U0CTS	PUARTL[1]	—	—	I	C8	C6
U0RTS	PUARTL[0]	—	—	O	D7	B5
USB						
USB_SPEED	PUSBH[0]	—	—	I/O	G14	G11
USB_CLK	PUSBL[7]	—	—	I	G15	F12

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
USB_RN	PUSBL[6]	—	—	I	J16	H13
USB_RP	PUSBL[5]	—	—	I	J15	J11
USB_RXD	PUSBL[4]	—	—	I	L15	L14
USB_SUSP	PUSBL[3]	—	—	O	M13	N13
USB_TN	PUSBL[2]	—	—	O	K14	J14
USB_TP	PUSBL[1]	—	—	O	K15	J12
USB_TXEN	PUSBL[0]	—	—	O	L14	K13
Timers (and PWMs)						
DT3IN	PTIMERH[3]	DT3OUT	$\overline{\text{U2RTS}}$	I	J4	G2
DT3OUT	PTIMERH[2]	PWM3	$\overline{\text{U2CTS}}$	O	K3	G1
DT2IN	PTIMERH[1]	DT2OUT	—	I	J2	F3
DT2OUT	PTIMERH[0]	PWM2	—	O	J3	F4
DT1IN	PTIMERL[3]	DT1OUT	—	I	H1	F1
DT1OUT	PTIMERL[2]	PWM1	—	O	H2	F2
DT0IN	PTIMERL[1]	DT0OUT	—	I	H3	E1
DT0OUT	PTIMERL[0]	PWM0	—	O	G3	E2
BDM/JTAG[2]						
DSCLK	—	$\overline{\text{TRST}}$	—	I	P14	P13
PSTCLK	—	TCLK	—	O	P16	P12
$\overline{\text{BKPT}}$	—	TMS	—	I	R15	N12
DSI	—	TDI	—	I	R16	M12
DSO	—	TDO	—	O	P15	K11
JTAG_EN	—	—	—	I	R14	P11
DDATA[3:0]	—	—	—	O	P10, N10, P11, N11	M7, N7, P8, L9
PST[3:0]	—	—	—	O	T10, R10, T11, R11	P7, L8, M8, N8
Test						
TEST	—	—	—	I	N9	N6
PLL_TEST	—	—	—	I	M14	—
Power Supplies						
VDDPLL	—	—	—	I	M15	M13

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
VSSPLL	—	—	—	I	K16	L13
VSS	—	—	—	I	A1, A10, A16, E5, E12, F6, F11, G7:10, H7:10, J1, J7:10, K7:10, L6, L11, M5, N16, R7, T1, T16	F7, F8, G6:9, H6:9, J7, J8
OVDD	—	—	—	I	E6:8, F5, F7, F8, G5, G6, H5, H6, J11, J12, K11, K12, L9, L10, L12, M9:11	E5:7, F5, F6, H10, J9, J10, K8:10
VDD	—	—	—	I	D8, H13, K4, N8	D6, G5, G12, L7
SD_VDD	—	—	—	I	E9:11, F9, F10, F12, G11, G12, H11, H12, J5, J6, K5, K6, L5, L7, L8, M6, M7, M8	E8:10, F9, F10, G10, H5, J5, J6, K5:7

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

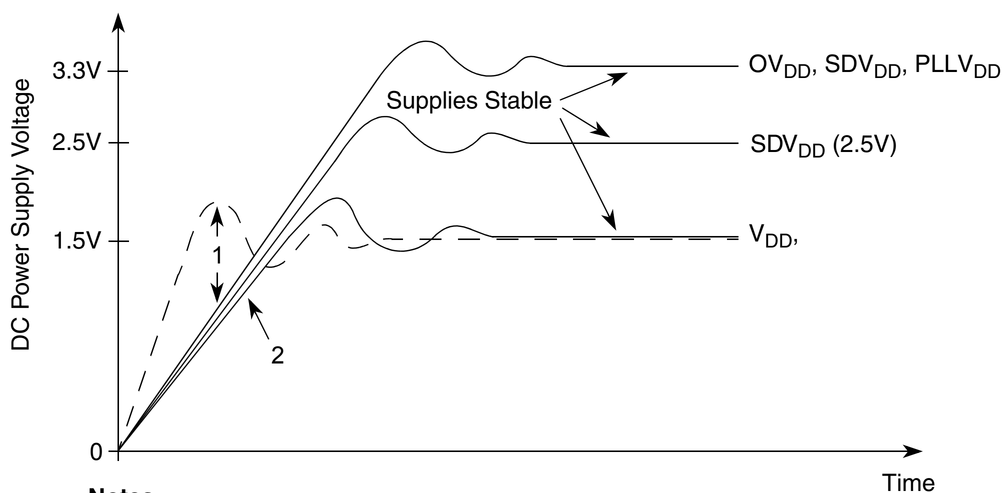
- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5275.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33uF, 0.1 µF, and 0.01 µF across each power supply

5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O V_{DD} (OV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} ($PLLV_{DD}$), and Core V_{DD} (V_{DD}).



Notes:
1. VDD should not exceed OVDD, SDVDD or PLLVDD by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/SDVDD/PLLVDD up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, SDVDD, VDD, or PLLVDD) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 2. Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and OV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and OV_{DD} are specified relative to V_{DD}.

5.2.1.1 Power Up Sequence

If OV_{DD}/SDV_{DD} are powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD}/SDV_{DD} powers up before V_{DD} must powered up. V_{DD} should not lead the OV_{DD}, $SDV_{DD,}$ or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or high current will be in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 µs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 µs or slower rise time for all supplies.
2. V_{DD}/$PLLV_{DD}$ and OV_{DD}/SDV_{DD} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD}/SD V_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

5.2.1.2 Power Down Sequence

If V_{DD} is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after V_{DD} powers down before OV_{DD}, SDV_{DD}, or $PLLV_{DD}$ must power down. V_{DD} should not lag OV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or undesired high current will be in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop V_{DD} to 0 V.
2. Drop OV_{DD}/SDV_{DD}/$PLLV_{DD}$ supplies.

5.3 Decoupling

- Place the decoupling capacitors as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 μF and 0.01 μF at each supply input

5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See electricals.

5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

5.7 Interface Recommendations

5.7.1 DDR SDRAM Controller

5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

Table 3. Synchronous DRAM Signal Connections

Signal	Description
SD_SRAS	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. SD_SRAS should be connected to the corresponding SDRAM SD_SRAS. Do not confuse SD_SRAS with the DRAM controller's SDRAM_CS[1:0], which should not be interfaced to the SDRAM SD_SRAS signals.
SD_SCAS	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. SD_SCAS should be connected to the corresponding signal labeled SD_SCAS on the SDRAM.
SD_WE	DRAM read/write. Asserted for write operations and negated for read operations.
SD_CS[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF5275. One SDRAM_CS signal selects one SDRAM block and connects to the corresponding CS signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
BS[3:2]	Column address strobe. For synchronous operation, BS[3:2] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
DDR_CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5275 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

The FEC supports an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF5275 Pin
Transmit clock	FEC*n*_TXCLK
Transmit enable	FEC*n*_TXEN
Transmit data	FEC*n*_TXD[3:0]
Transmit error	FEC*n*_TXER

6 Mechanicals/Pinouts

6.1 256 MAPBGA Pinout

Figure 3 is a consolidated MCF5274/75 pinout for the 256 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FEC1_RXD1	FEC1_RXDV	FEC1_CRS	FEC1_COL	FEC0_COL	FEC0_MDIO	U0RXD	U1RXD	VSS	A23	A20	A17	A14	SD_VREF	VSS	A
B	FEC1_RXD3	FEC1_RXD2	FEC1_RXD0	FEC1_RXCLK	FEC0_RXDV	FEC0_RXCLK	FEC0_MDC	U0TXD	U1TXD	I2C_SDA	A22	A19	A16	A13	A11	A9	B
C	FEC1_TXCLK	FEC1_RXER	FEC0_TXCLK	FEC0_RXER	FEC0_RXD2	FEC0_RXD0	FEC0_CRS	U0CTS	U1CTS	I2C_SCL	A21	A18	A15	A12	A10	A8	C
D	FEC1_TXER	FEC1_TXEN	FEC0_TXER	FEC0_TXEN	FEC0_RXD3	FEC0_RXD1	U0RTS	VDD	U1RTS	CS7	CS6	CS5	CS4	A7	A6	TSIZ1	D
E	FEC1_TXD3	FEC1_TXD2	FEC0_TXD3	NC	VSS	OVDD	OVDD	OVDD	SD_VDD	SD_VDD	SD_VDD	VSS	CS3	A5	A4	A3	E
F	FEC1_TXD0	FEC1_TXD1	FEC0_TXD2	FEC0_TXD1	OVDD	VSS	OVDD	OVDD	SD_VDD	SD_VDD	VSS	SD_VDD	CS2	A2	A1	A0	F
G	FEC1_MDIO	FEC1_MDC	DT0OUT	FEC0_TXD0	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	IRQ7	USB_SPEED	USB_CLK	TSIZ0	G
H	DT1IN	DT1OUT	DT0IN	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	VDD	IRQ4	IRQ5	IRQ6	H
J	VSS	DT2IN	DT2OUT	DT3IN	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	IRQ2	IRQ3	USB_RP	USB_RN	J
K	OE	SD_WE	DT3OUT	VDD	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	IRQ1	USB_TN	USB_TP	VSSPLL	K
L	SD_SCAS	SD_SRAS	SD_CKE	TS	SD_VDD	VSS	SD_VDD	SD_VDD	OVDD	OVDD	VSS	OVDD	TA	USB_TXEN	USB_RXD	EXTAL	L
M	D31	SD_CS1	BS3	SD_DQS3	VSS	SD_VDD	SD_VDD	SD_VDD	OVDD	OVDD	OVDD	NC	USB_SUSP	PLL_TEST	VDDPLL	XTAL	M
N	D30	D29	D28	D20	D16	SD_A10	CS1	VDD	TEST	DDATA2	DDATA0	QSPI_CS2	CLKMOD1	RSTOUT	RESET	VSS	N
P	D27	D26	D23	D19	SD_DQS2	TIP	R/W	RCON	U2CTS	DDATA3	DDATA1	QSPI_CS0	CLKMOD0	TRST/DSCLK	TDO/DSO	TCLK/PSTCLK	P
R	D25	D24	D22	D18	BS2	CS0	VSS	U2RTS	U2TXD	PST2	PST0	QSPI_DOUT	QSPI_CS3	JTAG_EN	TMS/BKPT	TDI/DSI	R
T	VSS	SD_VREF	D21	D17	SD_CS0	DDR_CLKOUT	DDR_CLKOUT	TEA	U2RXD	PST3	PST1	CLKOUT	QSPI_DIN	QSPI_CS1	QSPI_CLK	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. MCF5274 and MCF5275 Pinout (256 MAPBGA)

P_{INT} = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273 °C) + \Theta_{JMA} \times P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

8.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V
ESD Target for Machine Model	MM	200	V
HBM Circuit Description	R_{series}	1500	Ω
	C	100	pF
MM Circuit Description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) positive pulses negative pulses	 — —	 3 3	—
Interval of Pulses	—	1	sec

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 10. DC Electrical Specifications[1] (continued)

Characteristic	Symbol	Min	Max	Unit
Load Capacitance[7] Low Drive Strength High Drive Strength	C_L	 — —	 25 50	pF
Core Operating Supply Current[8] Master Mode WAIT DOZE STOP	I_{DD}	 — — — —	 175 15 10 100	 mA mA mA μA
I/O Pad Operating Supply Current Master Mode Low Power Modes	OI_{DD}	 — —	 250 250	 mA μA
DC Injection Current [3, 9, 10, 11] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single Pin Limit Total MCU Limit, Includes sum of all stressed pins	I_{IC}	 -1.0 -10	 1.0 10	mA

1 Refer to Table 11 for additional PLL specifications.
2 V_{REF} is specified as a nominal value only instead of a range, so no maximum value is listed.
3 This specification is guaranteed by design and is not 100% tested.
4 The actual V_{OH} and V_{OL} values for SSTL pads are dependent on the termination and drive strength used. The specifications numbers assume no parallel termination.
5 Refer to the MCF5274 signals chapter for pins having weak internal pull-up devices.
6 This parameter is characterized before qualification rather than 100% tested.
7 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.
8 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.
9 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.
10 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
11 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

Figure 10 shows an SRAM bus cycle terminated by $\overline{TEA}$ showing timings listed in Table 13.

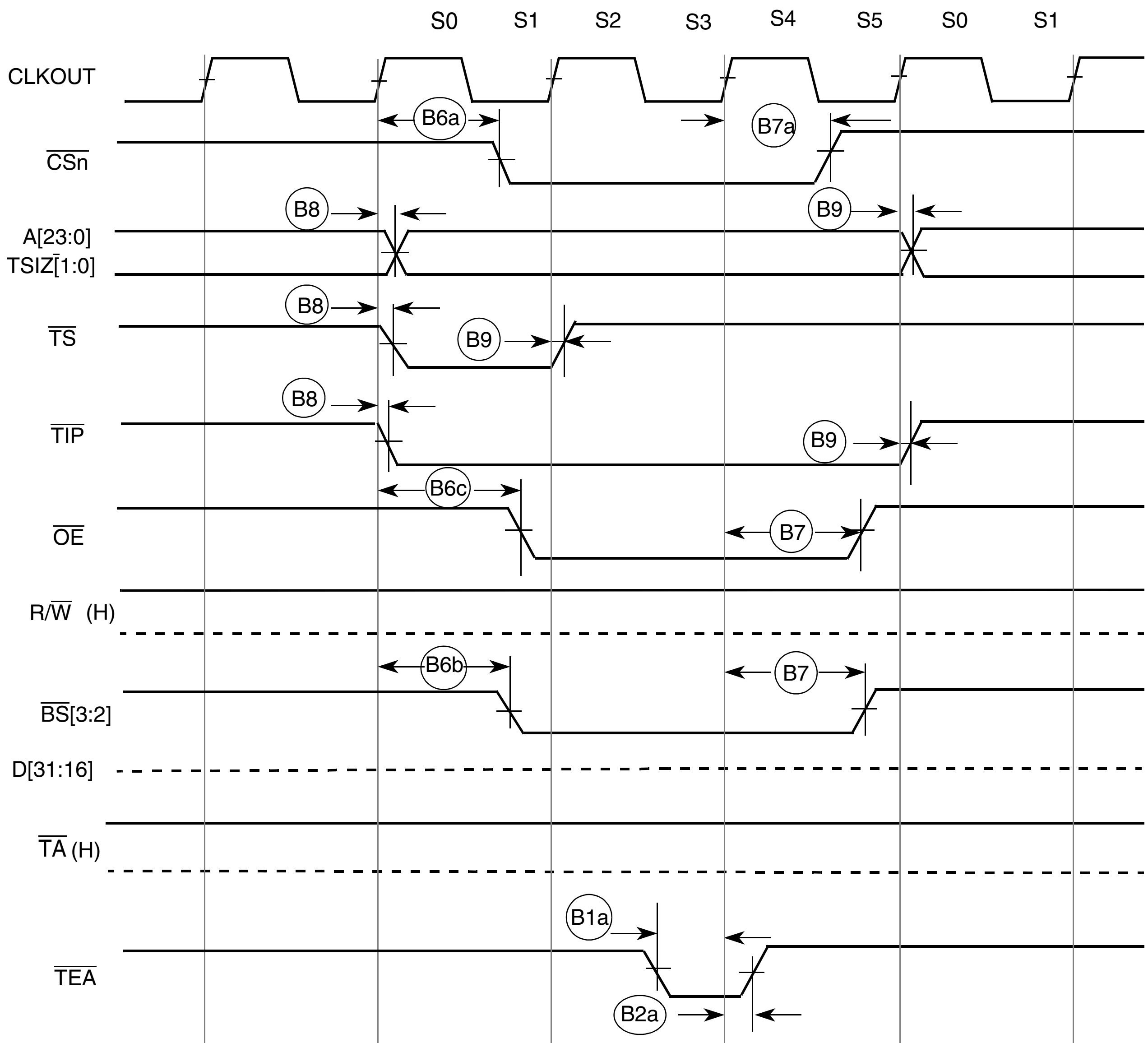


Figure 10. SRAM Read Bus Cycle Terminated by $\overline{TEA}$

8.8 DDR SDRAM AC Timing Characteristics

The DDR SDRAM controller uses SSTL2 and I/O drivers. Class I or Class II drive strength is available and is user programmable. DDR Clock timing specifications are given in Table 14 and Figure 11.

Table 14. DDR Clock Timing Specifications[1]

Symbol	Characteristic	Min	Max	Unit
V_{MP}	Clock output mid-point voltage	1.05	1.45	V
V_{OUT}	Clock output voltage level	-0.3	SDV_{DD} + 0.3	V
V_{ID}	Clock output differential voltage (peak to peak swing)	0.7	SDV_{DD} + 0.6	V
V_{IX}	Clock crossing point voltage	1.05	1.45	V

1 SD V_{DD} is nominally 2.5V.

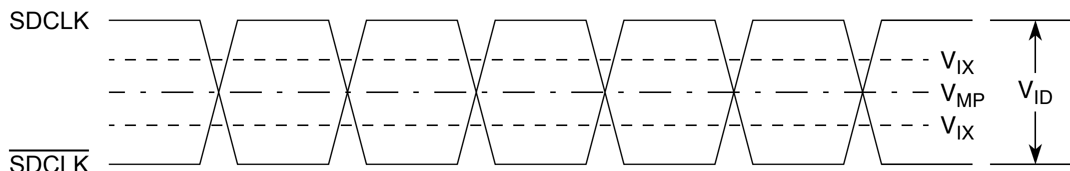


Figure 11. DDR Clock Timing Diagram

When using the DDR SDRAM controller the timing numbers in Table 15 must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the two DQS byte lanes.

Table 15. DDR Timing

NUM	Characteristic[1]	Symbol	Min	Max	Unit
	Frequency of operation[2]		TBD	83	MHz
DD1	Clock Period (DDR_CLKOUT)	t_{CK}	12	TBD	ns
DD2	Pulse Width High[3]	t_{CKH}	0.45	0.55	t_{CK}
DD3	Pulse Width Low[3]	t_{CKl}	0.45	0.55	t_{CK}
DD4	DDR_CLKOUT high to DDR address, SD_CKE, SD_CS[1:0], SD_SCAS, SD_SRAS, SD_WE valid	t_{CMV}	—	0.5 x t_{CK} + 1	ns
DD5	DDR_CLKOUT high to DDR address, SD_CKE, $\overline{SD_CS}$, $\overline{SD_SCAS}$, $\overline{SD_SRAS}$, $\overline{SD_WE}$ invalid	t_{CMH}	2	—	ns
DD6	Write command to first $\overline{SD_DQS}$ Latching Transition	t_{DQSS}	—	1.25	t_{CK}
DD7	$\overline{SD_DQS}$ high to Data and DM valid (write) - setup[4,5]	t_{QS}	1.5	—	ns
DD8	$\overline{SD_DQS}$ high to Data and DM invalid (write) - hold[4]	t_{QH}	1	—	ns
DD9	$\overline{SD_DQS}$ high to Data valid (read) - setup[6]	t_{IS}	—	1	ns
DD10	$\overline{SD_DQS}$ high to Data invalid (read) - hold[7]	t_{IH}	0.25 x t_{CK} + 1	—	ns
DD11	$\overline{SD_DQS}$ falling edge to CLKOUT high - setup	t_{DSS}	0.5	—	ns
DD12	$\overline{SD_DQS}$ falling edge to CLKOUT high - hold	t_{DSH}	0.5	—	ns

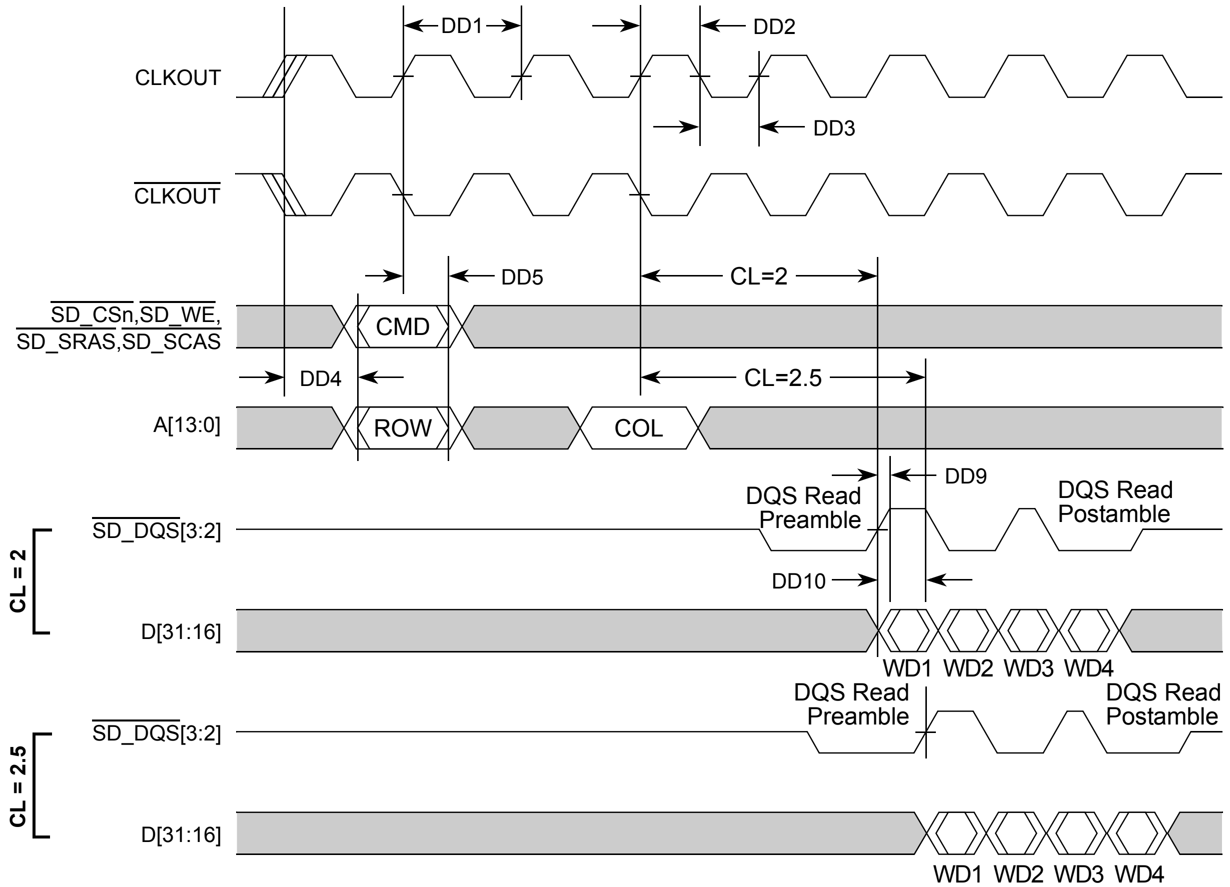


Figure 14. DDR Read Timing

8.9 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR control, timers, UARTS, FEC0, FEC1, Interrupts and USB interfaces. When in GPIO mode the timing specification for these pins is given in Table 16 and Figure 15.

Table 16. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.0	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

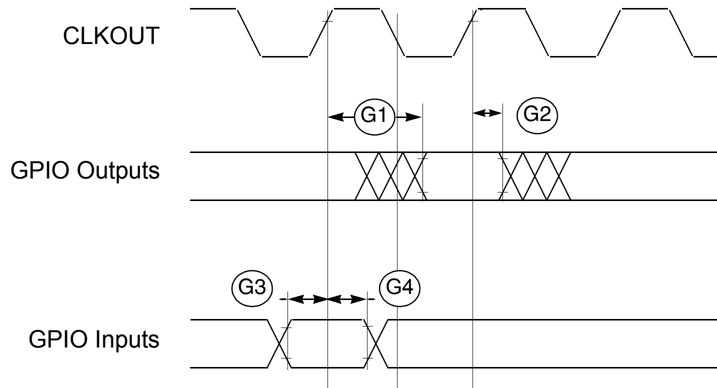


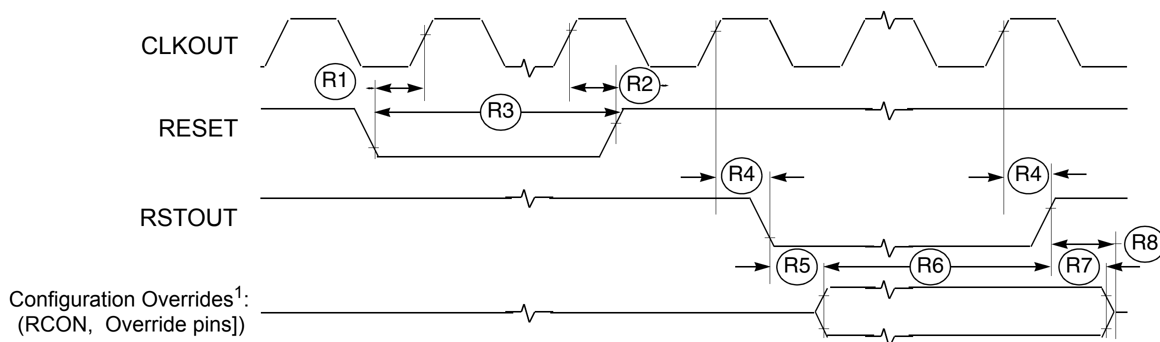
Figure 15. GPIO Timing

8.10 Reset and Configuration Override Timing

Table 17. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1 x t_{CYC}	ns

[1] All AC timing is shown with respect to 50% OV_{DD} levels unless otherwise noted.
[2] During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.



1. Refer to the Coldfire Integration Module (CIM) section for more information.

RESET and Configuration Override Timing

8.11.4 MII Serial Management Channel Timing (FEC*n*_MDIO and FEC*n*_MDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC*n*_MDC falling edge to FEC*n*_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC*n*_MDC falling edge to FEC*n*_MDIO output valid (max prop delay)	—	25	ns
M12	FEC*n*_MDIO (input) to FEC*n*_MDC rising edge setup	10	—	ns
M13	FEC*n*_MDIO (input) to FEC*n*_MDC rising edge hold	0	—	ns
M14	FEC*n*_MDC pulse width high	40%	60%	MDC period
M15	FEC*n*_MDC pulse width low	40%	60%	MDC period

Figure 19 shows MII serial management channel timings listed in Table 21.

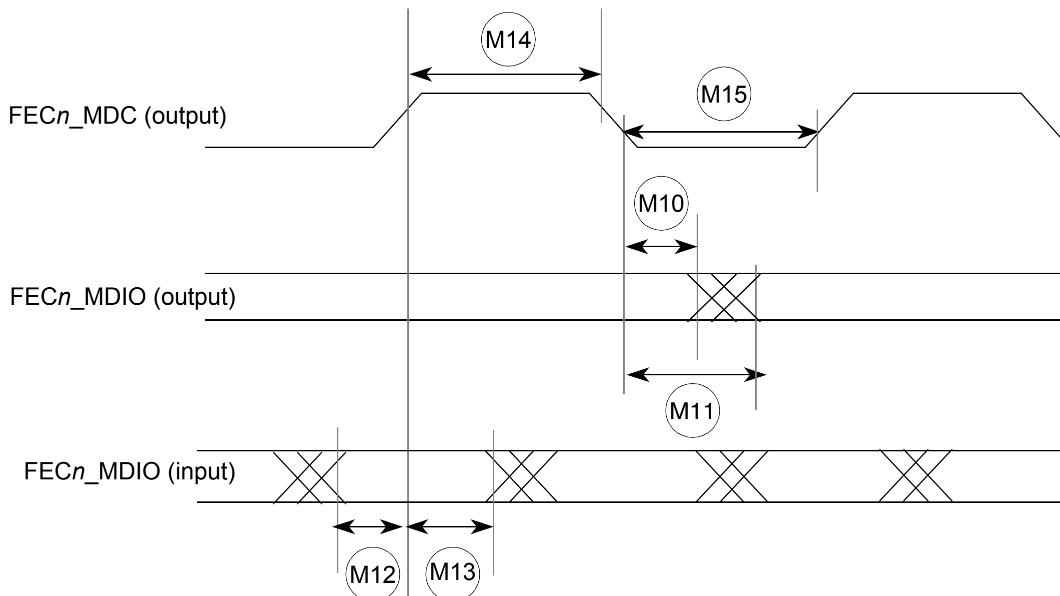


Figure 19. MII Serial Management Channel Timing Diagram

8.11.5 USB Interface AC Timing Specifications

Table 22 lists USB Interface timings.

Table 22. USB Interface Timing

Num	Characteristic	Min	Max	Units
US1	USB_CLK frequency of operation	48	48	MHz
US2	USB_CLK fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	2	ns
US3	USB_CLK rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	2	ns
US4	USB_CLK duty cycle (at 0.5 x O V_{DD})	45	55	%
Data Inputs				
US5	USB_RP, USB_RN, USB_RXD valid to USB_CLK high	6	—	ns
US6	USB_CLK high to USB_RP, USB_RN, USB_RXD invalid	6	—	ns
Data Outputs				
US7	USB_CLK high to USB_TP, USB_TN, USB_SUSP valid	—	12	ns
US8	USB_CLK high to USB_TP, USB_TN, USB_SUSP invalid	3	—	ns

Figure 20 shows USB interface timings listed in Table 22.

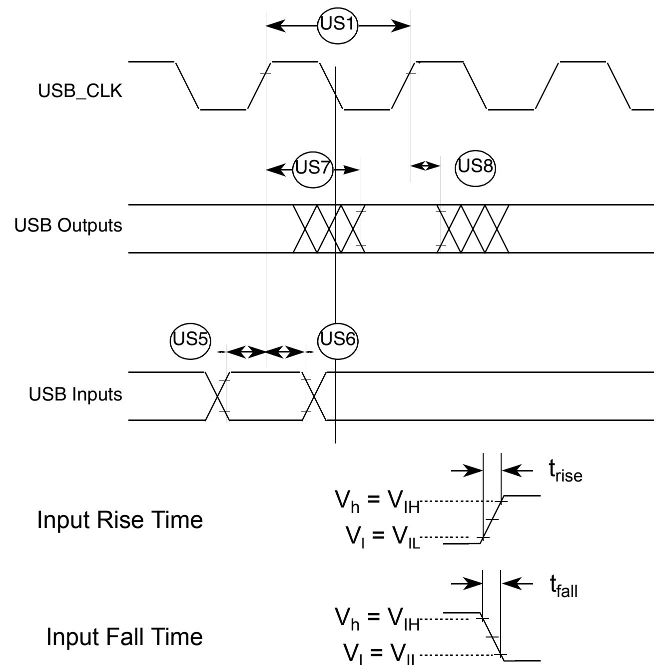


Figure 20. USB Signals Timing Diagram

8.12 I^2C Input/Output Timing Specifications

Table 23 lists specifications for the I^2C input timing parameters shown in Figure 21.

Table 23. I^2C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2 x t_{CYC}	—	ns
I2	Clock low period	8 x t_{CYC}	—	ns
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4 x t_{CYC}	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2 x t_{CYC}	—	ns
I9	Stop condition setup time	2 x t_{CYC}	—	ns

Table 24 lists specifications for the I^2C output timing parameters shown in Figure 21.

Table 24. I^2C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1 [1]	Start condition hold time	6 x t_{CYC}	—	ns
I2 [1]	Clock low period	10 x t_{CYC}	—	ns
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7 x t_{CYC}	—	ns
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10 x t_{CYC}	—	ns
I7 [1]	Data setup time	2 x t_{CYC}	—	ns
I8 [1]	Start condition setup time (for repeated start condition only)	20 x t_{CYC}	—	ns
I9 [1]	Stop condition setup time	10 x t_{CYC}	—	ns

[1] Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 24. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 24 are minimum values.

[2] Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

[3] Specified at a nominal 50-pF load.

Figure 21 shows timing for the values in Table 23 and Table 24.

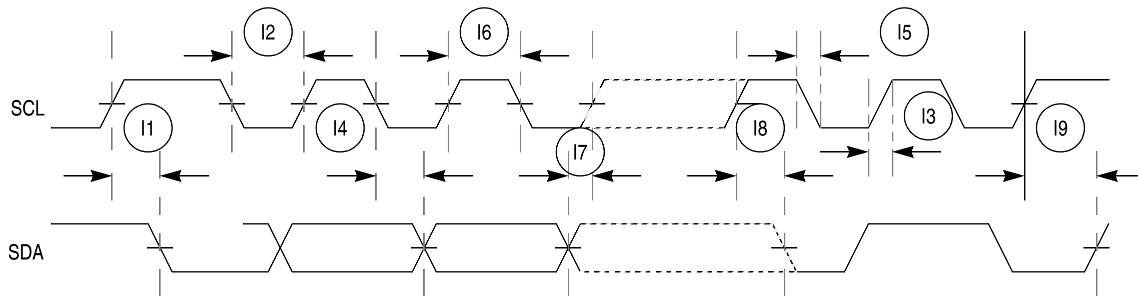


Figure 21. I²C Input/Output Timings

8.13 DMA Timers Timing Specifications

Table 25. Timer Module AC Timing Specifications

Name	Characteristic [1]	Min	Max	Unit
T1	T0IN / T1IN / T2IN / T3IN cycle time	3 x t_{CYC}	—	ns
T2	T0IN / T1IN / T2IN / T3IN pulse width	1 x t_{CYC}	—	ns

[1] All timing references to CLKOUT are given to its rising edge.

8.14 QSPI Electrical Specifications

Table 26. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

8.16 Debug AC Timing Specifications

Table 28 lists specifications for the debug AC timing parameters shown in Figure 28.

Table 28. Debug AC Timing Specification

Num	Characteristic	166 MHz		Units
		Min	Max	
D0	PSTCLK cycle time	—	0.5	t_{CYC}
D1	PST, DDATA to PSTCLK setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.0	—	ns
D3	DSI-to-DSCLK setup	1 x t_{CYC}	—	ns
D4 [1]	DSCLK-to-DSO hold	4 x t_{CYC}	—	ns
D5	DSCLK cycle time	5 x t_{CYC}	—	ns
D6	$\overline{\text{BKPT}}$ input data setup time to PSTCLK Rise	4	—	ns
D7	$\overline{\text{BKPT}}$ input data hold time to PSTCLK Rise	1.5	—	ns
D8	PSTCLK high to $\overline{\text{BKPT}}$ high Z	0.0	10.0	ns

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

Figure 27 shows real-time trace timing for the values in Table 28.

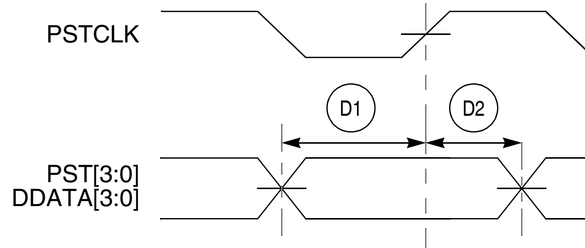


Figure 27. Real-Time Trace AC Timing

Figure 28 shows BDM serial port AC timing for the values in Table 28.

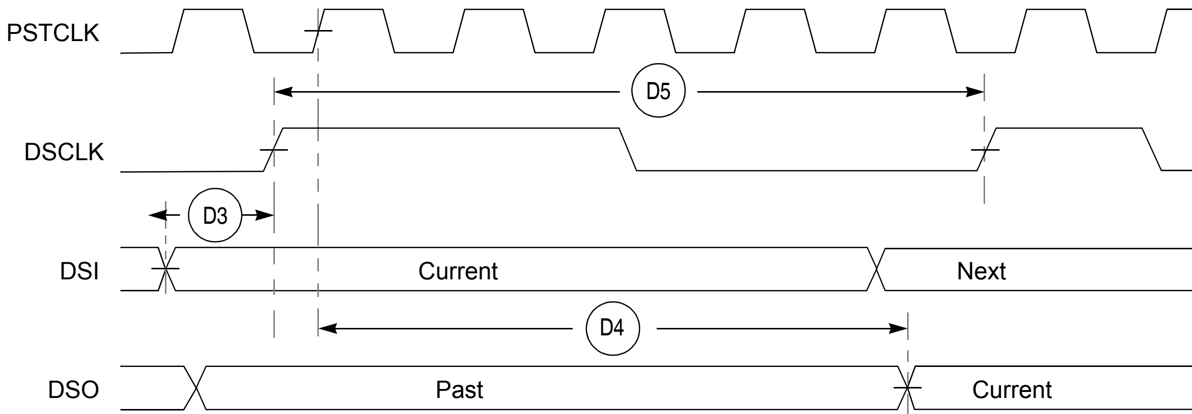


Figure 28. BDM Serial Port AC Timing

9 Documentation

Documentation regarding the MCF5275 and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

10 Revision History

Table 29 provides a revision history for this hardware specification.

Table 29. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.
1	Added Figure 6.
1.1	Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	Removed Overview, Features, Signal Descriptions, Modes of Operation, and Address Multiplexing sections. This information can be found in the MCF5275 Reference Manual. Removed list of documentation in Section 9, "Documentation.". An up-to-date list is always available on our web site. Changed CLKOUT -> PSTCLK in Section 8.16, "Debug AC Timing Specifications." Table 10: Update V_{DD} spec from 1.35-1.65 to 1.4-1.6. Table 13: Timings B6a, B6b, B6c, B7, B7a, B9, B12 updated: B6a, B6b, B6c maximum changed from "0.5t_{CYC} + 5" to "0.5t_{CYC} + 5.5" B7, B7a minimum changed from "0.5t_{CYC} + 1.5" to "0.5t_{CYC} + 1.0" B9, B11 minimum changed from "1.5" to "1.0"
1.3	Added Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions." Added thermal characteristics for 196 MAPBGA in Table 8. Updated package dimensions drawing, Figure 6.
2	Removed second sentence from Section 8.11.1, "MII Receive Signal Timing (FECn_RXD[3:0], FECn_RXDV, FECn_RXER, and FECn_RXCLK)," and Section 8.11.2, "MII Transmit Signal Timing (FECn_TXD[3:0], FECn_TXEN, FECn_TXER, FECn_TXCLK)," regarding no minimum frequency requirement for TXCLK. Removed third and fourth paragraphs from Section 8.11.2, "MII Transmit Signal Timing (FECn_TXD[3:0], FECn_TXEN, FECn_TXER, FECn_TXCLK)," as this feature is not supported on this device.
3	Corrected Ordering Information, Table 6. Figure 2: Moved $PLLV_{DD}$ from 1.5V to 3.3V supply line and corrected relevant text in sections below table. Table 10: Corrected maximum "Input High Voltage 3.3V I/O Pads", V_{IH} specification.
4	Table 10, added PLL supply voltage row