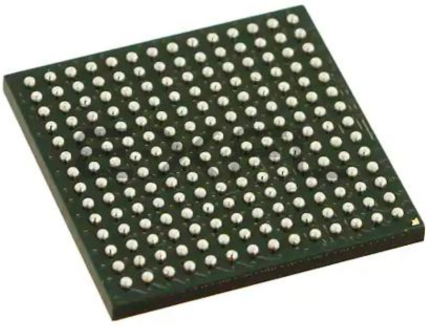

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, WDT
Number of I/O	61
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5275lcvm166

In addition, the MCF5275 family features an enhanced multiply accumulate unit (EMAC), large on-chip memory (64 Kbytes SRAM, 16 Kbytes configurable cache), and a 16-bit DDR SDRAM memory controller.

These devices are ideal for cost-sensitive applications requiring significant control processing for file management, connectivity, data buffering, and user interface, as well as signal processing in a variety of key markets such as security, imaging, networking, gaming, and medical. This leading package of integration and high performance allows fast time to market through easy code reuse and extensive third party tool support.

To locate any published errata or updates for this document, refer to the ColdFire products website at http://www.freescale.com/coldfire.

1 MCF5275 Family Configurations

Table 1. MCF5275 Family Configurations

Module	MCF5274L	MCF5275L	MCF5274	MCF5275
ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•
System Clock	up to 166 MHz			
Performance (Dhrystone 2.1 MIPS)	up to 159			
Instruction/Data Cache	16 Kbytes (configurable)			
Static RAM (SRAM)	64 Kbytes			
Interrupt Controllers (INTC)	2	2	2	2
Edge Port Module (EPORT)	•	•	•	•
External Interface Module (EIM)	•	•	•	•
4-channel Direct-Memory Access (DMA)	•	•	•	•
DDR SDRAM Controller	•	•	•	•
Fast Ethernet Controller (FEC)	1	1	2	2
Watchdog Timer Module (WDT)	•	•	•	•
4-channel Programmable Interval Timer Module (PIT)	•	•	•	•
32-bit DMA Timers	4	4	4	4
USB	•	•	•	•
QSPI	•	•	•	•
UART(s)	3	3	3	3
I^2C	•	•	•	•
PWM	4	4	4	4
General Purpose I/O Module (GPIO)	•	•	•	•
CIM = Chip Configuration Module + Reset Controller Module	•	•	•	•
Debug BDM	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•
Hardware Encryption	—	•	—	•
Package	196 MAPBGA		256 MAPBGA	

2 Block Diagram

The superset device in the MCF5275 family comes in a 256 Mold Array Plastic Ball Grid Array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5275, the superset device.

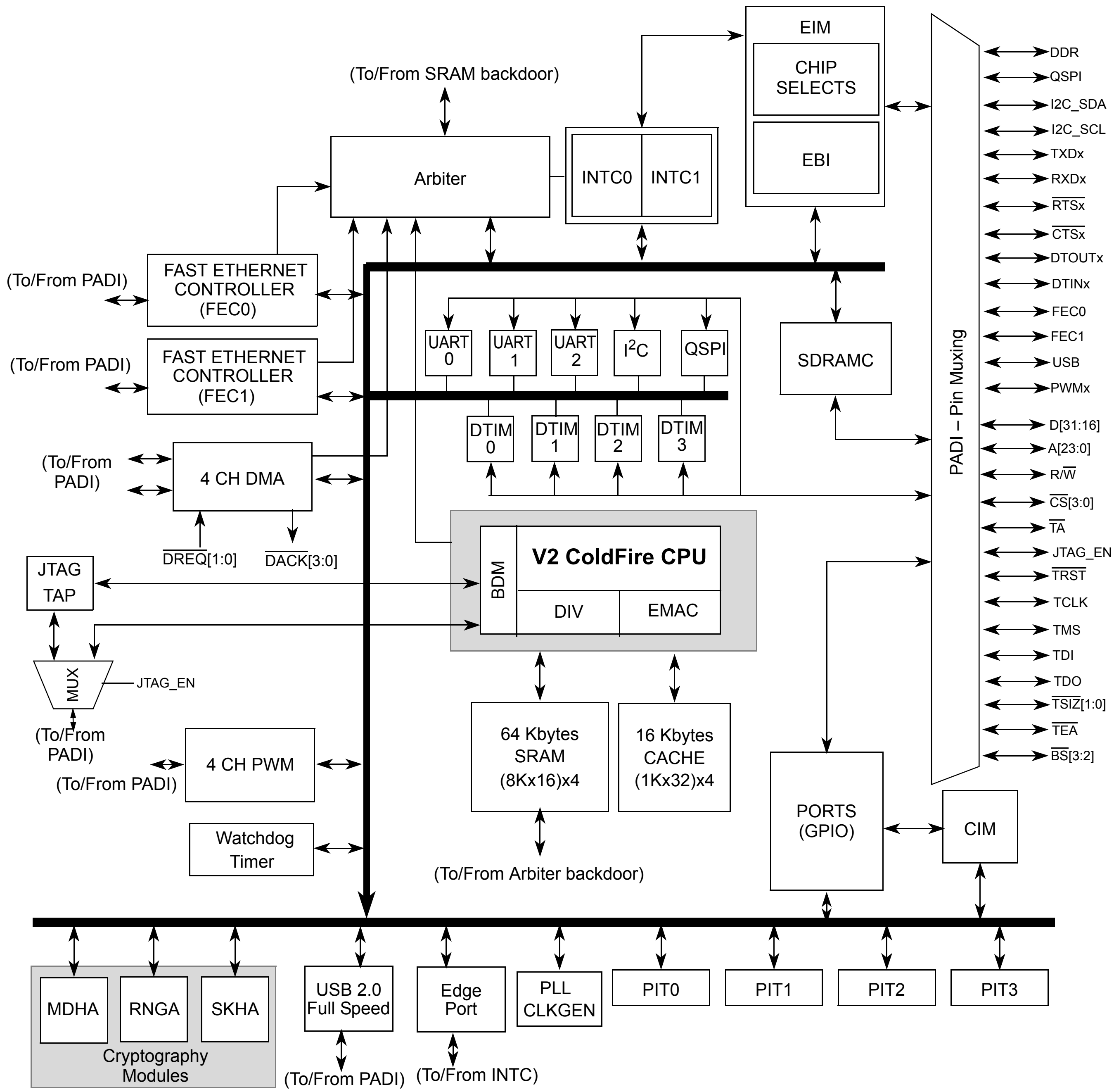

Figure 1. MCF5275 Block Diagram

3 Features

For a detailed feature list see the *MCF5275 Reference Manual* (MCF5275RM).

4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF5275 signals, consult the *MCF5275 Reference Manual* (MCF5275RM).

Table 2 lists the signals for the MCF5275 in functional group order. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts," for package diagrams.

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 2. MCF5274 and MCF5275 Signal Information and Muxing

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
Reset						
$\overline{\text{RESET}}$	—	—	—	I	N15	K12
$\overline{\text{RSTOUT}}$	—	—	—	O	N14	L12
Clock						
EXTAL	—	—	—	I	L16	M14
XTAL	—	—	—	O	M16	N14
CLKOUT	—	—	—	O	T12	P9
Mode Selection						
CLKMOD[1:0]	—	—	—	I	N13, P13	M11, N11
$\overline{\text{RCON}}$	—	—	—	I	P8	M6
External Memory Interface and Ports						
A[23:21]	PADDR[7:5]	$\overline{\text{CS}}$[6:4]	—	O	A11, B11, C11	A8, B8, C8
A[20:0]	—	—	—	O	A12, B12, C12, A13, B13, C13, A14, B14, C14, B15, C15, B16, C16, D14, D15, E14:16, F14:16	B9, D9, C9, C10, B10, A11, C11, B11, A12, D11, C12, B13, C13, D12, E11, D13, E12, F11, D14, E13, F13

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
D[31:16]	—	—	—	O	M1, N1, N2, N3, P1, P2, R1, R2, P3, R3, T3, N4, P4, R4, T4, N5	J3, L1, K2, K3, M1, L2, L3, L4, K4, J4, M2, N1, N2, M3, M4, N3
$\overline{\text{BS}}$[3:2]	$\overline{\text{PBS}}$[3:2]	$\overline{\text{CAS}}$[3:2]	—	O	M3, R5	K1, L5
$\overline{\text{OE}}$	PBUSCTL[7]	—	—	O	K1	H4
$\overline{\text{TA}}$	PBUSCTL[6]	—	—	I	L13	K14
$\overline{\text{TEA}}$	PBUSCTL[5]	$\overline{\text{DREQ1}}$	—	I	T8	—
R/$\overline{\text{W}}$	PBUSCTL[4]	—	—	O	P7	L6
TSIZ1	PBUSCTL[3]	DACK1	—	O	D16	B14
TSIZ0	PBUSCTL[2]	DACK0	—	O	G16	E14
$\overline{\text{TS}}$	PBUSCTL[1]	DACK2	—	O	L4	H2
$\overline{\text{TIP}}$	PBUSCTL[0]	$\overline{\text{DREQ0}}$	—	O	P6	—
Chip Selects						
$\overline{\text{CS}}$[7:1]	PCS[7:1]	—	—	O	D10:13, E13, F13, N7	D8, A9, A10, D10, B12, C14, P4
$\overline{\text{CS0}}$	—	—	—	O	R6	N5
DDR SDRAM Controller						
DDR_CLKOUT	—	—	—	O	T7	P6
$\overline{\text{DDR\_CLKOUT}}$	—	—	—	O	T6	P5
$\overline{\text{SD\_CS}}$[1:0]	PSDRAM[7:6]	$\overline{\text{CS}}$[3:2]	—	O	M2, T5	H3, M5
$\overline{\text{SD\_SRAS}}$	PSDRAM[5]	—	—	O	L2	H1
$\overline{\text{SD\_SCAS}}$	PSDRAM[4]	—	—	O	L1	G3
$\overline{\text{SD\_WE}}$	PSDRAM[3]	—	—	O	K2	G4
SD_A10	—	—	—	O	N6	N4
$\overline{\text{SD\_DQS}}$[3:2]	PSDRAM[2:1]	—	—	I/O	M4, P5	J2, P3
SD_CKE	PSDRAM[0]	—	—	O	L3	J1
SD_VREF	—	—	—	I	A15, T2	A13, P2
External Interrupts Port						
$\overline{\text{IRQ}}$[7:5]	PIRQ[7:5]	—	—	I	G13, H16, H15	F14, G13, G14
$\overline{\text{IRQ}}$[4]	PIRQ[4]	$\overline{\text{DREQ2}}$	—	I	H14	H11
$\overline{\text{IRQ}}$[3:2]	PIRQ[3:2]	$\overline{\text{DREQ}}$[3:2]	—	I	J14, J13	H14, H12

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
$\overline{IRQ1}$	PIRQ[1]	—	—	I	K13	J13
FEC0						
FEC0_MDIO	PFECI2C[5]	I2C_SDA	U2RXD	I/O	A7	A3
FEC0_MDC	PFECI2C[4]	I2C_SCL	U2TXD	O	B7	C5
FEC0_TXCLK	PFEC0H[7]	—	—	I	C3	C1
FEC0_TXEN	PFEC0H[6]	—	—	O	D4	C3
FEC0_TXD[0]	PFEC0H[5]	—	—	O	G4	D2
FEC0_COL	PFEC0H[4]	—	—	I	A6	B4
FEC0_RXCLK	PFEC0H[3]	—	—	I	B6	B3
FEC0_RXDV	PFEC0H[2]	—	—	I	B5	C4
FEC0_RXD[0]	PFEC0H[1]	—	—	I	C6	D5
FEC0_CRS	PFEC0H[0]	—	—	I	C7	A2
FEC0_TXD[3:1]	PFEC0L[7:5]	—	—	O	E3, F3, F4	D1, E3, D3
FEC0_TXER	PFEC0L[4]	—	—	O	D3	C2
FEC0_RXD[3:1]	PFEC0L[3:1]	—	—	I	D5, C5, D6	D4, B1, B2
FEC0_RXER	PFEC0L[0]	—	—	I	C4	E4
FEC1						
FEC1_MDIO	PFECI2C[3]	—	—	I/O	G1	—
FEC1_MDC	PFECI2C[2]	—	—	O	G2	—
FEC1_TXCLK	PFEC1H[7]	—	—	I	C1	—
FEC1_TXEN	PFEC1H[6]	—	—	O	D2	—
FEC1_TXD[0]	PFEC1H[5]	—	—	O	F1	—
FEC1_COL	PFEC1H[4]	—	—	I	A5	—
FEC1_RXCLK	PFEC1H[3]	—	—	I	B4	—
FEC1_RXDV	PFEC1H[2]	—	—	I	A3	—
FEC1_RXD[0]	PFEC1H[1]	—	—	I	B3	—
FEC1_CRS	PFEC1H[0]	—	—	I	A4	—
FEC1_TXD[3:1]	PFEC1L[7:5]	—	—	O	E1, E2, F2	—
FEC1_TXER	PFEC1L[4]	—	—	O	D1	—
FEC1_RXD[3:1]	PFEC1L[3:1]	—	—	I	B1, B2, A2	—
FEC1_RXER	PFEC1L[0]	—	—	I	C2	—

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
VSSPLL	—	—	—	I	K16	L13
VSS	—	—	—	I	A1, A10, A16, E5, E12, F6, F11, G7:10, H7:10, J1, J7:10, K7:10, L6, L11, M5, N16, R7, T1, T16	F7, F8, G6:9, H6:9, J7, J8
OVDD	—	—	—	I	E6:8, F5, F7, F8, G5, G6, H5, H6, J11, J12, K11, K12, L9, L10, L12, M9:11	E5:7, F5, F6, H10, J9, J10, K8:10
VDD	—	—	—	I	D8, H13, K4, N8	D6, G5, G12, L7
SD_VDD	—	—	—	I	E9:11, F9, F10, F12, G11, G12, H11, H12, J5, J6, K5, K6, L5, L7, L8, M6, M7, M8	E8:10, F9, F10, G10, H5, J5, J6, K5:7

1 Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

2 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5275.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33uF, 0.1 µF, and 0.01 µF across each power supply

5.2.1.2 Power Down Sequence

If V_{DD} is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after V_{DD} powers down before OV_{DD}, SDV_{DD}, or $PLLV_{DD}$ must power down. V_{DD} should not lag OV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or undesired high current will be in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop V_{DD} to 0 V.
2. Drop OV_{DD}/SDV_{DD}/$PLLV_{DD}$ supplies.

5.3 Decoupling

- Place the decoupling capacitors as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 µF and 0.01 µF at each supply input

5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See electricals.

5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

5.7 Interface Recommendations

5.7.1 DDR SDRAM Controller

5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

Table 3. Synchronous DRAM Signal Connections

Signal	Description
$\overline{\text{SD\_SRAS}}$	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SDRAM\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals.
$\overline{\text{SD\_SCAS}}$	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM.
$\overline{\text{SD\_WE}}$	DRAM read/write. Asserted for write operations and negated for read operations.
$\overline{\text{SD\_CS}}$[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF5275. One $\overline{\text{SDRAM\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
$\overline{\text{BS}}$[3:2]	Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:2] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
DDR_CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5275 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

The FEC supports an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF5275 Pin
Transmit clock	FEC*n*_TXCLK
Transmit enable	FEC*n*_TXEN
Transmit data	FEC*n*_TXD[3:0]
Transmit error	FEC*n*_TXER

Table 4. MII Mode (continued)

Signal Description	MCF5275 Pin
Collision	FEC*n*_COL
Carrier sense	FEC*n*_CRS
Receive clock	FEC*n*_RXCLK
Receive enable	FEC*n*_RXDV
Receive data	FEC*n*_RXD[3:0]
Receive error	FEC*n*_RXER
Management channel clock	FEC*n*_MDC
Management channel serial data	FEC*n*_MDIO

The serial mode interface operates in what is generally referred to as AMD mode. The MCF5275 configuration for seven-wire serial mode connections to the external transceiver are shown in Table 5.

Table 5. Seven-Wire Mode Configuration

Signal Description	MCF5275 Pin
Transmit clock	FEC*n*_TXCLK
Transmit enable	FEC*n*_TXEN
Transmit data	FEC*n*_TXD[0]
Collision	FEC*n*_COL
Receive clock	FEC*n*_RXCLK
Receive enable	FEC*n*_RXDV
Receive data	FEC*n*_RXD[0]
Unused, configure as PB14	FEC*n*_RXER
Unused input, tie to ground	FEC*n*_CRS
Unused, configure as PB[13:11]	FEC*n*_RXD[3:1]
Unused output, ignore	FEC*n*_TXER
Unused, configure as PB[10:8]	FEC*n*_TXD[3:1]
Unused, configure as PB15	FEC*n*_MDC
Input after reset, connect to ground	FEC*n*_MDIO

Refer to the M5275EVB evaluation board user’s manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5275 site by navigating to: http://www.freescale.com/coldfire.

5.7.3 BDM

Use the BDM interface as shown in the M5275EVB evaluation board user’s manual. The schematics for this board are accessible at the MCF5275 site by navigating to: http://www.freescale.com/coldfire.

6 Mechanicals/Pinouts

6.1 256 MAPBGA Pinout

Figure 3 is a consolidated MCF5274/75 pinout for the 256 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FEC1_RXD1	FEC1_RXDV	FEC1_CRS	FEC1_COL	FEC0_COL	FEC0_MDIO	U0RXD	U1RXD	VSS	A23	A20	A17	A14	SD_VREF	VSS	A
B	FEC1_RXD3	FEC1_RXD2	FEC1_RXD0	FEC1_RXCLK	FEC0_RXDV	FEC0_RXCLK	FEC0_MDC	U0TXD	U1TXD	I2C_SDA	A22	A19	A16	A13	A11	A9	B
C	FEC1_TXCLK	FEC1_RXER	FEC0_TXCLK	FEC0_RXER	FEC0_RXD2	FEC0_RXD0	FEC0_CRS	U0CTS	U1CTS	I2C_SCL	A21	A18	A15	A12	A10	A8	C
D	FEC1_TXER	FEC1_TXEN	FEC0_TXER	FEC0_TXEN	FEC0_RXD3	FEC0_RXD1	U0RTS	VDD	U1RTS	CS7	CS6	CS5	CS4	A7	A6	TSIZ1	D
E	FEC1_TXD3	FEC1_TXD2	FEC0_TXD3	NC	VSS	OVDD	OVDD	OVDD	SD_VDD	SD_VDD	SD_VDD	VSS	CS3	A5	A4	A3	E
F	FEC1_TXD0	FEC1_TXD1	FEC0_TXD2	FEC0_TXD1	OVDD	VSS	OVDD	OVDD	SD_VDD	SD_VDD	VSS	SD_VDD	CS2	A2	A1	A0	F
G	FEC1_MDIO	FEC1_MDC	DT0OUT	FEC0_TXD0	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	IRQ7	USB_SPEED	USB_CLK	TSIZ0	G
H	DT1IN	DT1OUT	DT0IN	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	VDD	IRQ4	IRQ5	IRQ6	H
J	VSS	DT2IN	DT2OUT	DT3IN	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	IRQ2	IRQ3	USB_RP	USB_RN	J
K	OE	SD_WE	DT3OUT	VDD	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	IRQ1	USB_TN	USB_TP	VSSPLL	K
L	SD_SCAS	SD_SRAS	SD_CKE	TS	SD_VDD	VSS	SD_VDD	SD_VDD	OVDD	OVDD	VSS	OVDD	TA	USB_TXEN	USB_RXD	EXTAL	L
M	D31	SD_CS1	BS3	SD_DQS3	VSS	SD_VDD	SD_VDD	SD_VDD	OVDD	OVDD	OVDD	NC	USB_SUSP	PLL_TEST	VDDPLL	XTAL	M
N	D30	D29	D28	D20	D16	SD_A10	CS1	VDD	TEST	DDATA2	DDATA0	QSPI_CS2	CLKMOD1	RSTOUT	RESET	VSS	N
P	D27	D26	D23	D19	SD_DQS2	TIP	R/W	RCON	U2CTS	DDATA3	DDATA1	QSPI_CS0	CLKMOD0	TRST/DSCLK	TDO/DSO	TCLK/PSTCLK	P
R	D25	D24	D22	D18	BS2	CS0	VSS	U2RTS	U2TXD	PST2	PST0	QSPI_DOUT	QSPI_CS3	JTAG_EN	TMS/BKPT	TDI/DSI	R
T	VSS	SD_VREF	D21	D17	SD_CS0	DDR_CLKOUT	DDR_CLKOUT	TEA	U2RXD	PST3	PST1	CLKOUT	QSPI_DIN	QSPI_CS1	QSPI_CLK	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. MCF5274 and MCF5275 Pinout (256 MAPBGA)

6.3 196 MAPBGA Pinout

Figure 5 is a consolidated MCF5274L/75L pinout for the 196 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	FEC0_CRS	FEC0_MDIO	U0RXD	U0TXD	U1RXD	I2C_SCL	A23	CS6	CS5	A15	A12	SD_VREF	NC	A
B	FEC0_RXD2	FEC0_RXD1	FEC0_RXCLK	FEC0_COL	U0RTS	U1RTS	I2C_SDA	A22	A20	A16	A13	CS3	A9	TSIZ1	B
C	FEC0_TXCLK	FEC0_TXER	FEC0_TXEN	FEC0_RXDV	FEC0_MDC	U0CTS	U1CTS	A21	A18	A17	A14	A10	A8	CS2	C
D	FEC0_TXD3	FEC0_TXD0	FEC0_TXD1	FEC0_RXD3	FEC0_RXD0	VDD	U1TXD	CS7	A19	CS4	A11	A7	A5	A2	D
E	DT0IN	DT0OUT	FEC0_TXD2	FEC0_RXER	OVDD	OVDD	OVDD	SD_VDD2	SD_VDD2	SD_VDD2	A6	A4	A1	TSIZ0	E
F	DT1IN	DT1OUT	DT2IN	DT2OUT	OVDD	OVDD	VSS	VSS	SD_VDD2	SD_VDD2	A3	USB_CLK	A0	IRQ7	F
G	DT3OUT	DT3IN	SD_CAS	SD_WE	VDD	VSS	VSS	VSS	VSS	SD_VDD2	USB_SPEED	VDD	IRQ6	IRQ5	G
H	SD_SRAS	TS	SD_CS1	OE	SD_VDD1	VSS	VSS	VSS	VSS	OVDD	IRQ4	IRQ2	USB_RN	IRQ3	H
J	SD_CKE	SD_DQS3	D31	D22	SD_VDD1	SD_VDD1	VSS	VSS	OVDD	OVDD	USB_RP	USB_TP	IRQ1	USB_TN	J
K	BS3	D29	D28	D23	SD_VDD1	SD_VDD1	SD_VDD1	OVDD	OVDD	OVDD	TDO/DSO	RESET	USB_TXEN	TA	K
L	D30	D26	D25	D24	BS2	R/W	VDD	PST2	DDATA0	QSPI_DOUT	QSPI_CLK	RSTOUT	VSSPLL	USB_RXD	L
M	D27	D21	D18	D17	SD_CS0	RCON	DDATA3	PST1	QSPI_CS0	QSPI_DIN	CLKMOD1	TDI/DSI	VDDPLL	EXTAL	M
N	D20	D19	D16	SD_A10	CS0	TEST	DDATA2	PST0	QSPI_CS2	QSPI_CS1	CLKMOD0	TMS/BKPT	USB_SUSP	XTAL	N
P	NC	SD_VREF	SD_DQS2	CS1	DDR_CLKOUT	DDR_CLKOUT	PST3	DDATA1	CLKOUT	QSPI_CS3	JTAG_EN	TCLK/PSTCLK	TRST/DSCLK	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 5. MCF5274L and MCF5275L Pinout (196 MAPBGA)

8.4 DC Electrical Specifications

Table 10. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	V_{DD}	1.4	1.6	V
I/O Pad Supply Voltage	OV_{DD}	3.0	3.6	V
PLL Supply Voltage	V_{DDPLL}	3.0	3.6	V
SSTL I/O Pad Supply Voltage	SDV_{DD}	2.3	2.7	V
SSTL I/O Pad Supply Voltage	SDV_{DD}	3.0	3.6	V
SSTL Memory pads reference voltage (SD V_{DD} = 2.5V)	V_{REF}	0.5 SD V_{DD}	—[2]	V
SSTL Memory pads reference voltage (SD V_{DD} = 3.3V)	V_{REF}	0.45 SD V_{DD}	—[2]	V
Input High Voltage 3.3V I/O Pads	V_{IH}	0.7 x OV_{DD}	OV_{DD} + 0.3	V
Input Low Voltage 3.3V I/O Pads	V_{IL}	V_{SS} – 0.3	0.35 x OV_{DD}	V
Output High Voltage 3.3V I/O Pads I_{OH} = –2.0 mA	V_{OH}	OV_{DD} - 0.5	—	V
Output Low Voltage 3.3V I/O Pads I_{OL} = 2.0mA	V_{OL}	—	0.5	V
Input Hysteresis 3.3V I/O Pads	V_{HYS}	0.06 x V_{DD}	—	mV
Input High Voltage SSTL 3.3V/2.5V[3]	V_{IH}	V_{REF} + 0.3	SDV_{DD} + 0.3	V
Input Low Voltage SSTL 3.3V/2.5V[3]	V_{IL}	V_{SS} - 0.3	V_{REF} - 0.3	V
Output High Voltage SSTL 3.3V/2.5V[4] I_{OH} = –5.0 mA	V_{OH}	SDV_{DD} - 0.25V	—	V
Output Low Voltage SSTL 3.3V/2.5V[4] I_{OL} = 5.0 mA	V_{OL}	—	0.35	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	-1.0	1.0	μA
High Impedance (Off-State) Leakage Current V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	-1.0	1.0	μA
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[5]	I_{APU}	-10	-130	μA
Input Capacitance [6] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

8.5 Oscillator and Phase Lock Loop (PLLMRFM) Electrical Specifications

Table 11. PLL Electrical Specifications[1]

Characteristic	Symbol	Min	Max	Unit
PLL Reference Frequency Range Crystal reference External reference 1:1 Mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 25 25 83	MHz
Core frequency CLKOUT Frequency [2] External reference On-Chip PLL Frequency	f_{core} $f_{sys/2}$	 0 f_{ref} / 32	166 83 83	MHz MHz MHz
Loss of Reference Frequency [3, 5]	f_{LOR}	100	1000	kHz
Self Clocked Mode Frequency [4, 5]	f_{SCM}	TBD	TBD	MHz
Crystal Start-up Time [5, 6]	t_{cst}	—	10	ms
EXTAL Input High Voltage Crystal Mode All other modes (Dual Controller (1:1), Bypass, External)	V_{IHEXT} V_{IHEXT}	 TBD TBD	 TBD TBD	V
EXTAL Input Low Voltage Crystal Mode All other modes (Dual Controller (1:1), Bypass, External)	V_{ILEXT} V_{ILEXT}	 TBD TBD	 TBD TBD	V
XTAL Output High Voltage I_{OH} = 1.0 mA	V_{OH}	 TBD	 —	V
XTAL Output Low Voltage I_{OL} = 1.0 mA	V_{OL}	 —	 TBD	V
XTAL Load Capacitance[7]		5	30	pF
PLL Lock Time [8]	t_{lpll}	—	750	µs
Power-up To Lock Time [6, 9] With Crystal Reference Without Crystal Reference[10]	t_{lplk}	 — —	 11 750	 ms µs
1:1 Mode Clock Skew (between CLKOUT and EXTAL) [11]	t_{skew}	-1	1	ns
Duty Cycle of reference [5]	t_{dc}	40	60	% $f_{sys/2}$
Frequency un-LOCK Range	f_{UL}	-3.8	4.1	% $f_{sys/2}$
Frequency LOCK Range	f_{LCK}	-1.7	2.0	% $f_{sys/2}$
CLKOUT Period Jitter, [5, 6, 9,12, 13] Measured at $f_{sys/2}$ Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	 — —	 5 .01	% $f_{sys/2}$
Frequency Modulation Range Limit[14, 15] ($f_{sys/2}$Max must not be exceeded)	C_{mod}	0.8	2.2	% $f_{sys/2}$
ICO Frequency. $f_{ico} = f_{ref} * 2 * (MFD+2)$[16]	f_{ico}	48	83	MHz

1 All values given are initial design targets and subject to change.
2 All internal registers retain data at 0 Hz.
3 “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.

Figure 10 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 13.

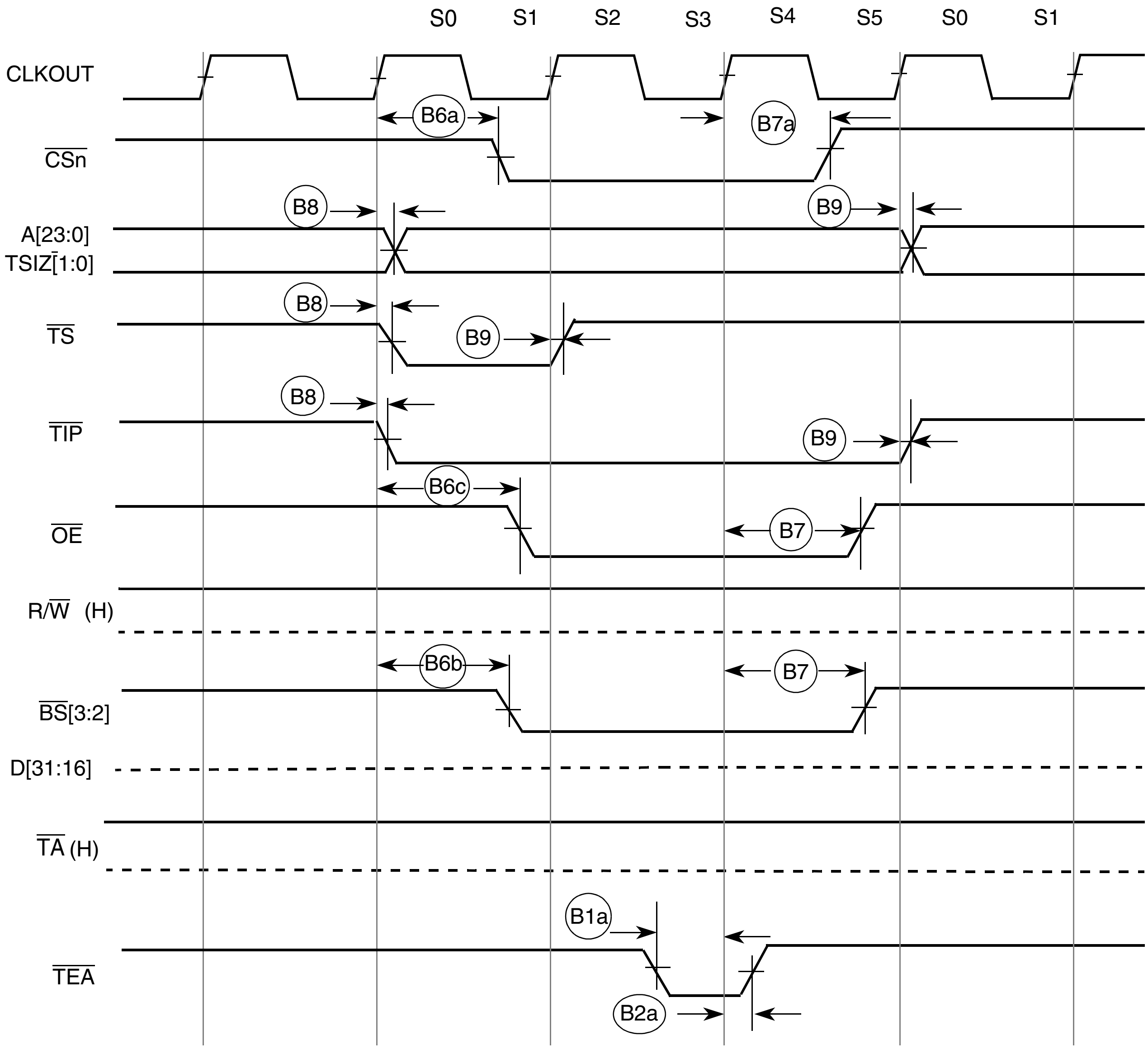

Figure 10. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$

8.8 DDR SDRAM AC Timing Characteristics

The DDR SDRAM controller uses SSTL2 and I/O drivers. Class I or Class II drive strength is available and is user programmable. DDR Clock timing specifications are given in Table 14 and Figure 11.

Table 14. DDR Clock Timing Specifications[1]

Symbol	Characteristic	Min	Max	Unit
V_{MP}	Clock output mid-point voltage	1.05	1.45	V
V_{OUT}	Clock output voltage level	-0.3	SDV_{DD} + 0.3	V
V_{ID}	Clock output differential voltage (peak to peak swing)	0.7	SDV_{DD} + 0.6	V
V_{IX}	Clock crossing point voltage	1.05	1.45	V

[1] SD V_{DD} is nominally 2.5V.

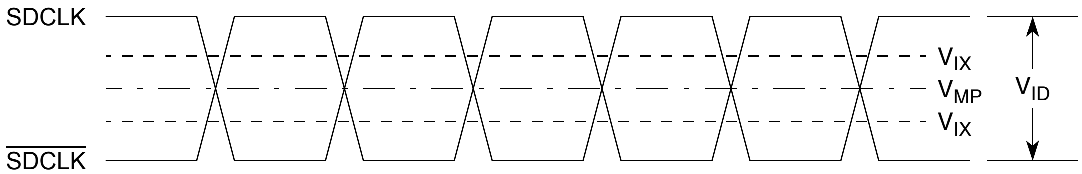

Figure 11. DDR Clock Timing Diagram

When using the DDR SDRAM controller the timing numbers in Table 15 must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the two DQS byte lanes.

Table 15. DDR Timing

NUM	Characteristic[1]	Symbol	Min	Max	Unit
	Frequency of operation[2]		TBD	83	MHz
DD1	Clock Period (DDR_CLKOUT)	t_{CK}	12	TBD	ns
DD2	Pulse Width High[3]	t_{CKH}	0.45	0.55	t_{CK}
DD3	Pulse Width Low[3]	t_{CKl}	0.45	0.55	t_{CK}
DD4	DDR_CLKOUT high to DDR address, SD_CKE, SD_CS[1:0], SD_SCAS, SD_SRAS, SD_WE valid	t_{CMV}	—	0.5 x t_{CK} + 1	ns
DD5	DDR_CLKOUT high to DDR address, SD_CKE, $\overline{\text{SD\_CS}}$, $\overline{\text{SD\_SCAS}}$, $\overline{\text{SD\_SRAS}}$, $\overline{\text{SD\_WE}}$ invalid	t_{CMH}	2	—	ns
DD6	Write command to first $\overline{\text{SD\_DQS}}$ Latching Transition	t_{DQSS}	—	1.25	t_{CK}
DD7	$\overline{\text{SD\_DQS}}$ high to Data and DM valid (write) - setup[4,5]	t_{QS}	1.5	—	ns
DD8	$\overline{\text{SD\_DQS}}$ high to Data and DM invalid (write) - hold[4]	t_{QH}	1	—	ns
DD9	$\overline{\text{SD\_DQS}}$ high to Data valid (read) - setup[6]	t_{IS}	—	1	ns
DD10	$\overline{\text{SD\_DQS}}$ high to Data invalid (read) - hold[7]	t_{IH}	0.25 x t_{CK} + 1	—	ns
DD11	$\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - setup	t_{DSS}	0.5	—	ns
DD12	$\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - hold	t_{DSH}	0.5	—	ns

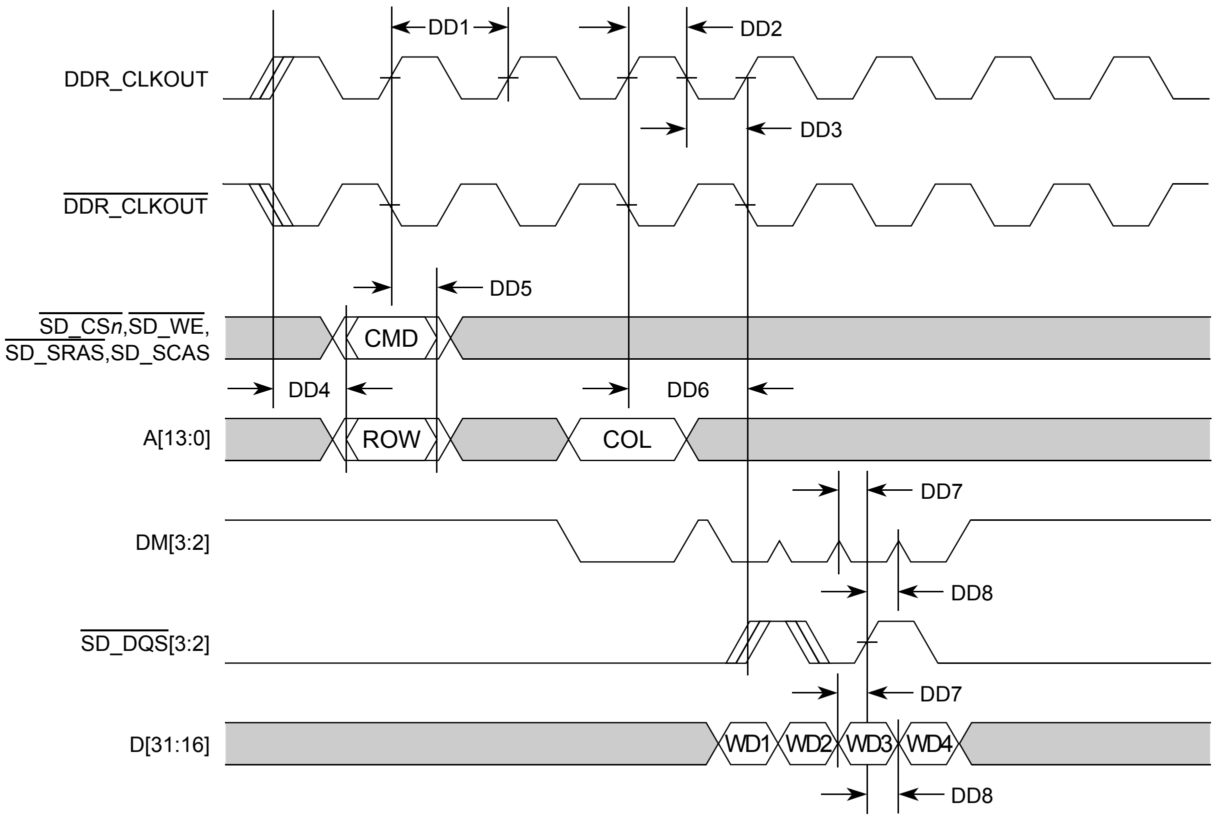

Figure 13. DDR Write Timing

Table 19. MII Transmit Channel Timing

Num	Characteristic	Min	Max	Unit
M5	FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER invalid	5	—	ns
M6	FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER valid	—	25	ns
M7	FEC*n*_TXCLK pulse width high	35%	65%	FEC*n*_TXCLK period
M8	FEC*n*_TXCLK pulse width low	35%	65%	FEC*n*_TXCLK period

Figure 17 shows MII transmit signal timings listed in Table 19.

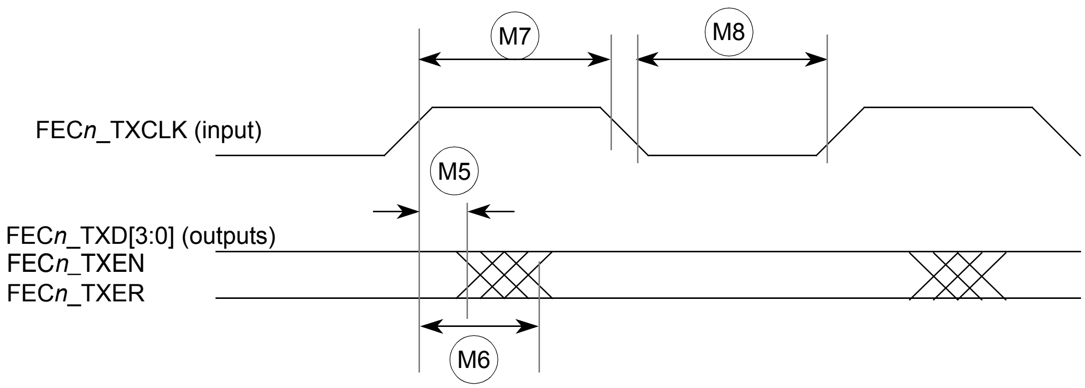

Figure 17. MII Transmit Signal Timing Diagram

8.11.3 MII Async Inputs Signal Timing (FEC*n*_CRS and FEC*n*_COL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Asynchronous Input Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC*n*_CRS, FEC*n*_COL minimum pulse width	1.5	—	FEC*n*_TXCLK period

Figure 18 shows MII asynchronous input timings listed in Table 20.

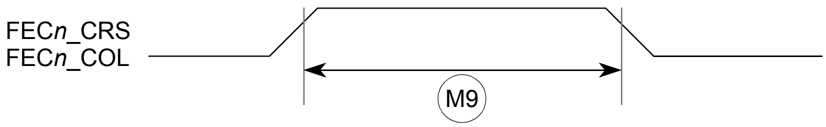

Figure 18. MII Async Inputs Timing Diagram

8.11.4 MII Serial Management Channel Timing (FEC*n*_MDIO and FEC*n*_MDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC*n*_MDC falling edge to FEC*n*_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC*n*_MDC falling edge to FEC*n*_MDIO output valid (max prop delay)	—	25	ns
M12	FEC*n*_MDIO (input) to FEC*n*_MDC rising edge setup	10	—	ns
M13	FEC*n*_MDIO (input) to FEC*n*_MDC rising edge hold	0	—	ns
M14	FEC*n*_MDC pulse width high	40%	60%	MDC period
M15	FEC*n*_MDC pulse width low	40%	60%	MDC period

Figure 19 shows MII serial management channel timings listed in Table 21.

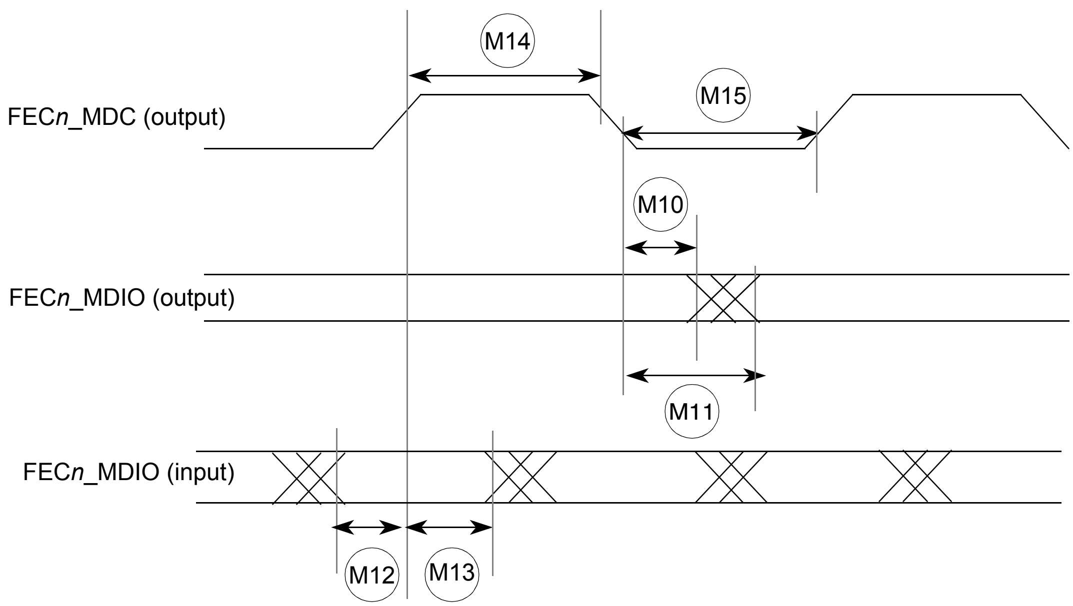

Figure 19. MII Serial Management Channel Timing Diagram

8.11.5 USB Interface AC Timing Specifications

Table 22 lists USB Interface timings.

Table 22. USB Interface Timing

Num	Characteristic	Min	Max	Units
US1	USB_CLK frequency of operation	48	48	MHz
US2	USB_CLK fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	2	ns
US3	USB_CLK rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	2	ns
US4	USB_CLK duty cycle (at 0.5 x O V_{DD})	45	55	%
Data Inputs				
US5	USB_RP, USB_RN, USB_RXD valid to USB_CLK high	6	—	ns
US6	USB_CLK high to USB_RP, USB_RN, USB_RXD invalid	6	—	ns
Data Outputs				
US7	USB_CLK high to USB_TP, USB_TN, USB_SUSP valid	—	12	ns
US8	USB_CLK high to USB_TP, USB_TN, USB_SUSP invalid	3	—	ns

Figure 20 shows USB interface timings listed in Table 22.

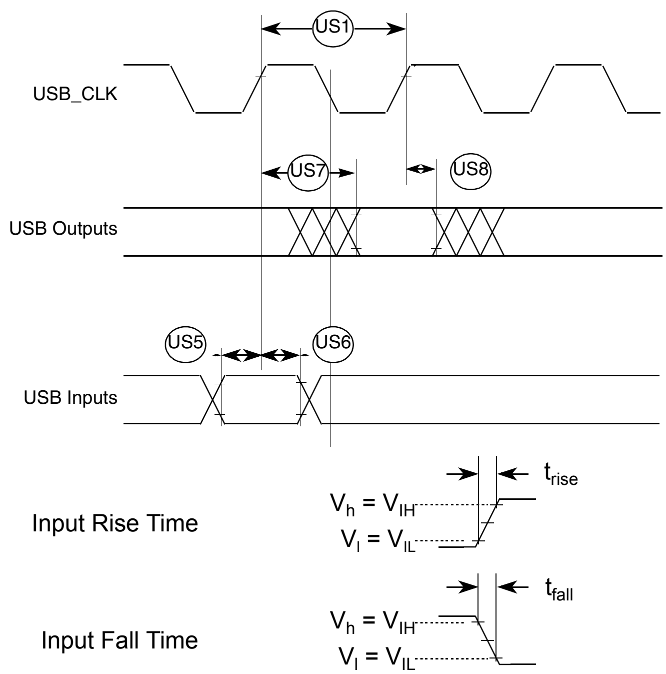

Figure 20. USB Signals Timing Diagram

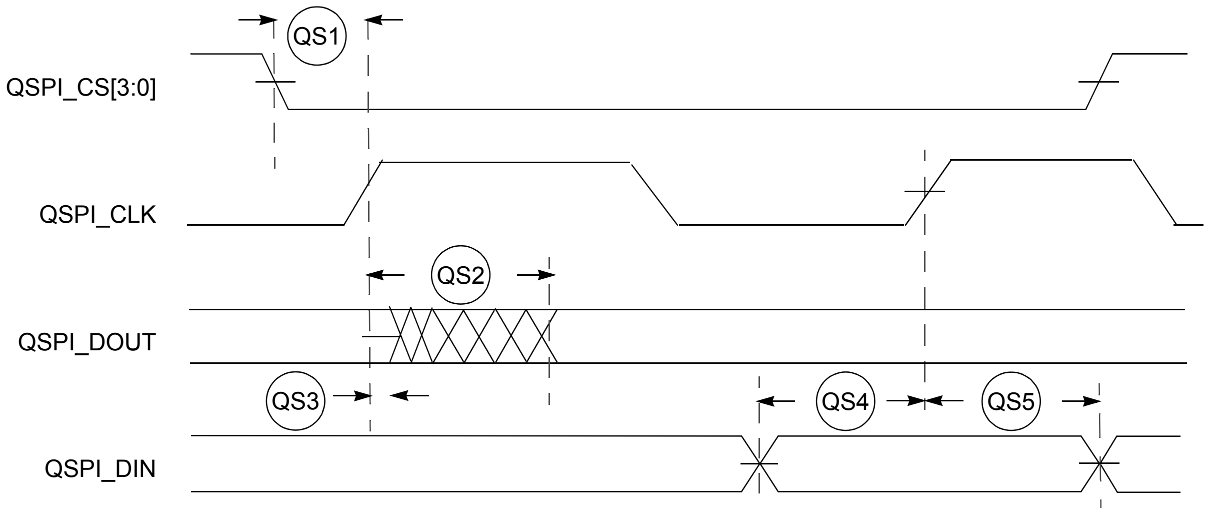

Figure 22. QSPI Timing

8.15 JTAG and Boundary Scan Timing

Table 27. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4 x t_{CYC}	—	ns
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

[1] JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.