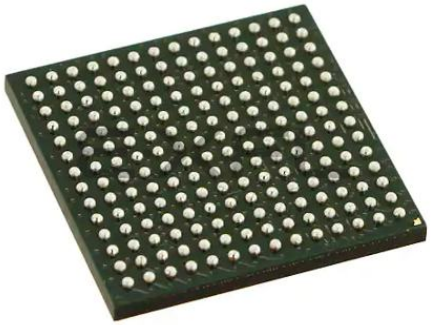

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, WDT
Number of I/O	61
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5275lcvm166j

2 Block Diagram

The superset device in the MCF5275 family comes in a 256 Mold Array Plastic Ball Grid Array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5275, the superset device.

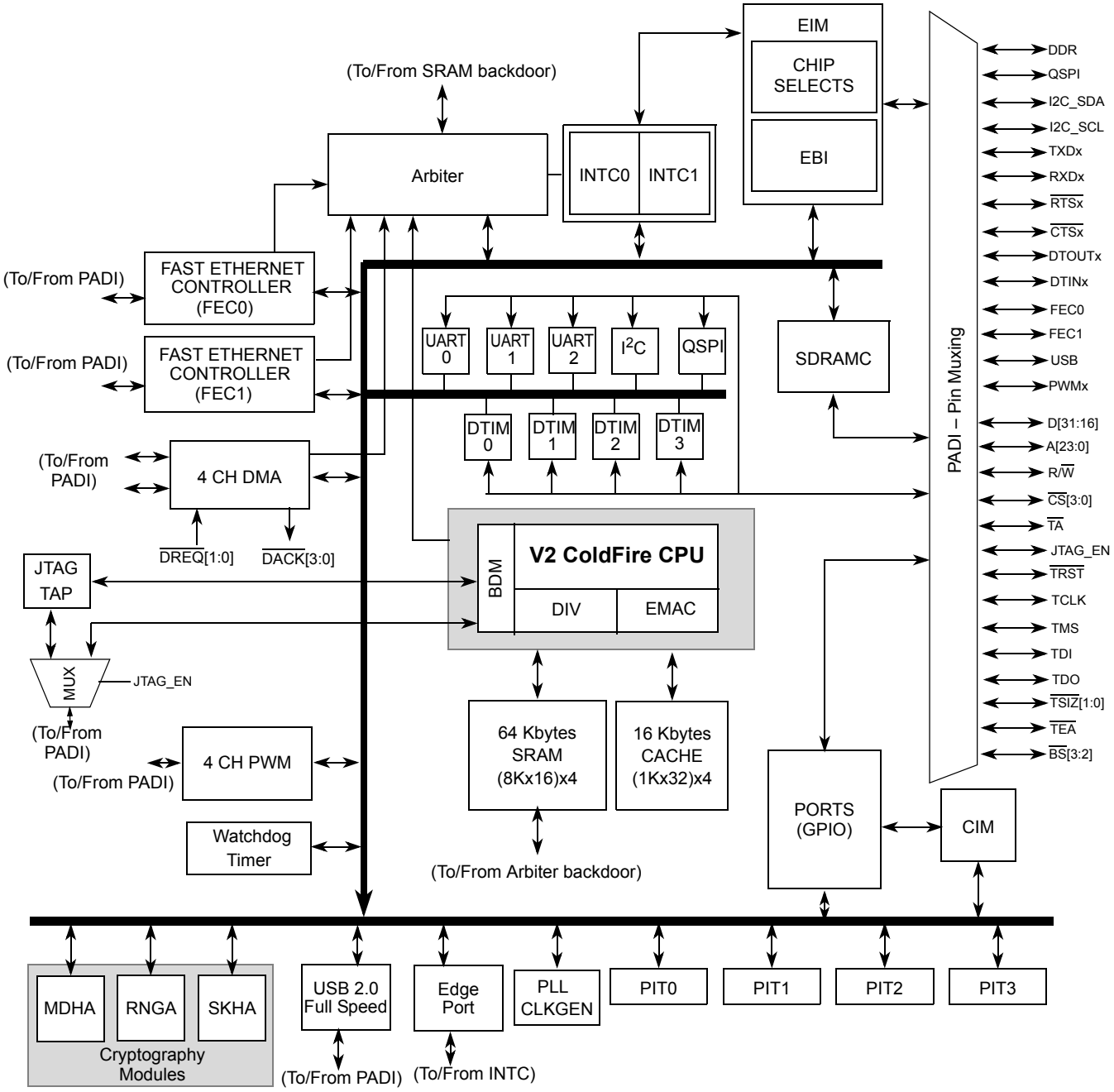


Figure 1. MCF5275 Block Diagram

3 Features

For a detailed feature list see the *MCF5275 Reference Manual* (MCF5275RM).

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
D[31:16]	—	—	—	O	M1, N1, N2, N3, P1, P2, R1, R2, P3, R3, T3, N4, P4, R4, T4, N5	J3, L1, K2, K3, M1, L2, L3, L4, K4, J4, M2, N1, N2, M3, M4, N3
$\overline{BS}$[3:2]	$\overline{PBS}$[3:2]	$\overline{CAS}$[3:2]	—	O	M3, R5	K1, L5
$\overline{OE}$	PBUSCTL[7]	—	—	O	K1	H4
$\overline{TA}$	PBUSCTL[6]	—	—	I	L13	K14
$\overline{TEA}$	PBUSCTL[5]	$\overline{DREQ1}$	—	I	T8	—
R/$\overline{W}$	PBUSCTL[4]	—	—	O	P7	L6
TSIZ1	PBUSCTL[3]	DACK1	—	O	D16	B14
TSIZ0	PBUSCTL[2]	DACK0	—	O	G16	E14
$\overline{TS}$	PBUSCTL[1]	DACK2	—	O	L4	H2
$\overline{TIP}$	PBUSCTL[0]	$\overline{DREQ0}$	—	O	P6	—
Chip Selects						
$\overline{CS}$[7:1]	PCS[7:1]	—	—	O	D10:13, E13, F13, N7	D8, A9, A10, D10, B12, C14, P4
$\overline{CS0}$	—	—	—	O	R6	N5
DDR SDRAM Controller						
DDR_CLKOUT	—	—	—	O	T7	P6
$\overline{DDR\_CLKOUT}$	—	—	—	O	T6	P5
$\overline{SD\_CS}$[1:0]	PSDRAM[7:6]	$\overline{CS}$[3:2]	—	O	M2, T5	H3, M5
$\overline{SD\_SRAS}$	PSDRAM[5]	—	—	O	L2	H1
$\overline{SD\_SCAS}$	PSDRAM[4]	—	—	O	L1	G3
$\overline{SD\_WE}$	PSDRAM[3]	—	—	O	K2	G4
SD_A10	—	—	—	O	N6	N4
$\overline{SD\_DQS}$[3:2]	PSDRAM[2:1]	—	—	I/O	M4, P5	J2, P3
SD_CKE	PSDRAM[0]	—	—	O	L3	J1
SD_VREF	—	—	—	I	A15, T2	A13, P2
External Interrupts Port						
$\overline{IRQ}$[7:5]	PIRQ[7:5]	—	—	I	G13, H16, H15	F14, G13, G14
$\overline{IRQ}$[4]	PIRQ[4]	$\overline{DREQ2}$	—	I	H14	H11
$\overline{IRQ}$[3:2]	PIRQ[3:2]	$\overline{DREQ}$[3:2]	—	I	J14, J13	H14, H12

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
$\overline{\text{IRQ1}}$	PIRQ[1]	—	—	I	K13	J13
FEC0						
FEC0_MDIO	PFECI2C[5]	I2C_SDA	U2RXD	I/O	A7	A3
FEC0_MDC	PFECI2C[4]	I2C_SCL	U2TXD	O	B7	C5
FEC0_TXCLK	PFEC0H[7]	—	—	I	C3	C1
FEC0_TXEN	PFEC0H[6]	—	—	O	D4	C3
FEC0_TXD[0]	PFEC0H[5]	—	—	O	G4	D2
FEC0_COL	PFEC0H[4]	—	—	I	A6	B4
FEC0_RXCLK	PFEC0H[3]	—	—	I	B6	B3
FEC0_RXDV	PFEC0H[2]	—	—	I	B5	C4
FEC0_RXD[0]	PFEC0H[1]	—	—	I	C6	D5
FEC0_CRS	PFEC0H[0]	—	—	I	C7	A2
FEC0_TXD[3:1]	PFEC0L[7:5]	—	—	O	E3, F3, F4	D1, E3, D3
FEC0_TXER	PFEC0L[4]	—	—	O	D3	C2
FEC0_RXD[3:1]	PFEC0L[3:1]	—	—	I	D5, C5, D6	D4, B1, B2
FEC0_RXER	PFEC0L[0]	—	—	I	C4	E4
FEC1						
FEC1_MDIO	PFECI2C[3]	—	—	I/O	G1	—
FEC1_MDC	PFECI2C[2]	—	—	O	G2	—
FEC1_TXCLK	PFEC1H[7]	—	—	I	C1	—
FEC1_TXEN	PFEC1H[6]	—	—	O	D2	—
FEC1_TXD[0]	PFEC1H[5]	—	—	O	F1	—
FEC1_COL	PFEC1H[4]	—	—	I	A5	—
FEC1_RXCLK	PFEC1H[3]	—	—	I	B4	—
FEC1_RXDV	PFEC1H[2]	—	—	I	A3	—
FEC1_RXD[0]	PFEC1H[1]	—	—	I	B3	—
FEC1_CRS	PFEC1H[0]	—	—	I	A4	—
FEC1_TXD[3:1]	PFEC1L[7:5]	—	—	O	E1, E2, F2	—
FEC1_TXER	PFEC1L[4]	—	—	O	D1	—
FEC1_RXD[3:1]	PFEC1L[3:1]	—	—	I	B1, B2, A2	—
FEC1_RXER	PFEC1L[0]	—	—	I	C2	—

Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate1	Alternate2	Dir.[1]	MCF5274 MCF5275 256 MAPBGA	MCF5274L MCF5275L 196 MAPBGA
VSSPLL	—	—	—	I	K16	L13
VSS	—	—	—	I	A1, A10, A16, E5, E12, F6, F11, G7:10, H7:10, J1, J7:10, K7:10, L6, L11, M5, N16, R7, T1, T16	F7, F8, G6:9, H6:9, J7, J8
OVDD	—	—	—	I	E6:8, F5, F7, F8, G5, G6, H5, H6, J11, J12, K11, K12, L9, L10, L12, M9:11	E5:7, F5, F6, H10, J9, J10, K8:10
VDD	—	—	—	I	D8, H13, K4, N8	D6, G5, G12, L7
SD_VDD	—	—	—	I	E9:11, F9, F10, F12, G11, G12, H11, H12, J5, J6, K5, K6, L5, L7, L8, M6, M7, M8	E8:10, F9, F10, G10, H5, J5, J6, K5:7

[1] Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

[2] If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

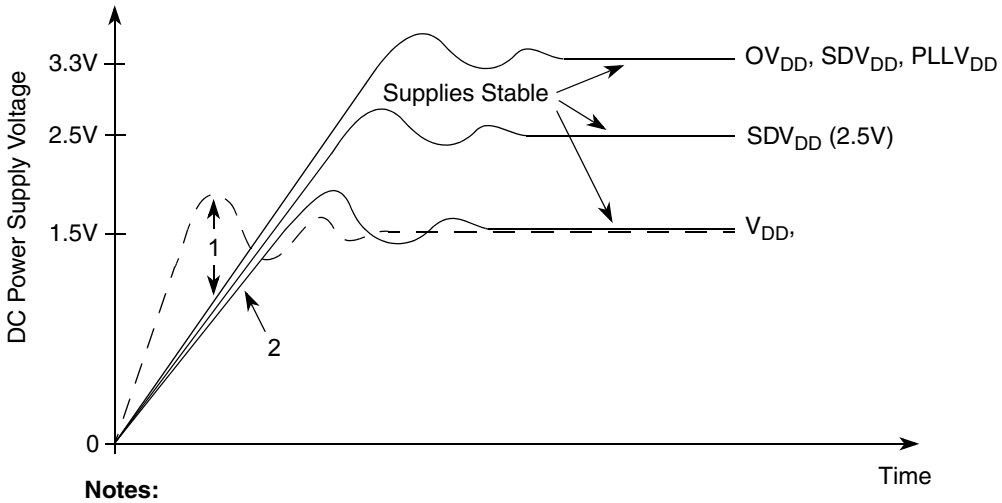
- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5275.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33uF, 0.1 µF, and 0.01 µF across each power supply

5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O V_{DD} (OV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} ($PLLV_{DD}$), and Core V_{DD} (V_{DD}).



Notes:
1. VDD should not exceed OVDD, SDVDD or PLLVDD by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/SDVDD/PLLVDD up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, SDVDD, VDD, or PLLVDD) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 2. Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and OV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and OV_{DD} are specified relative to V_{DD}.

5.2.1.1 Power Up Sequence

If OV_{DD}/SDV_{DD} are powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD}/SDV_{DD} powers up before V_{DD} must powered up. V_{DD} should not lead the OV_{DD}, SDV_{DD}, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or high current will be in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 µs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 µs or slower rise time for all supplies.
2. V_{DD}/$PLLV_{DD}$ and OV_{DD}/SDV_{DD} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD}/SD V_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

5.2.1.2 Power Down Sequence

If V_{DD} is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after V_{DD} powers down before OV_{DD}, SDV_{DD}, or $PLLV_{DD}$ must power down. V_{DD} should not lag OV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or undesired high current will be in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop V_{DD} to 0 V.
2. Drop OV_{DD}/SDV_{DD}/$PLLV_{DD}$ supplies.

5.3 Decoupling

- Place the decoupling capacitors as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 µF and 0.01 µF at each supply input

5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See electricals.

5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

Table 4. MII Mode (continued)

Signal Description	MCF5275 Pin
Collision	FEC*n*_COL
Carrier sense	FEC*n*_CRS
Receive clock	FEC*n*_RXCLK
Receive enable	FEC*n*_RXDV
Receive data	FEC*n*_RXD[3:0]
Receive error	FEC*n*_RXER
Management channel clock	FEC*n*_MDC
Management channel serial data	FEC*n*_MDIO

The serial mode interface operates in what is generally referred to as AMD mode. The MCF5275 configuration for seven-wire serial mode connections to the external transceiver are shown in Table 5.

Table 5. Seven-Wire Mode Configuration

Signal Description	MCF5275 Pin
Transmit clock	FEC*n*_TXCLK
Transmit enable	FEC*n*_TXEN
Transmit data	FEC*n*_TXD[0]
Collision	FEC*n*_COL
Receive clock	FEC*n*_RXCLK
Receive enable	FEC*n*_RXDV
Receive data	FEC*n*_RXD[0]
Unused, configure as PB14	FEC*n*_RXER
Unused input, tie to ground	FEC*n*_CRS
Unused, configure as PB[13:11]	FEC*n*_RXD[3:1]
Unused output, ignore	FEC*n*_TXER
Unused, configure as PB[10:8]	FEC*n*_TXD[3:1]
Unused, configure as PB15	FEC*n*_MDC
Input after reset, connect to ground	FEC*n*_MDIO

Refer to the M5275EVB evaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5275 site by navigating to: http://www.freescale.com/coldfire.

5.7.3 BDM

Use the BDM interface as shown in the M5275EVB evaluation board user's manual. The schematics for this board are accessible at the MCF5275 site by navigating to: http://www.freescale.com/coldfire.

6 Mechanicals/Pinouts

6.1 256 MAPBGA Pinout

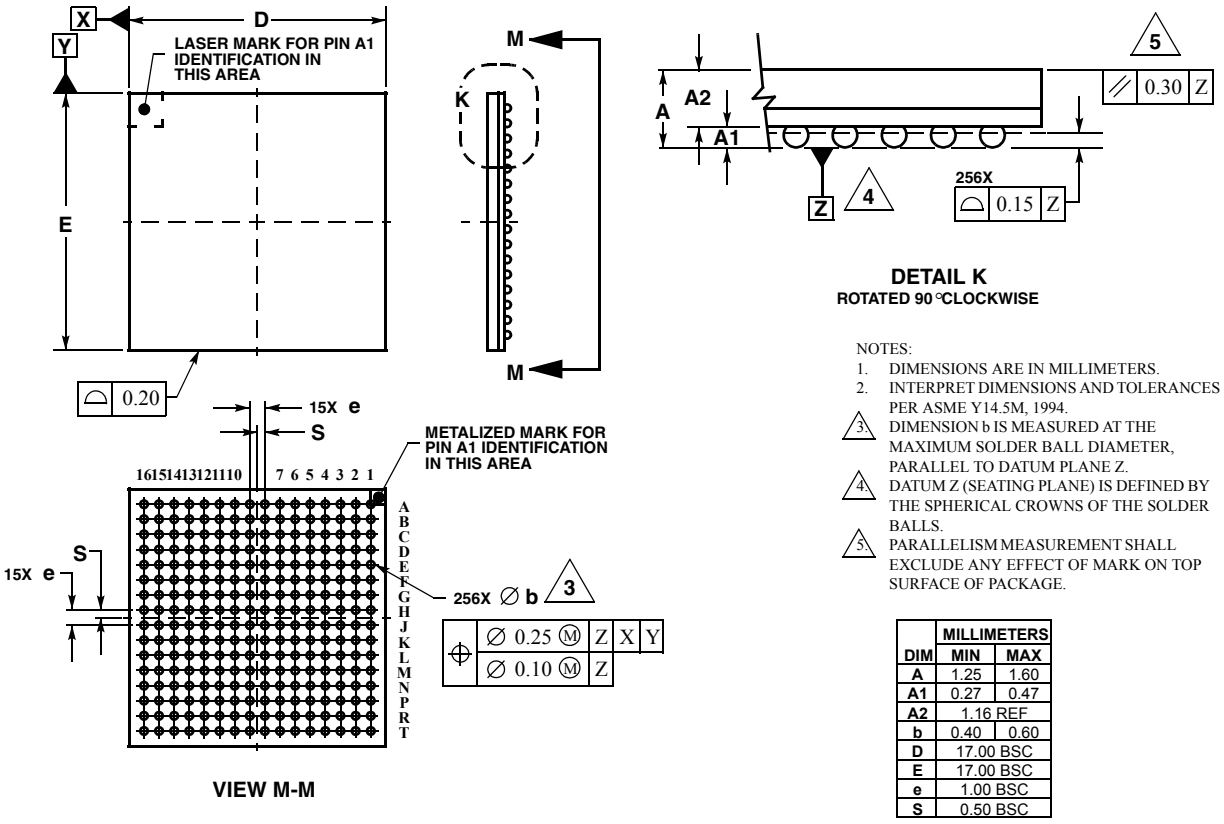
Figure 3 is a consolidated MCF5274/75 pinout for the 256 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FEC1_ RXD1	FEC1_ RXDV	FEC1_ CRS	FEC1_ COL	FEC0_ COL	FEC0_ MDIO	U0RXD	U1RXD	VSS	A23	A20	A17	A14	SD_ VREF	VSS	A
B	FEC1_ RXD3	FEC1_ RXD2	FEC1_ RXD0	FEC1_ RXCLK	FEC0_ RXDV	FEC0_ RXCLK	FEC0_ MDC	U0TXD	U1TXD	I2C_ SDA	A22	A19	A16	A13	A11	A9	B
C	FEC1_ TXCLK	FEC1_ RXER	FEC0_ TXCLK	FEC0_ RXER	FEC0_ RXD2	FEC0_ RXD0	FEC0_ CRS	$\overline{\text{U0CTS}}$	$\overline{\text{U1CTS}}$	I2C_ SCL	A21	A18	A15	A12	A10	A8	C
D	FEC1_ TXER	FEC1_ TXEN	FEC0_ TXER	FEC0_ TXEN	FEC0_ RXD3	FEC0_ RXD1	$\overline{\text{U0RTS}}$	VDD	$\overline{\text{U1RTS}}$	$\overline{\text{CS7}}$	$\overline{\text{CS6}}$	$\overline{\text{CS5}}$	$\overline{\text{CS4}}$	A7	A6	TSIZ1	D
E	FEC1_ TXD3	FEC1_ TXD2	FEC0_ TXD3	NC	VSS	OVDD	OVDD	OVDD	SD_VDD	SD_VDD	SD_VDD	VSS	$\overline{\text{CS3}}$	A5	A4	A3	E
F	FEC1_ TXD0	FEC1_ TXD1	FEC0_ TXD2	FEC0_ TXD1	OVDD	VSS	OVDD	OVDD	SD_VDD	SD_VDD	VSS	SD_VDD	$\overline{\text{CS2}}$	A2	A1	A0	F
G	FEC1_ MDIO	FEC1_ MDC	DT0OUT	FEC0_ TXD0	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	$\overline{\text{IRQ7}}$	USB_ SPEED	USB_ CLK	TSIZ0	G
H	DT1IN	DT1OUT	DT0IN	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	VDD	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ6}}$	H
J	VSS	DT2IN	DT2OUT	DT3IN	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ3}}$	USB_RP	USB_RN	J
K	$\overline{\text{OE}}$	$\overline{\text{SD_WE}}$	DT3OUT	VDD	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\text{IRQ1}}$	USB_TN	USB_TP	VSSPLL	K
L	$\overline{\text{SD_ SCAS}}$	$\overline{\text{SD_ SRAS}}$	SD_CKE	$\overline{\text{TS}}$	SD_VDD	VSS	SD_VDD	SD_VDD	OVDD	OVDD	VSS	OVDD	$\overline{\text{TA}}$	USB_ TXEN	USB_ RXD	EXTAL	L
M	D31	$\overline{\text{SD_CS1}}$	$\overline{\text{BS3}}$	SD_DQS3	VSS	SD_VDD	SD_VDD	SD_VDD	OVDD	OVDD	OVDD	NC	USB_ SUSP	PLL_ TEST	VDDPLL	XTAL	M
N	D30	D29	D28	D20	D16	SD_A10	$\overline{\text{CS1}}$	VDD	TEST	DDATA2	DDATA0	QSPI_ CS2	CLK MOD1	$\overline{\text{RSTOUT}}$	$\overline{\text{RESET}}$	VSS	N
P	D27	D26	D23	D19	SD_DQS2	$\overline{\text{TIP}}$	R/$\overline{\text{W}}$	$\overline{\text{RCON}}$	$\overline{\text{U2CTS}}$	DDATA3	DDATA1	QSPI_ CS0	CLK MOD0	$\overline{\text{TRST}}$/ DSCLK	TDO/ DSO	TCLK/ PSTCLK	P
R	D25	D24	D22	D18	$\overline{\text{BS2}}$	$\overline{\text{CS0}}$	VSS	$\overline{\text{U2RTS}}$	U2TXD	PST2	PST0	QSPI_ DOUT	QSPI_ CS3	JTAG_ EN	TMS/ $\overline{\text{BKPT}}$	TDI/DSI	R
T	VSS	SD_ VREF	D21	D17	$\overline{\text{SD_CS0}}$	$\overline{\text{DDR_CLK OUT}}$	DDR_CLK OUT	$\overline{\text{TEA}}$	U2RXD	PST3	PST1	CLKOUT	QSPI_ DIN	QSPI_ CS1	QSPI_ CLK	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. MCF5274 and MCF5275 Pinout (256 MAPBGA)

6.2 Package Dimensions - 256 MAPBGA

Figure 6 shows MCF5275 256 MAPBGA package dimensions.



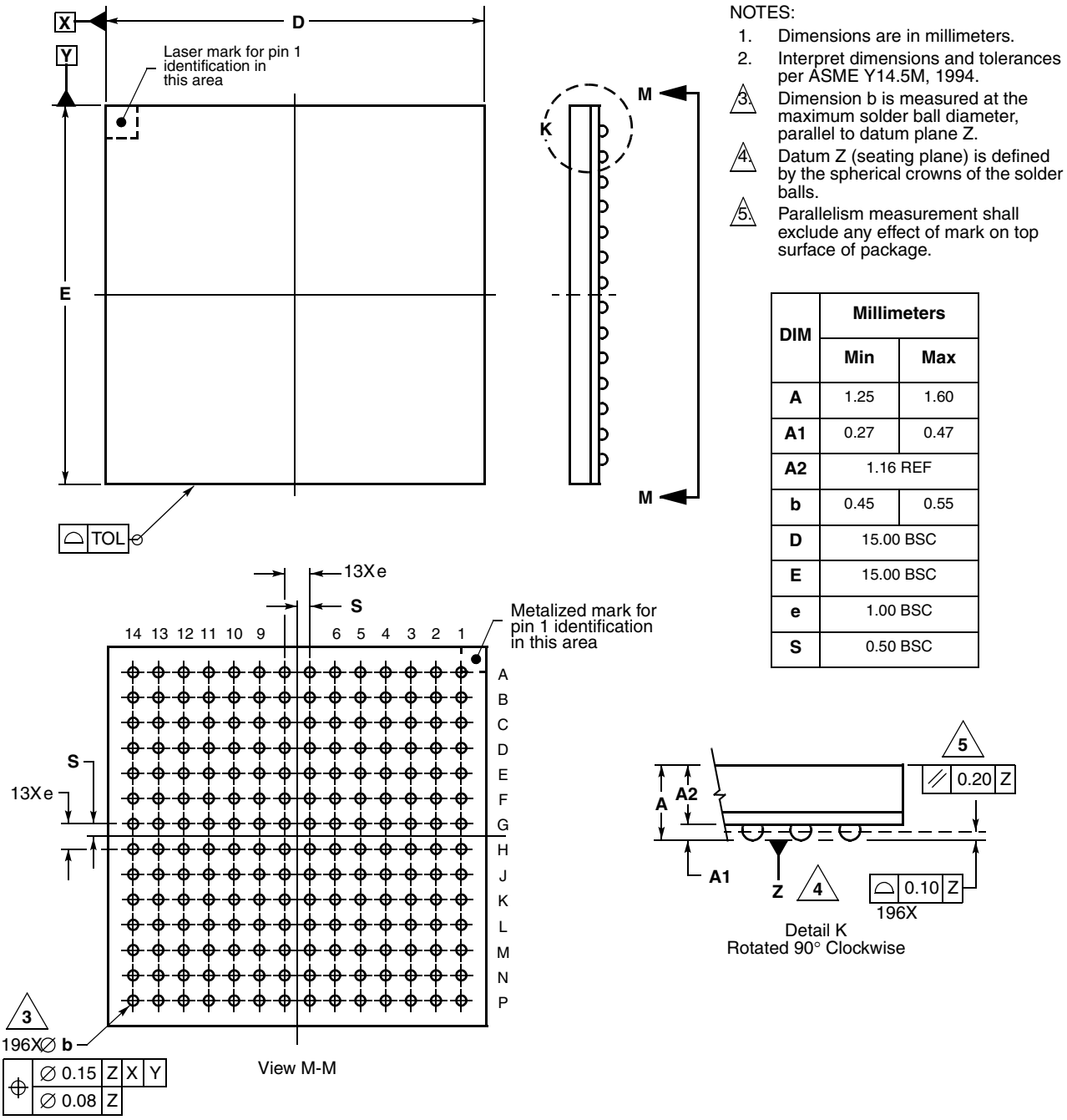
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

DIM	MILLIMETERS MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 4. 256 MAPBGA Package Dimensions

6.4 Package Dimensions - 196 MAPBGA

Figure 6 shows MCF5275 196 MAPBGA package dimensions.



DIM	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 6. 196 MAPBGA Package Dimensions

7 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5274LVM166	MCF5274L RISC Microprocessor	196 MAPBGA	166 MHz	0° to +70° C
MCF5274LCVM166				-40° to +85° C
MCF5274VM166	MCF5274 RISC Microprocessor	256 MAPBGA	166 MHz	0° to +70° C
MCF5274CVM166				-40° to +85° C
MCF5275LCVM166	MCF5275L RISC Microprocessor	196 MAPBGA	166 MHz	-40° to +85° C
MCF5275CVM166	MCF5275 RISC Microprocessor	256 MAPBGA	166 MHz	-40° to +85° C

8 Electrical Characteristics

This appendix contains electrical specification tables and reference timing diagrams for the MCF5275 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5275.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

8.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
I/O Pad Supply Voltage (3.3V)	OV_{DD}	– 0.3 to +4.0	V
Memory Interface SSTL 2.5V Pad Supply Voltage	SDV_{DD}	– 0.3 to + 2.8	V
Memory Interface SSTL 3.3V Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

P_{INT} = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

8.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V
ESD Target for Machine Model	MM	200	V
HBM Circuit Description	R_{series}	1500	Ω
	C	100	pF
MM Circuit Description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) positive pulses negative pulses	 — —	 3 3	—
Interval of Pulses	—	1	sec

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 10. DC Electrical Specifications[1] (continued)

Characteristic	Symbol	Min	Max	Unit
Load Capacitance[7] Low Drive Strength High Drive Strength	C_L	 — —	 25 50	pF
Core Operating Supply Current[8] Master Mode WAIT DOZE STOP	I_{DD}	 — — — —	 175 15 10 100	 mA mA mA µA
I/O Pad Operating Supply Current Master Mode Low Power Modes	OI_{DD}	 — —	 250 250	 mA µA
DC Injection Current [3, 9, 10, 11] $V_{NEGCLAMP}$ =V_{SS}– 0.3 V, $V_{POSCLAMP}$ = V_{DD} + 0.3 Single Pin Limit Total MCU Limit, Includes sum of all stressed pins	I_{IC}	 -1.0 -10	 1.0 10	mA

1 Refer to Table 11 for additional PLL specifications.

2 V_{REF} is specified as a nominal value only instead of a range, so no maximum value is listed.

3 This specification is guaranteed by design and is not 100% tested.

4 The actual V_{OH} and V_{OL} values for SSTL pads are dependent on the termination and drive strength used. The specifications numbers assume no parallel termination.

5 Refer to the MCF5274 signals chapter for pins having weak internal pull-up devices.

6 This parameter is characterized before qualification rather than 100% tested.

7 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.

8 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

9 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

10 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

11 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 Proper PC board layout procedures must be followed to achieve specifications.
7 Load capacitance determined from crystal manufacturer specifications and includes circuit board parasitics.
8 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
9 Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDPLL} are valid to $\overline{RSTOUT}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
10 $t_{lpll} = (64 * 4 * 5 + 5 \times \tau) \times T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6} \times 2(MFD + 2)$
11 PLL is operating in 1:1 PLL mode.
12 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the jitter percentage for a given interval.
13 Based on slow system clock of 33MHz maximum frequency.
14 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100KHz.
15 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.
16 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

8.6 External Interface Timing Characteristics

Table 12 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 12. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
B0	CLKOUT	t_{CYC}	12	—	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	9	—	ns
B1b	$\overline{BKPT}$ valid to CLKOUT high[3]	t_{BKVCH}	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{BKPT}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:16]) valid to CLKOUT high	t_{DIVCH}	4	—	ns
B5	CLKOUT high to data input (D[31:16]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications have been indicated taking into account the full drive strength for the pads.
2 $\overline{TEA}$ and $\overline{TA}$ pins are being referred to as control inputs.
3 Refer to figure A-19.

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 13.

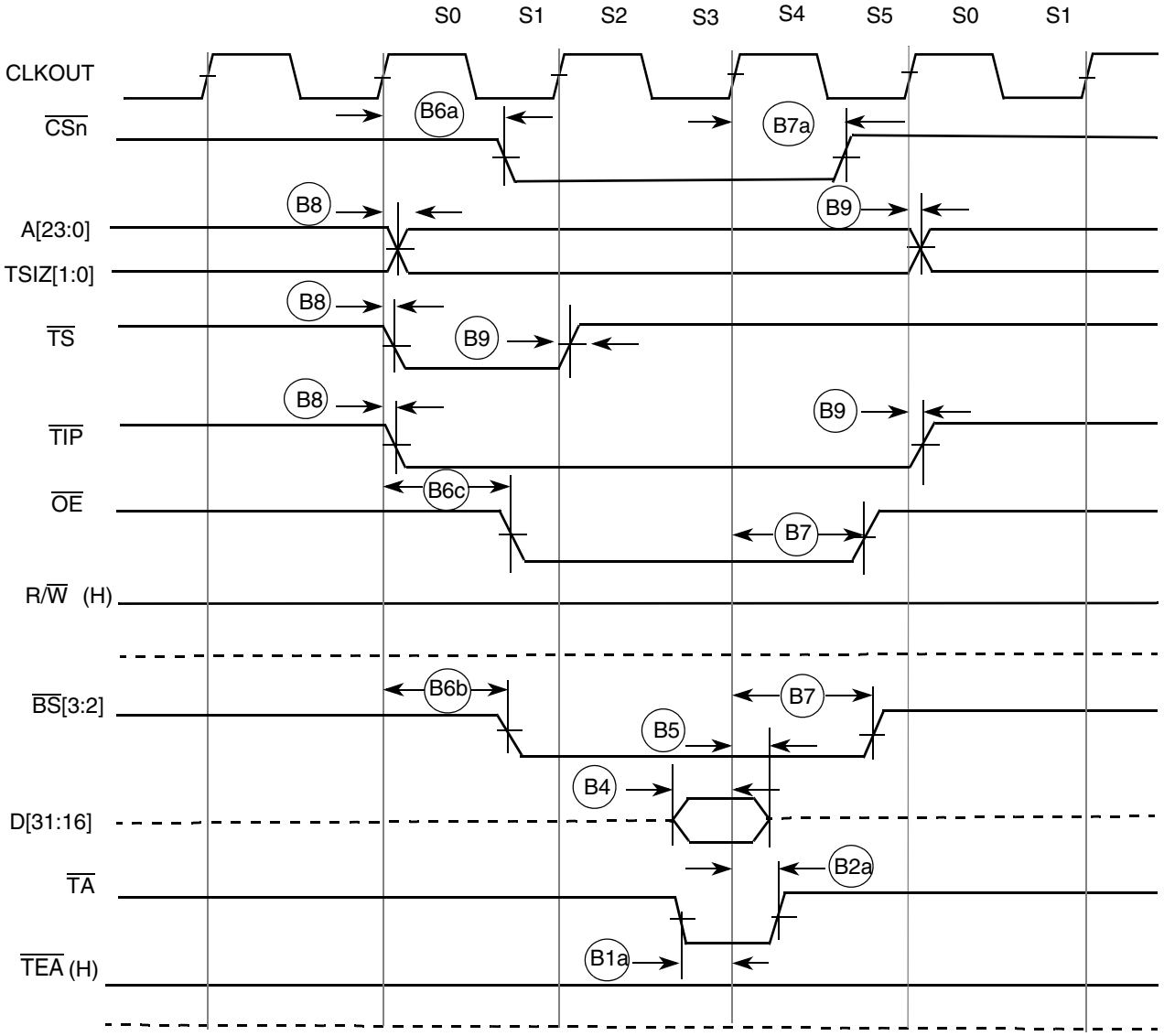


Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$

8.11 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 5.0 V or 3.3 V.

8.11.1 MII Receive Signal Timing (FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER, and FEC*n*_RXCLK)

The receiver functions correctly up to a FEC*n*_RXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC*n*_RXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER to FEC*n*_RXCLK setup	5	—	ns
M2	FEC*n*_RXCLK to FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER hold	5	—	ns
M3	FEC*n*_RXCLK pulse width high	35%	65%	FEC*n*_RXCLK period
M4	FEC*n*_RXCLK pulse width low	35%	65%	FEC*n*_RXCLK period

Figure 16 shows MII receive signal timings listed in Table 18.

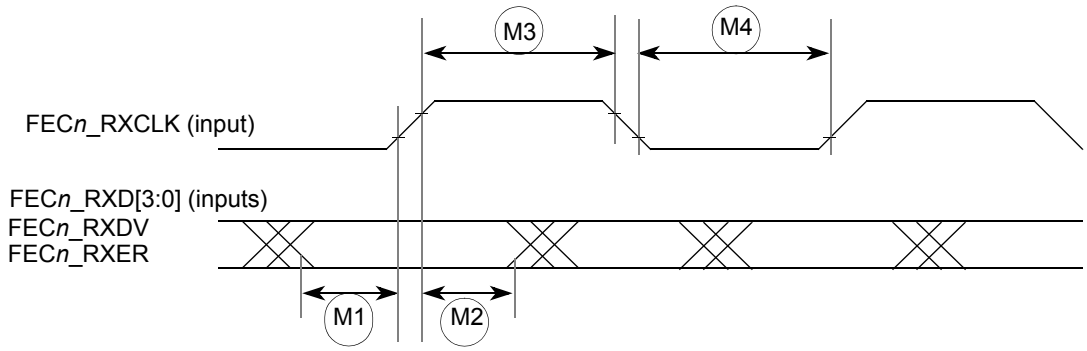


Figure 16. MII Receive Signal Timing Diagram

8.11.2 MII Transmit Signal Timing (FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER, FEC*n*_TXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC*n*_TXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC*n*_TXCLK frequency.

8.11.5 USB Interface AC Timing Specifications

Table 22 lists USB Interface timings.

Table 22. USB Interface Timing

Num	Characteristic	Min	Max	Units
US1	USB_CLK frequency of operation	48	48	MHz
US2	USB_CLK fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	2	ns
US3	USB_CLK rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	2	ns
US4	USB_CLK duty cycle (at 0.5 x O V_{DD})	45	55	%
Data Inputs				
US5	USB_RP, USB_RN, USB_RXD valid to USB_CLK high	6	—	ns
US6	USB_CLK high to USB_RP, USB_RN, USB_RXD invalid	6	—	ns
Data Outputs				
US7	USB_CLK high to USB_TP, USB_TN, USB_SUSP valid	—	12	ns
US8	USB_CLK high to USB_TP, USB_TN, USB_SUSP invalid	3	—	ns

Figure 20 shows USB interface timings listed in Table 22.

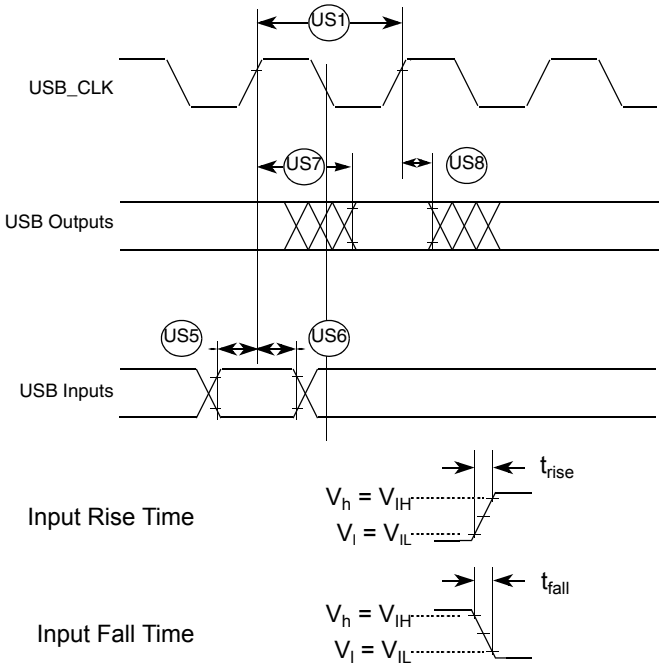


Figure 20. USB Signals Timing Diagram

8.12 I²C Input/Output Timing Specifications

Table 23 lists specifications for the I²C input timing parameters shown in Figure 21.

Table 23. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2 x t_{CYC}	—	ns
I2	Clock low period	8 x t_{CYC}	—	ns
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4 x t_{CYC}	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2 x t_{CYC}	—	ns
I9	Stop condition setup time	2 x t_{CYC}	—	ns

Table 24 lists specifications for the I²C output timing parameters shown in Figure 21.

Table 24. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6 x t_{CYC}	—	ns
I2 [1]	Clock low period	10 x t_{CYC}	—	ns
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7 x t_{CYC}	—	ns
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10 x t_{CYC}	—	ns
I7 [1]	Data setup time	2 x t_{CYC}	—	ns
I8 [1]	Start condition setup time (for repeated start condition only)	20 x t_{CYC}	—	ns
I9 [1]	Stop condition setup time	10 x t_{CYC}	—	ns

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 24. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 24 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

9 Documentation

Documentation regarding the MCF5275 and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

10 Revision History

Table 29 provides a revision history for this hardware specification.

Table 29. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.
1	Added Figure 6.
1.1	Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	Removed Overview, Features, Signal Descriptions, Modes of Operation, and Address Multiplexing sections. This information can be found in the MCF5275 Reference Manual. Removed list of documentation in Section 9, "Documentation.". An up-to-date list is always available on our web site. Changed CLKOUT -> PSTCLK in Section 8.16, "Debug AC Timing Specifications." Table 10: Update V_{DD} spec from 1.35-1.65 to 1.4-1.6. Table 13: Timings B6a, B6b, B6c, B7, B7a, B9, B12 updated: B6a, B6b, B6c maximum changed from "$0.5t_{CYC}$ + 5" to "$0.5t_{CYC}$ + 5.5" B7, B7a minimum changed from "$0.5t_{CYC}$ + 1.5" to "$0.5t_{CYC}$ + 1.0" B9, B11 minimum changed from "1.5" to "1.0"
1.3	Added Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions." Added thermal characteristics for 196 MAPBGA in Table 8. Updated package dimensions drawing, Figure 6.
2	Removed second sentence from Section 8.11.1, "MII Receive Signal Timing (FECn_RXD[3:0], FECn_RXDV, FECn_RXER, and FECn_RXCLK)," and Section 8.11.2, "MII Transmit Signal Timing (FECn_TXD[3:0], FECn_TXEN, FECn_TXER, FECn_TXCLK)," regarding no minimum frequency requirement for TXCLK. Removed third and fourth paragraphs from Section 8.11.2, "MII Transmit Signal Timing (FECn_TXD[3:0], FECn_TXEN, FECn_TXER, FECn_TXCLK)," as this feature is not supported on this device.
3	Corrected Ordering Information, Table 6. Figure 2: Moved $PLLV_{DD}$ from 1.5V to 3.3V supply line and corrected relevant text in sections below table. Table 10: Corrected maximum "Input High Voltage 3.3V I/O Pads", V_{IH} specification.
4	Table 10, added PLL supply voltage row

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